Building and Programming complete MPSoCs in reconfigurable systems

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MPsoC 2007

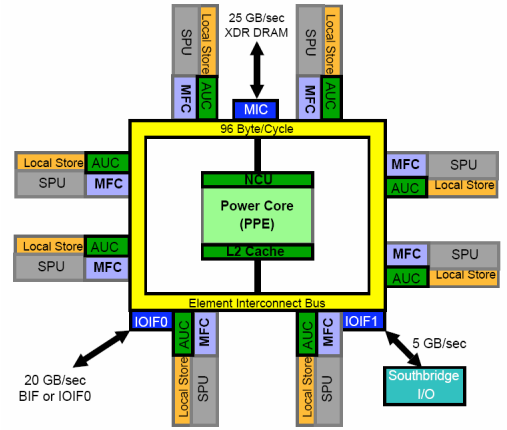
XILINX®

Outline

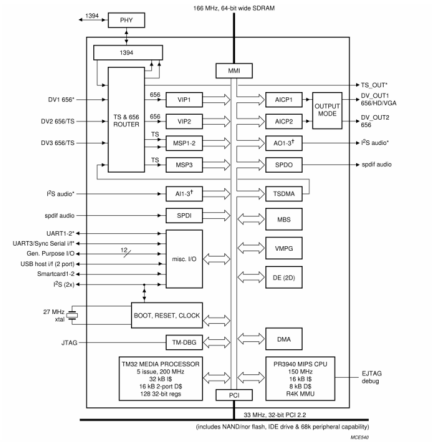
- Control Processors and Operating Systems in FPGAs
- XUP, HDTV processing
- UC Berkeley Bee2 and programming
- Bee3 sneak peak

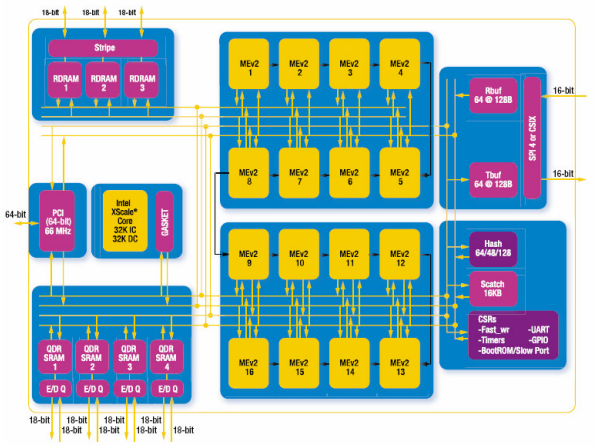
Control Processors Everywhere

IBM/Sony Cell Processor (Media + computing)

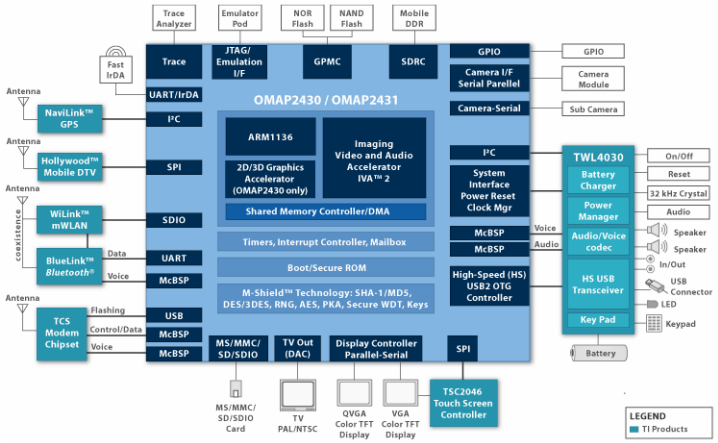


Nexperia PNX8526 (Digital TV)



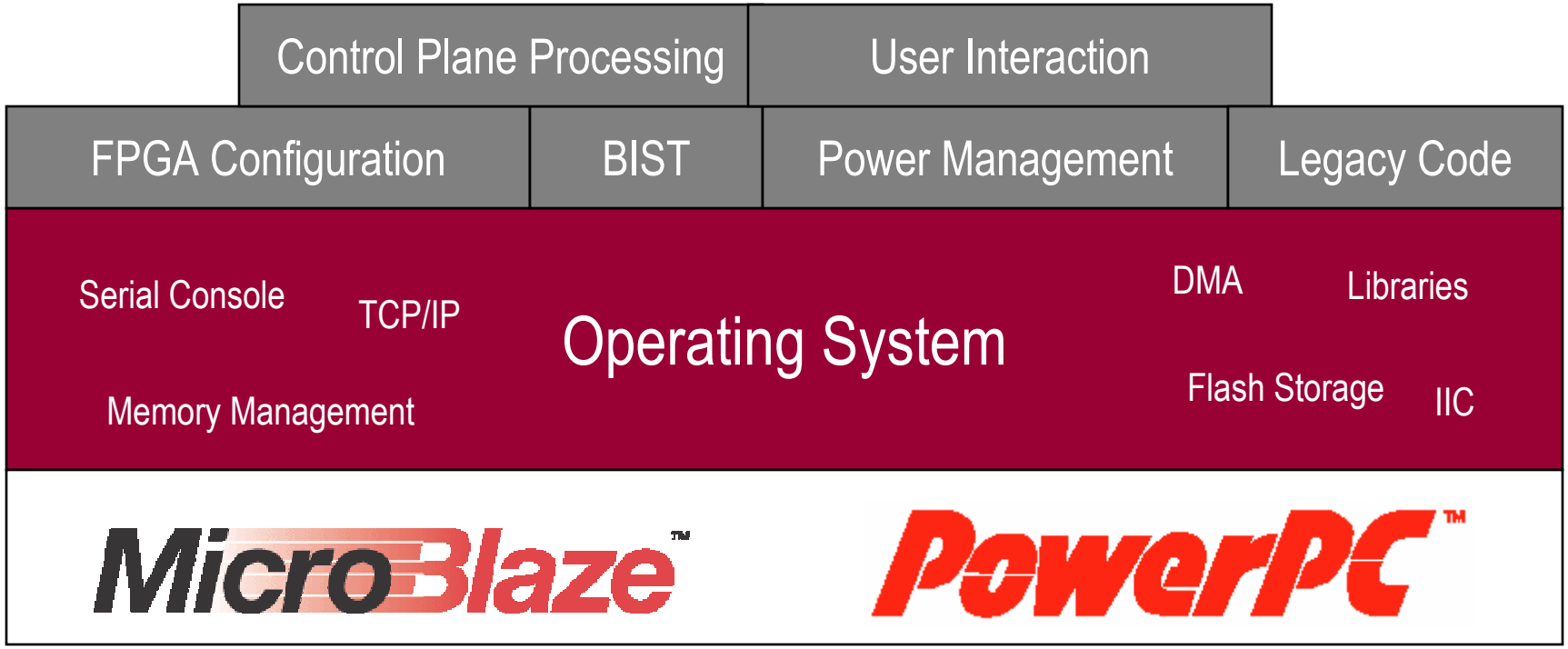


Intel IXP2800 (Network Processing)



TI OMAP2430 (Cell Phone Handsets)

Control Processors in FPGAs

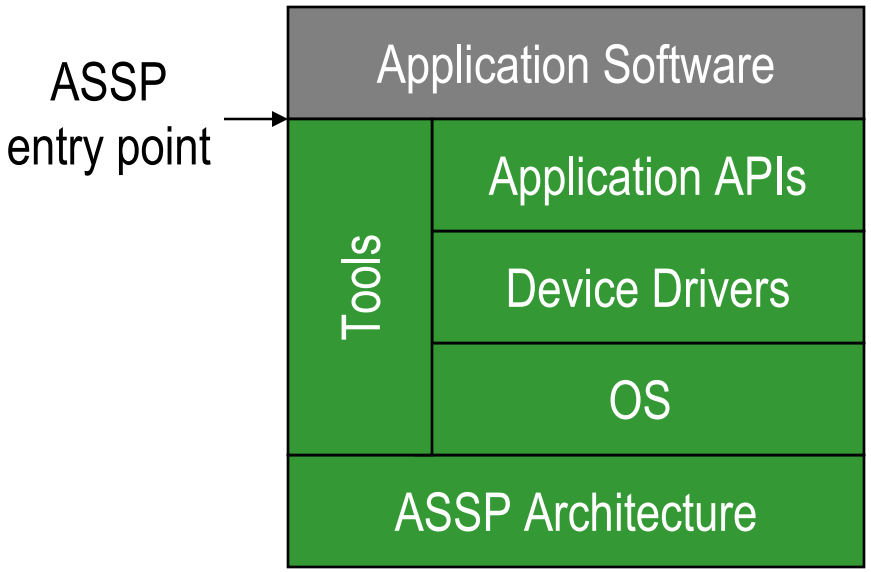


75% of processor users also use an Operating System

Key OS Properties

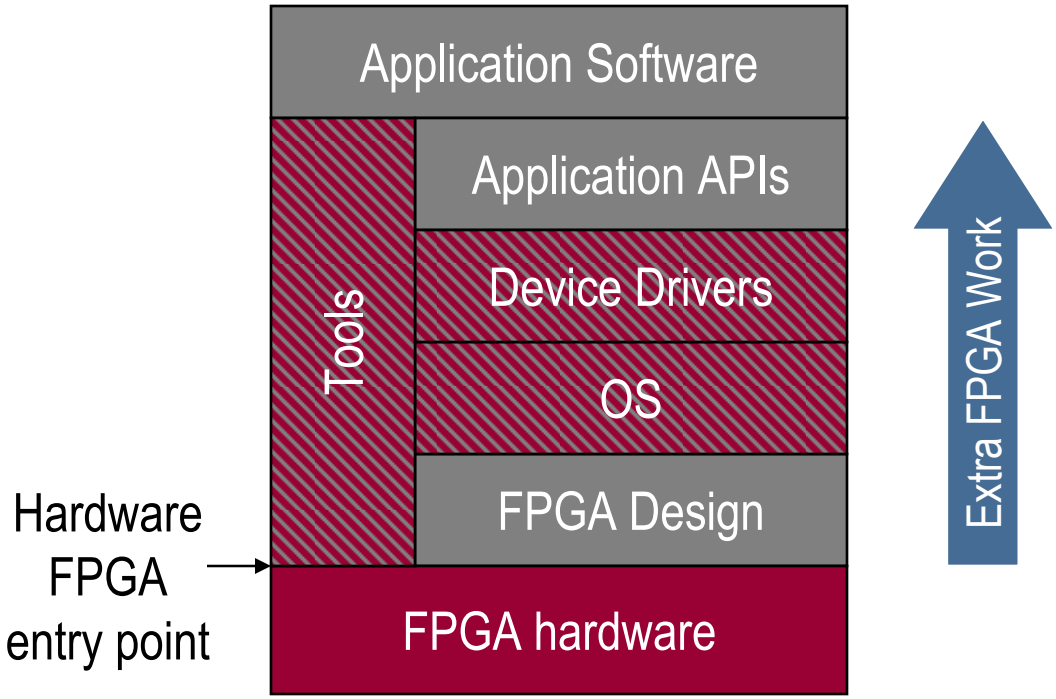
- An OS is more than hardware APIs.
- Basic properties:
  - No user code can ever crash the operating system
  - Framework for modularity and extensibility
  - Fair sharing of resources for independent users
    - Includes anything from simple locking to QOS guarantees
- These properties are crucial for debugging, and design-in-the-large.

ASSP Software Platform



- Most processor/ASSP vendors implement new architectures relatively rarely.
  - maybe every 1-3 years.
- New architectures typically require some porting and verification.

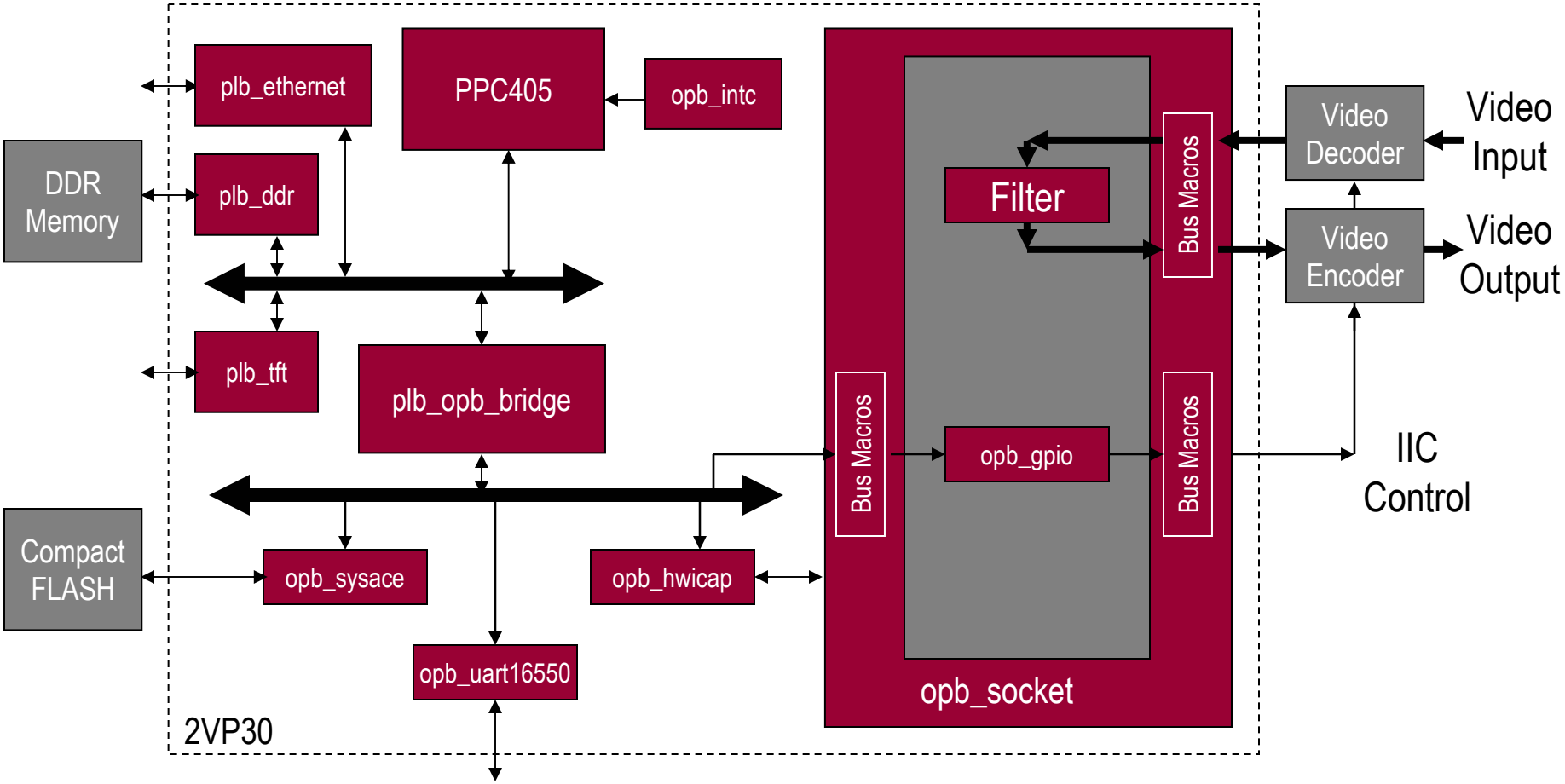
FPGA Software Platform



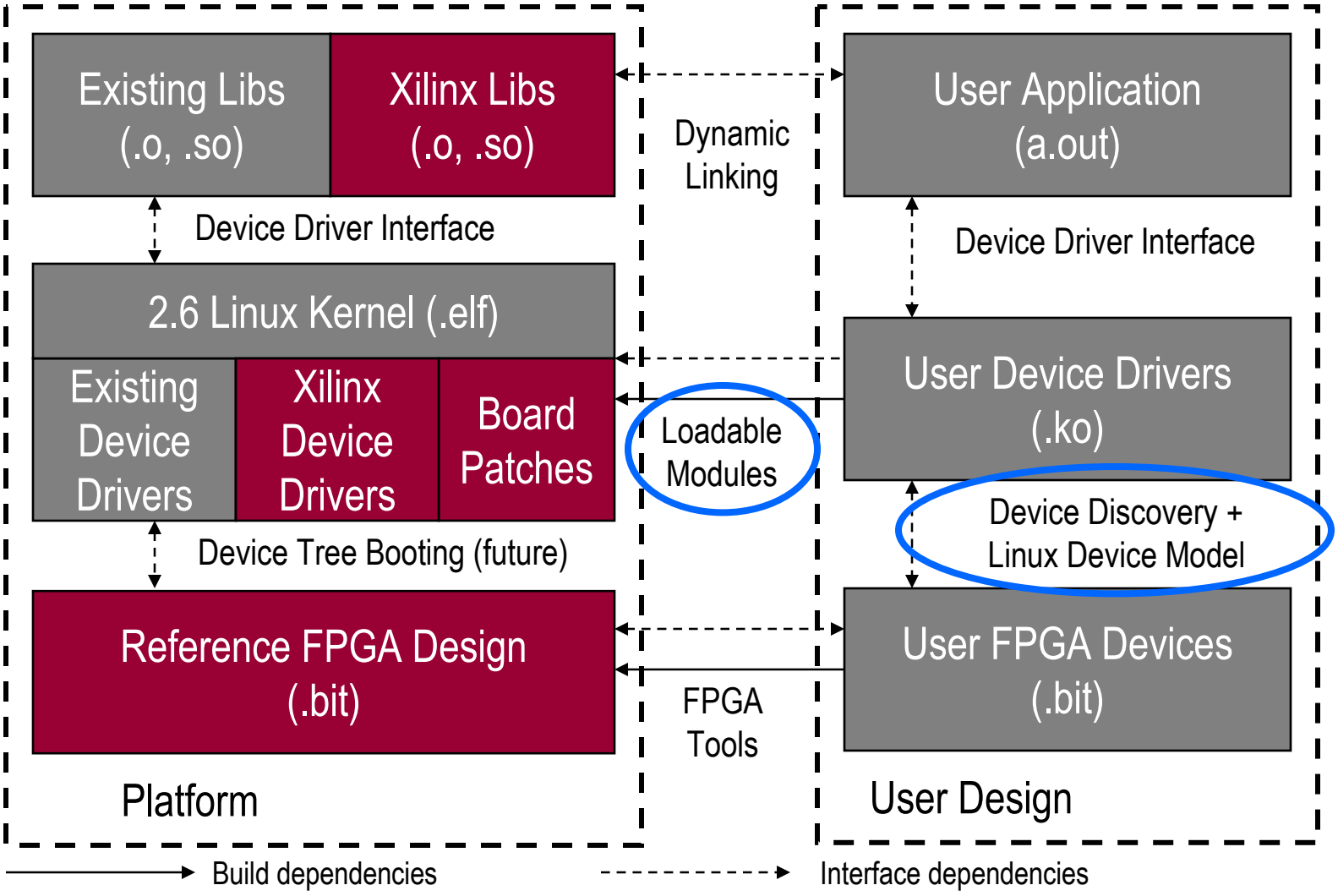
Domain and board specific additional System Architectures

Challenge: Building a generic software platform for user-specified hardware

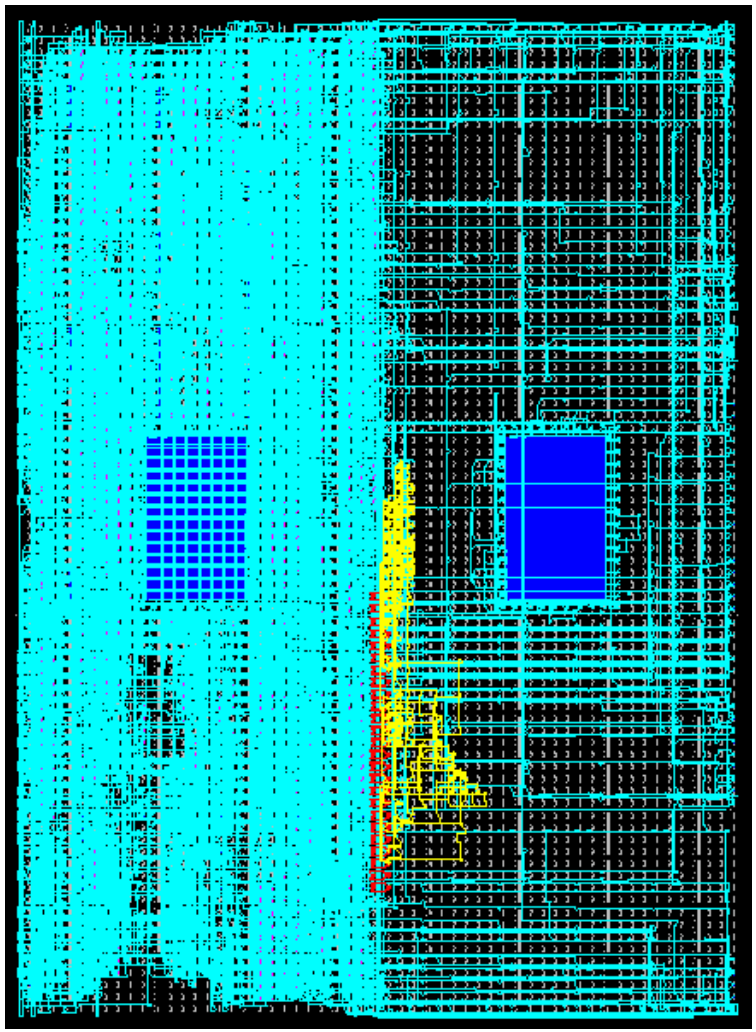
Demonstration Architecture



Achieving Decoupling



Demonstration Design



Static Processor Subsystem

Interfaces

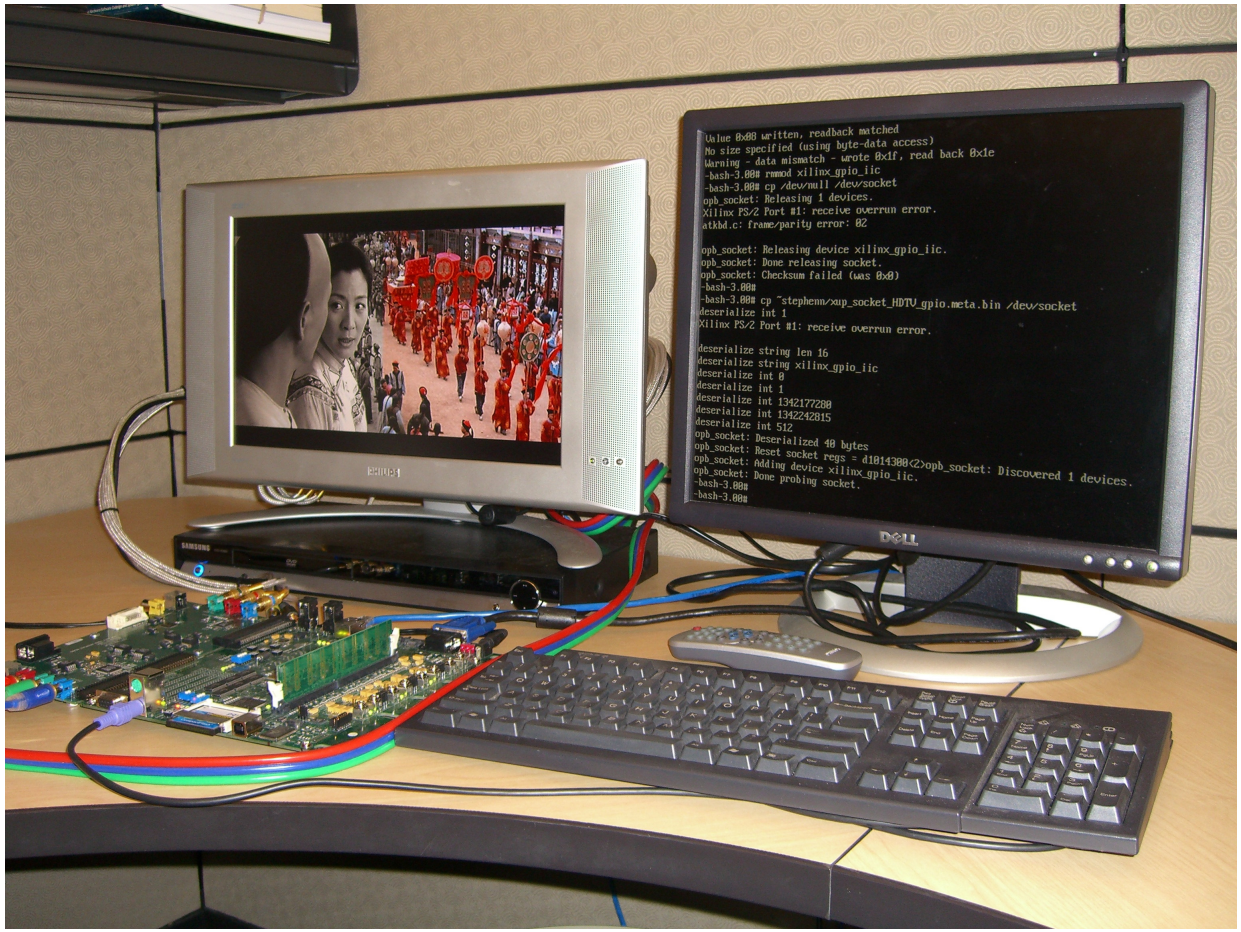
Video Filter + IIC

6850 4-LUTs (unoptimized)
24% of 2VP30
8% of 4VFX100

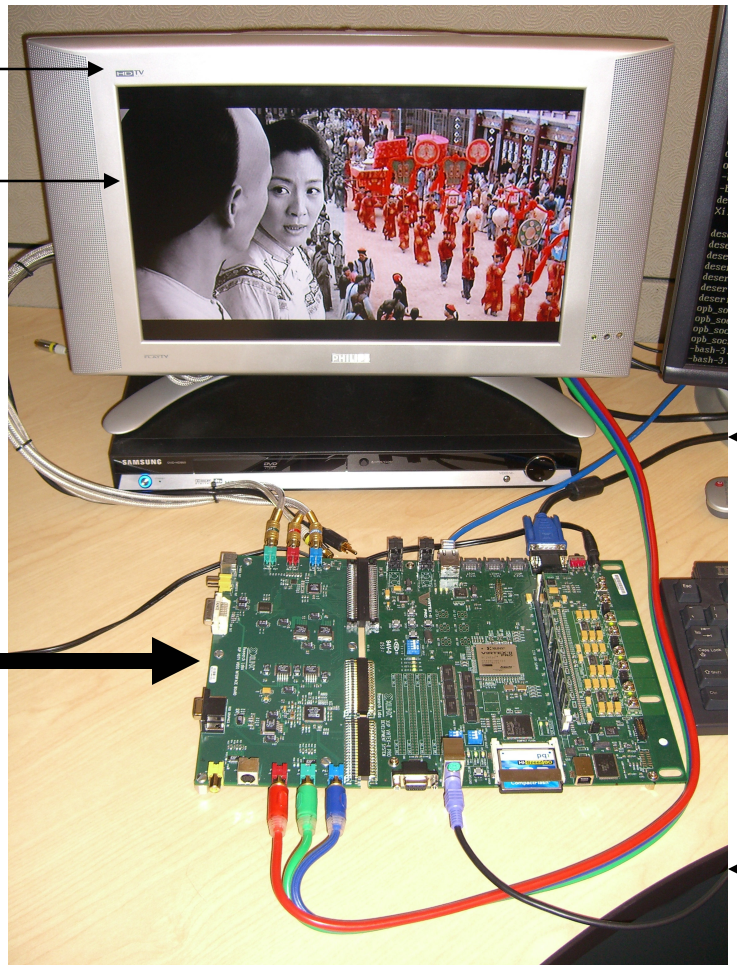
Demonstration

- Boot generic processor subsystem with empty socket.
  - Load static configuration from SystemACE.
  - Load Linux Bootloader + Kernel from SystemACE.
  - Decompress Linux Kernel and start executing.
  - Load Root Filesystem over NFS.
  - Load Kernel modules from Root Filesystem
- Load application-specific partial bitstream
  - stored on NFS.
- Load meta-information
  - Kernel loads appropriate device drivers.
  - Enable Bus Macros
- HDTV video signal processing, in this demo a simple filter

Demonstration system



The FPGA system



UC Berkeley, Xilinx and Microsoft Research: BEE

Special thanks to Chen Chang (UC Berkeley) and Chuck Thacker (Microsoft Research). Research of many excellent people.

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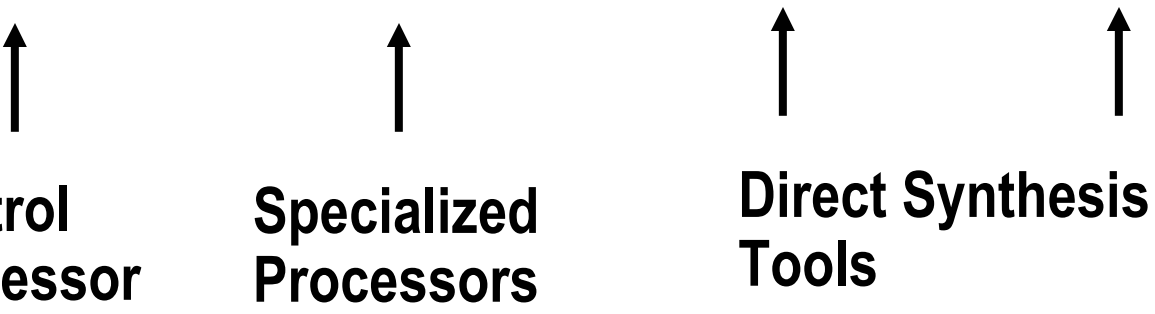
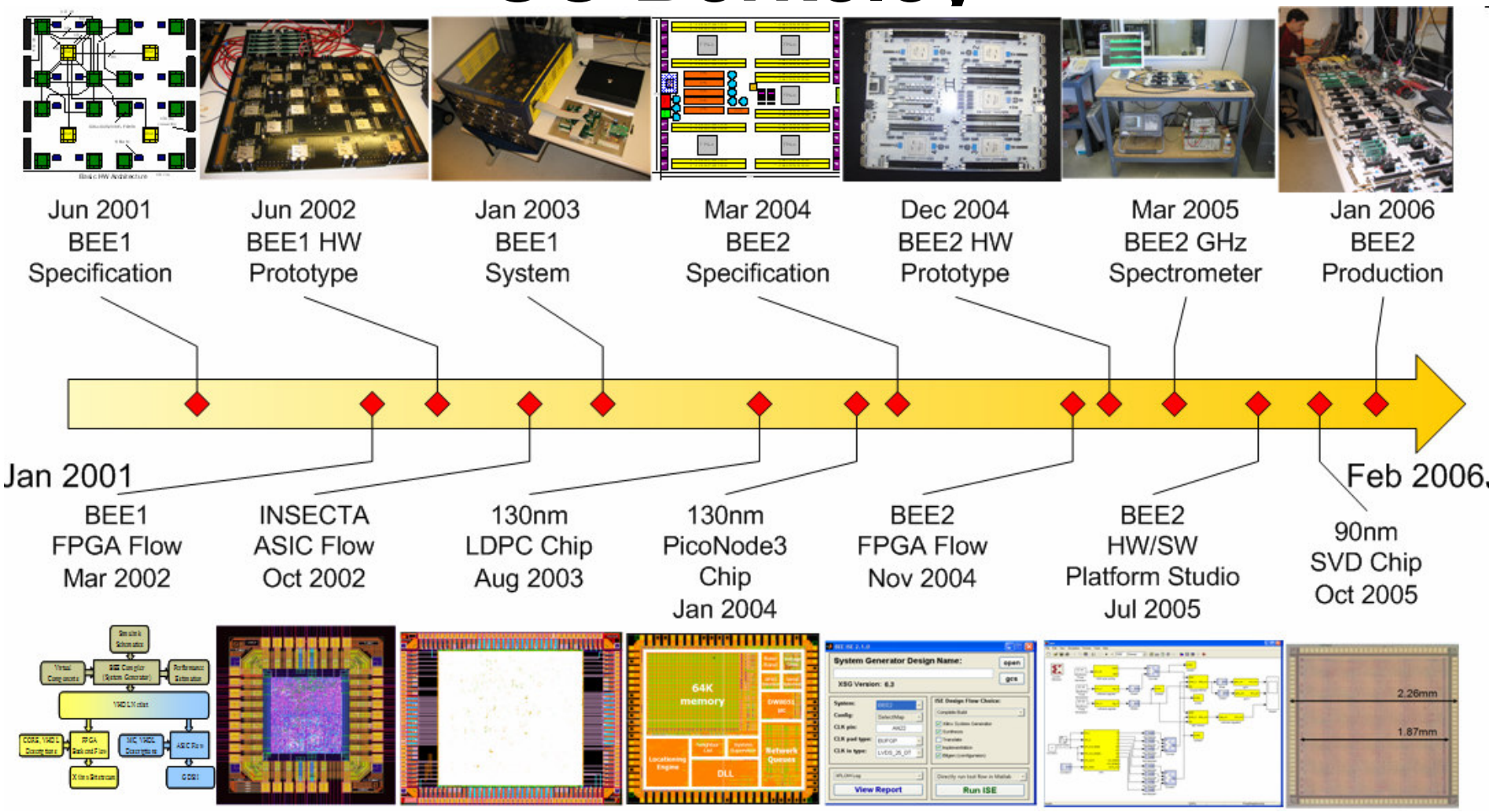
Signal Processing Systems

clock:sample	1000:1	100:1	10:1	1:1
500MHz clock	500Ks/s	5Ms/s	50Ms/s	500Ms/s
Memories	4-256KByte	4-256KByte	10KByte	1KByte
Applications	control → audio →	mobile video → HDTV → comms → radar		



History of BEE Technology at UC Berkeley



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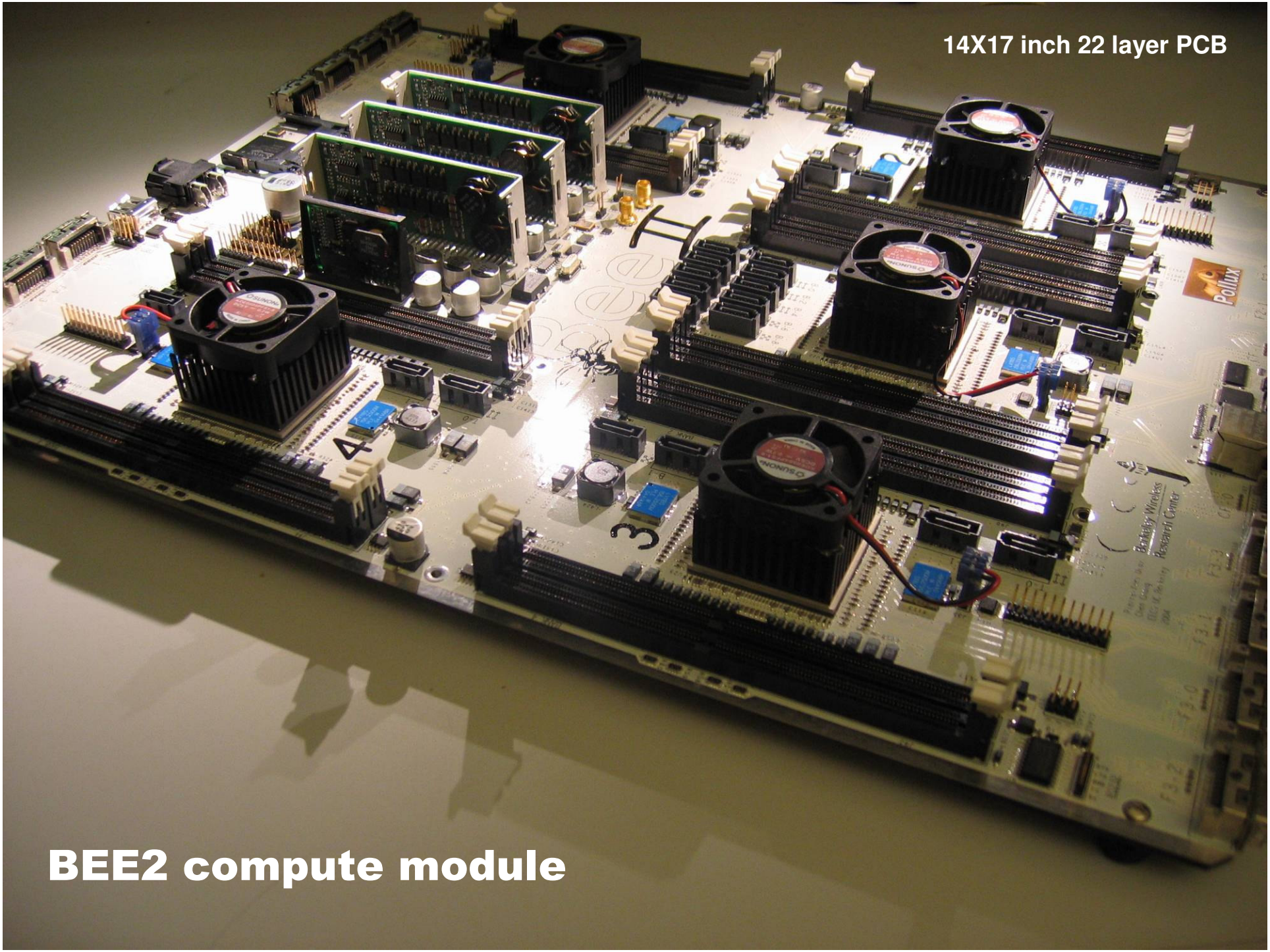
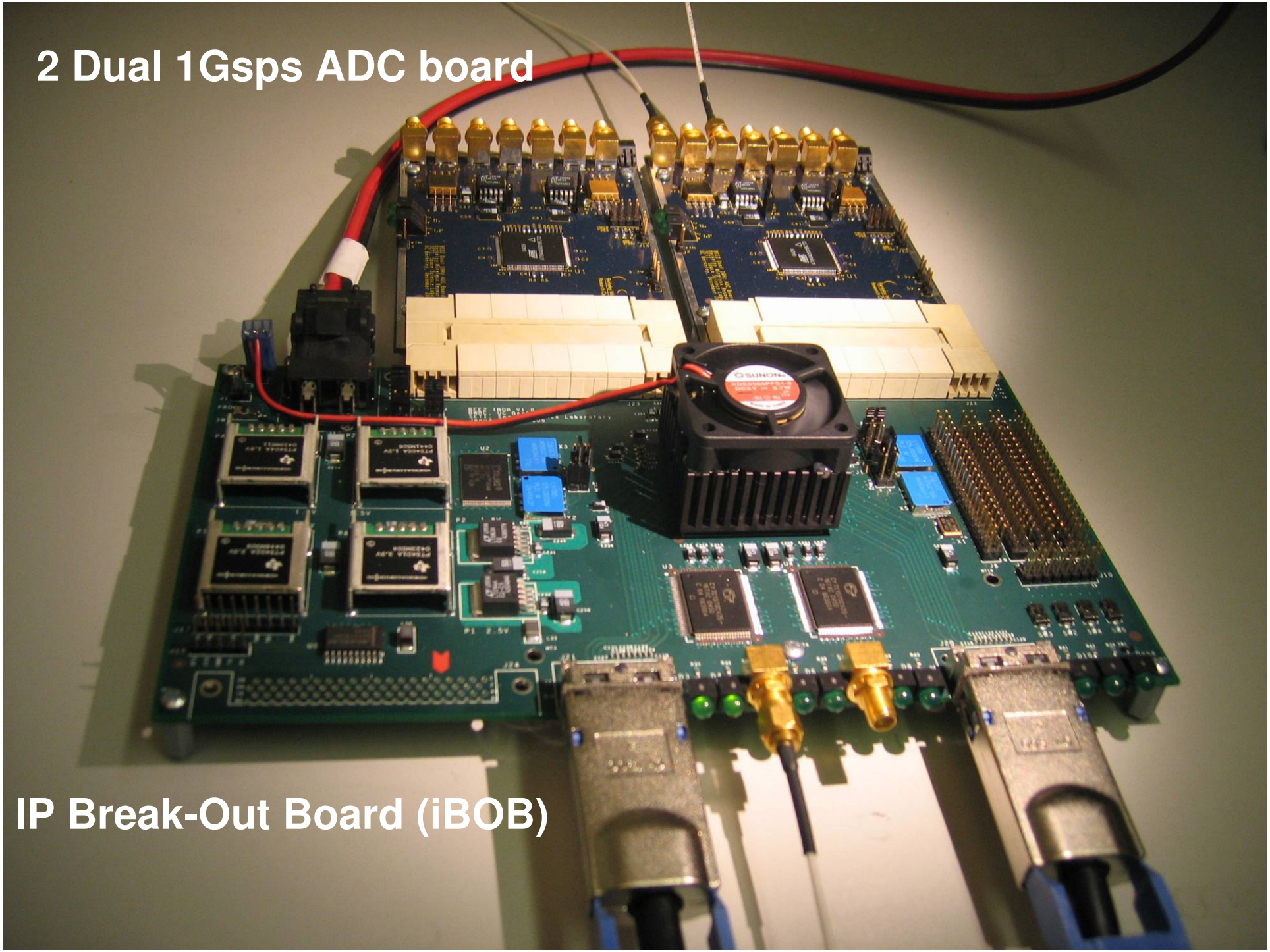
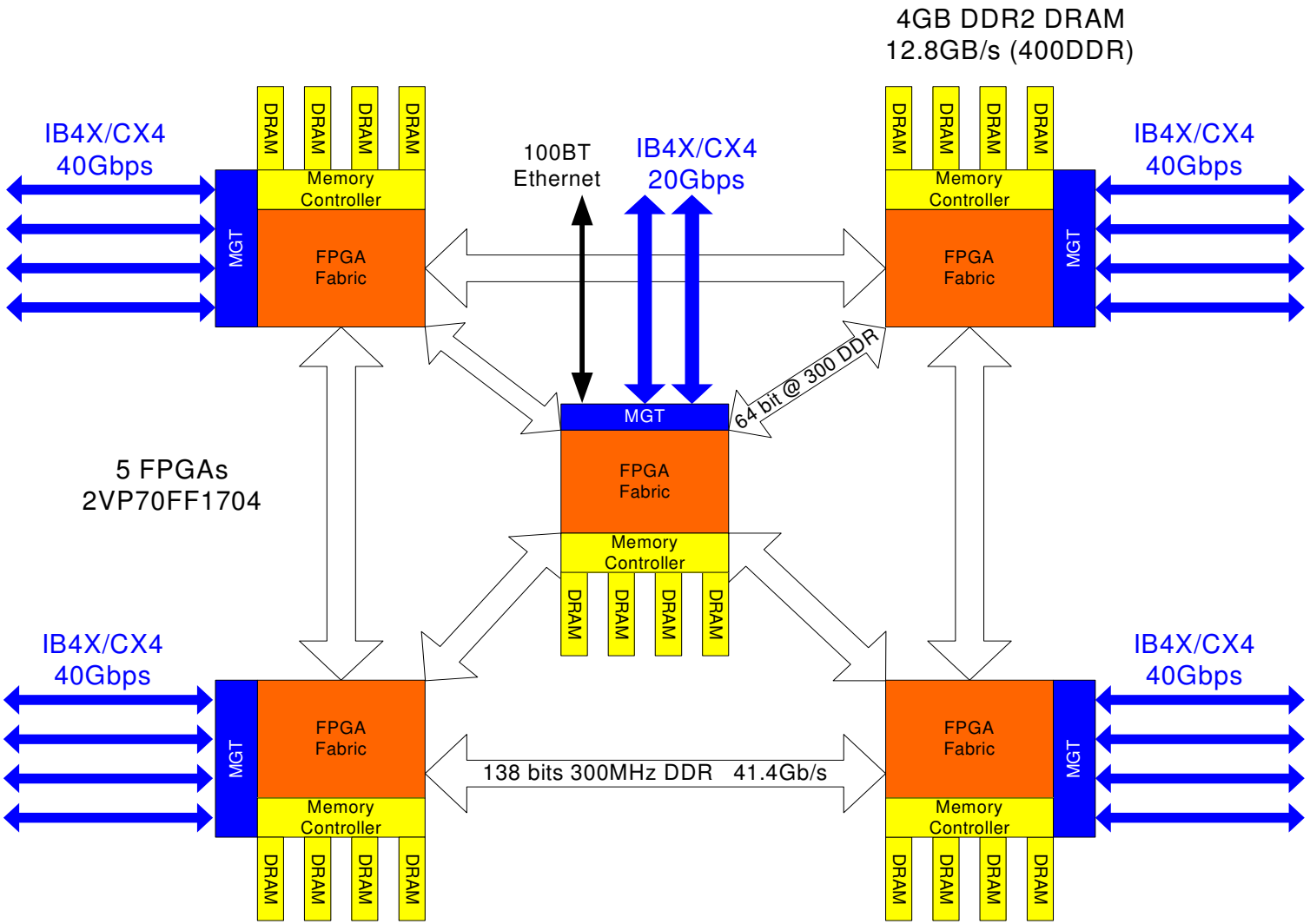

14X17 inch 22 layer PCB
Pollux
Berkeley Wireless Research Center
BEE2 compute module

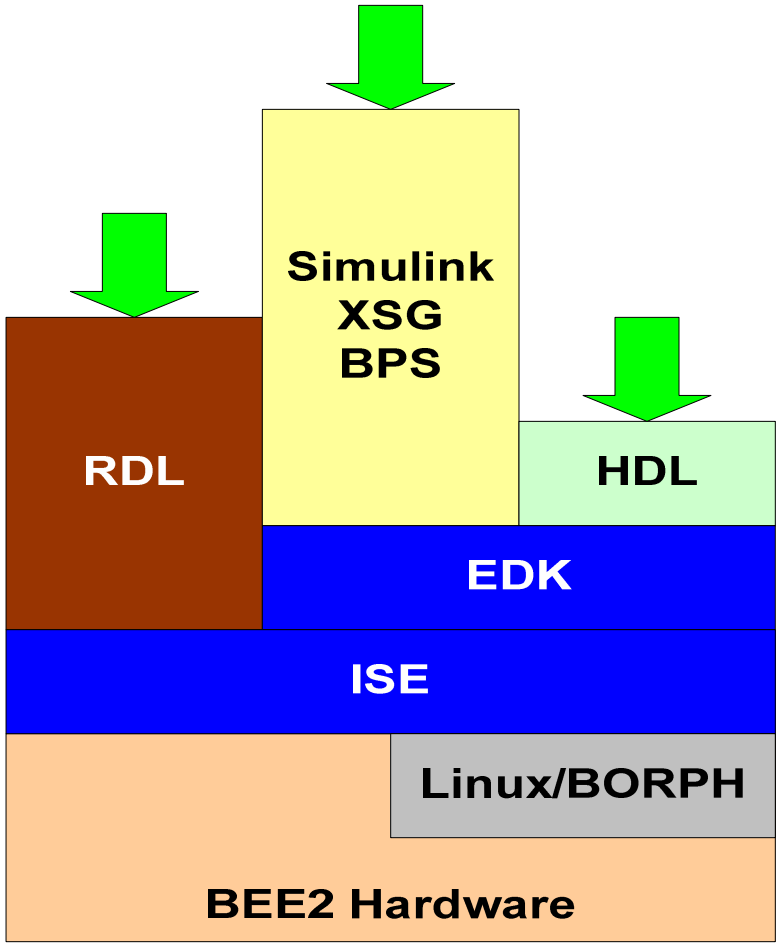

2 Dual 1Gsps ADC board
IP Break-Out Board (iBOB)

Compute Module Diagram



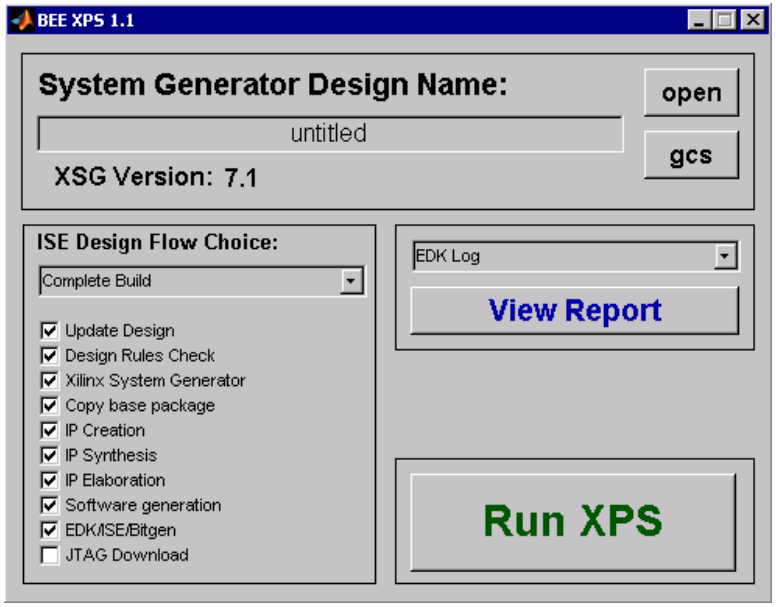
The Programming Challenge

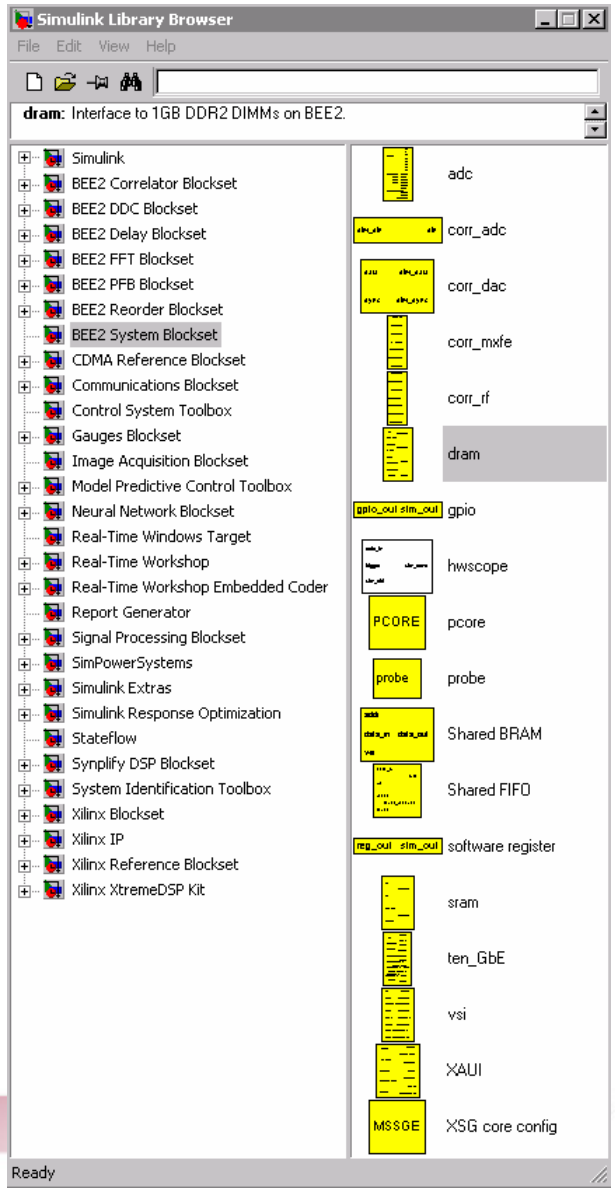
- Hardware complexity
  - Lots of FPGA resources
  - DDR2-400 DRAM
  - 10G Ethernet
  - GHz Analog I/O
  - Embedded Processor Cores
- Software integrations
  - OS: Linux, TinySH
  - Device drivers
  - User applications
- Multi-disciplined user base
  - Signal processing
  - MP emulation
  - Compute acceleration



BEE Platform Studio (BPS)

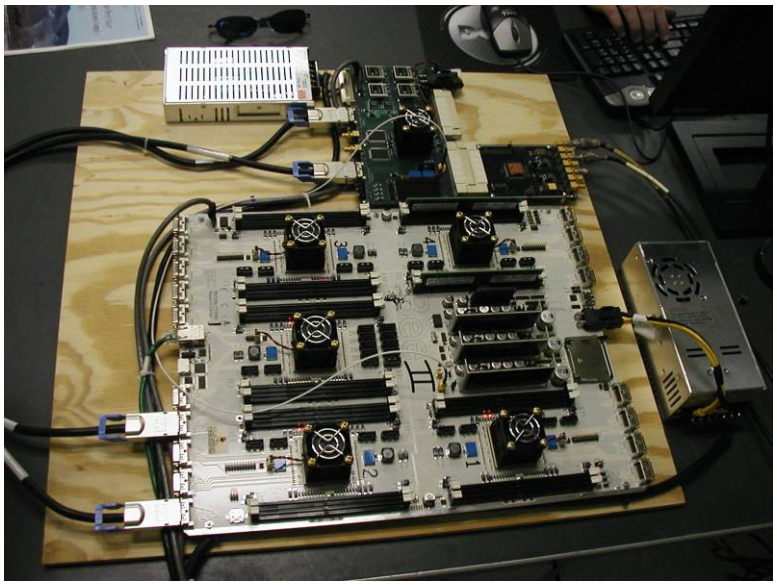
- BEE Platform Studio v1.1
  - Simulink library support for system devices
  - Full software integration with Linux OS support
  - Simple GUI in Matlab/Simulink
  - Require no knowledge of backend tool flow from end users

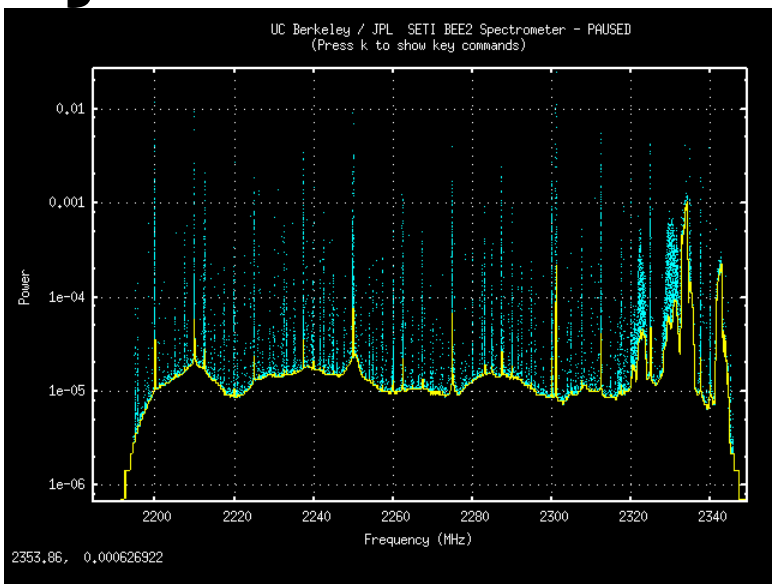


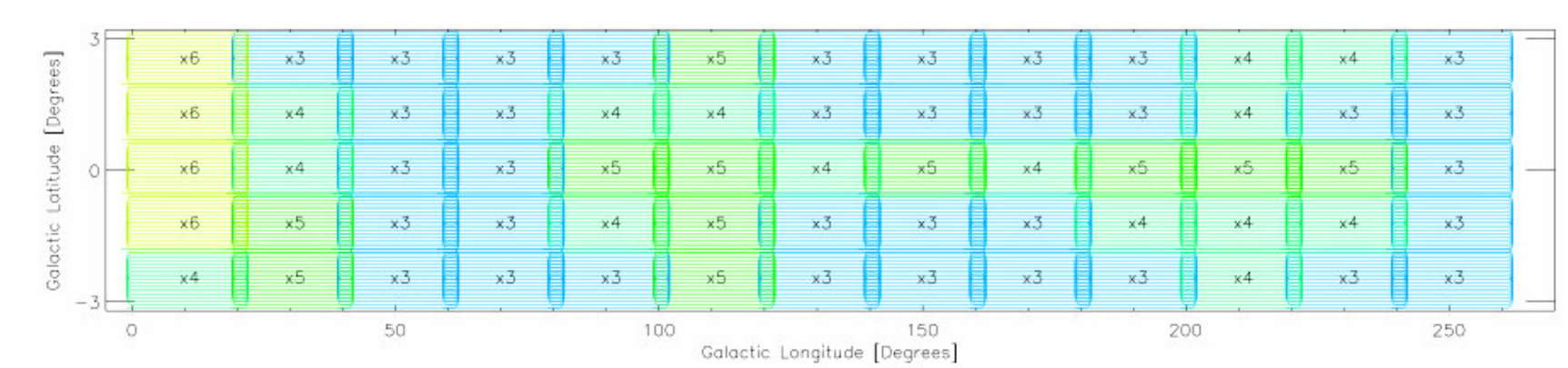


Case Study

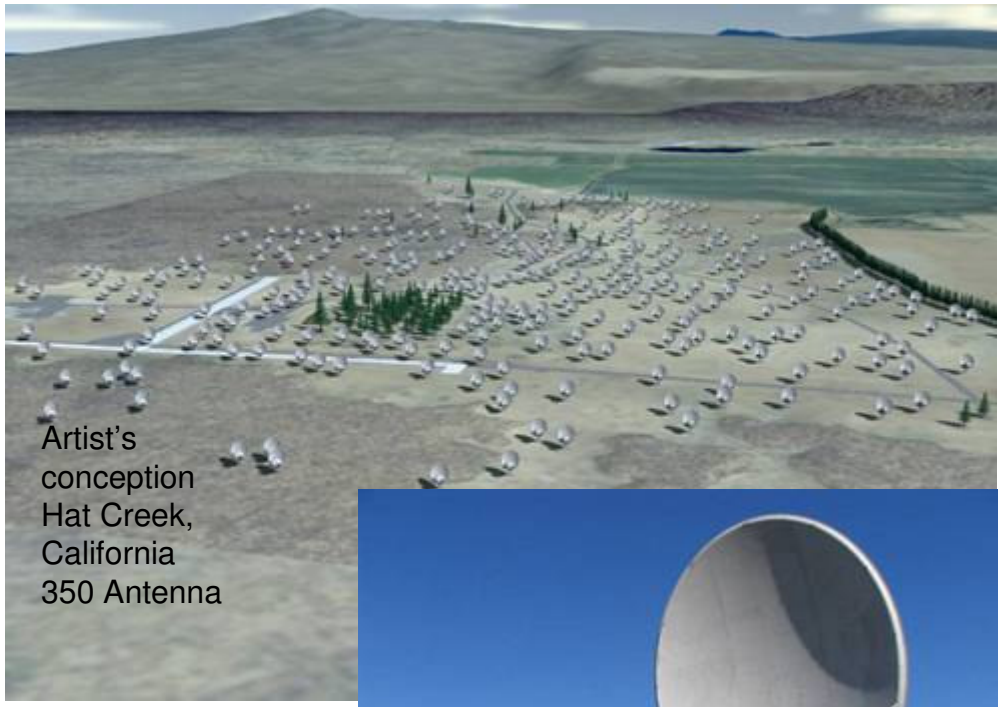
JPL/SETI Galactic Plane Sky Survey

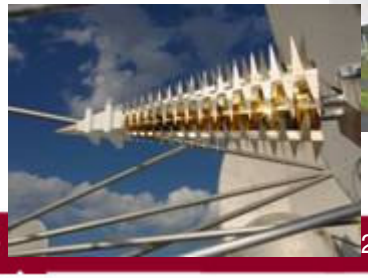






16-Antenna Correlator at Allen Telescope Array





RAMP/ BEE3 Preview

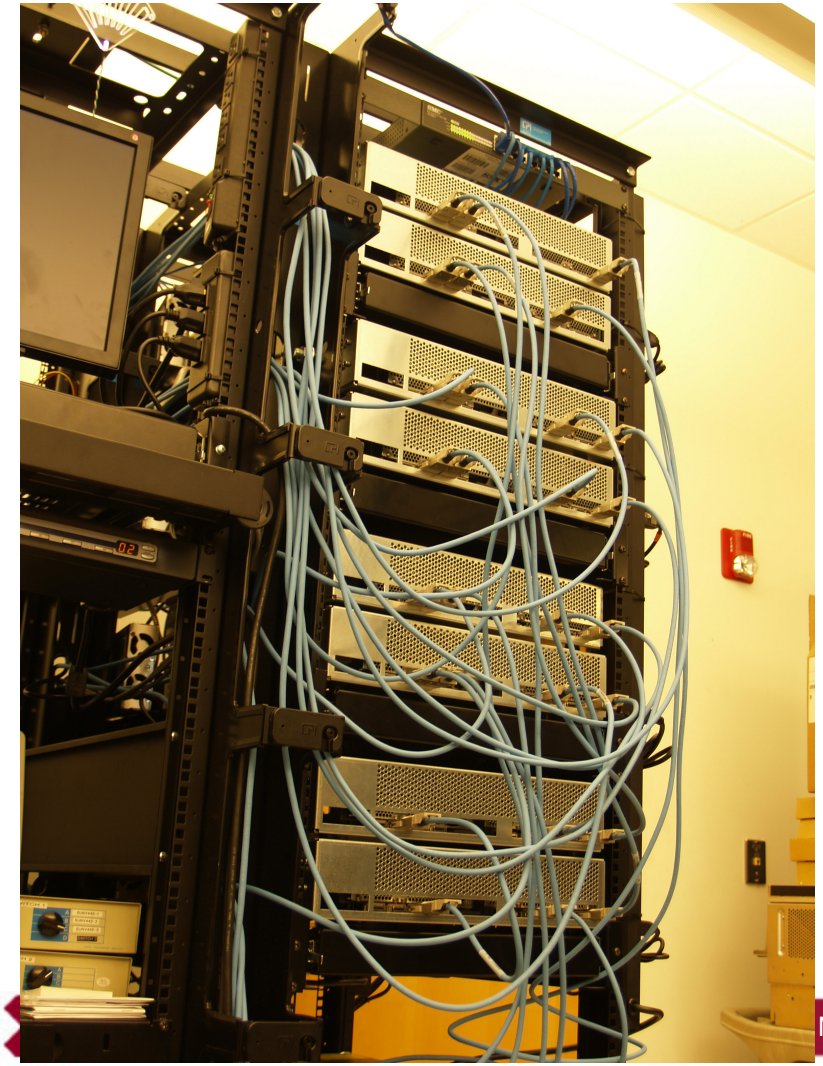
Research Accelerator for Multiple Processors

David Patterson (Berkeley, CO-PI), Arvind (MIT), Krste Asanovíc (MIT), Derek Chiou (Texas), James Hoe(CMU), Christos Kozyrakis(Stanford), Shih-Lien Lu (Intel), Mark Oskin (Washington), Jan Rabaey (Berkeley), and John Wawrzynek (Berkeley-PI)

Microsoft

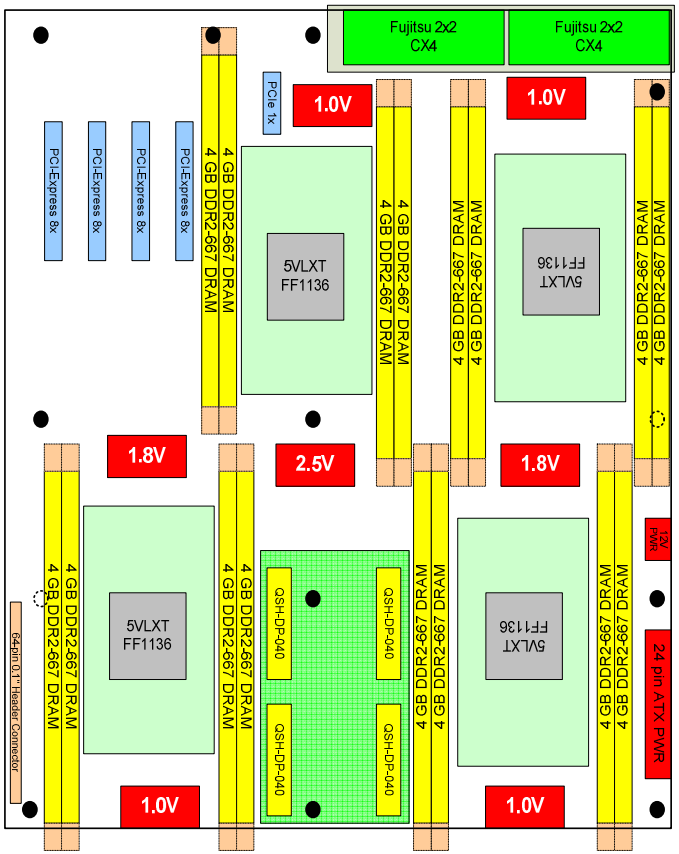
Power.org™

RAMP Blue Prototype (1/07)



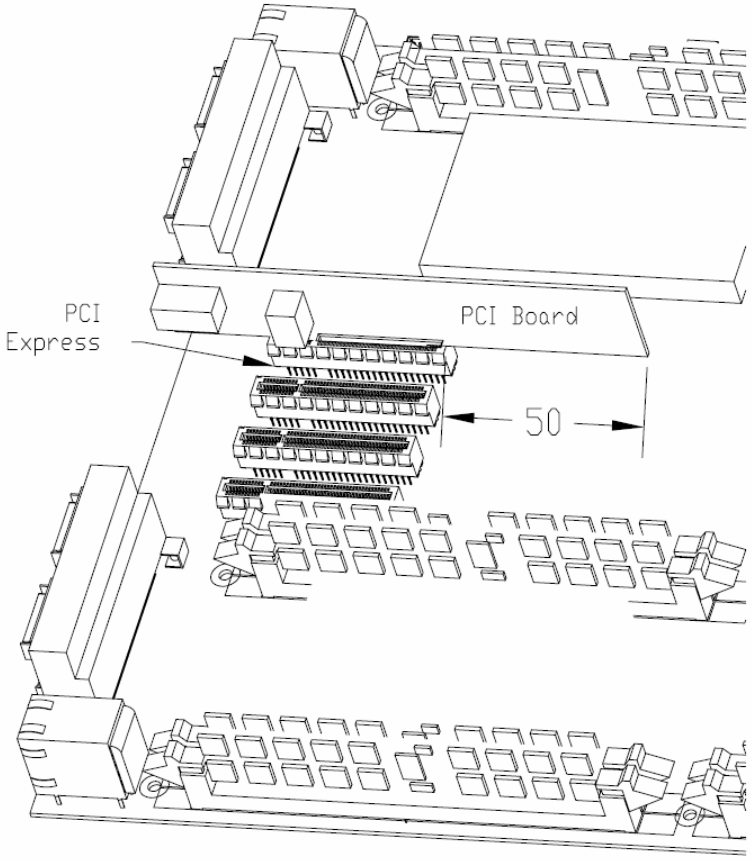
- 8 MicroBlaze cores / FPGA
- 8 BEE2 modules (32 “user” FPGAs) x 4 FPGAs/module = 256 cores @ 100MHz
- Full star-connection between modules
- It works; runs NAS benchmarks
- CPUs are softcore MicroBlazes (32-bit Xilinx RISC architecture)

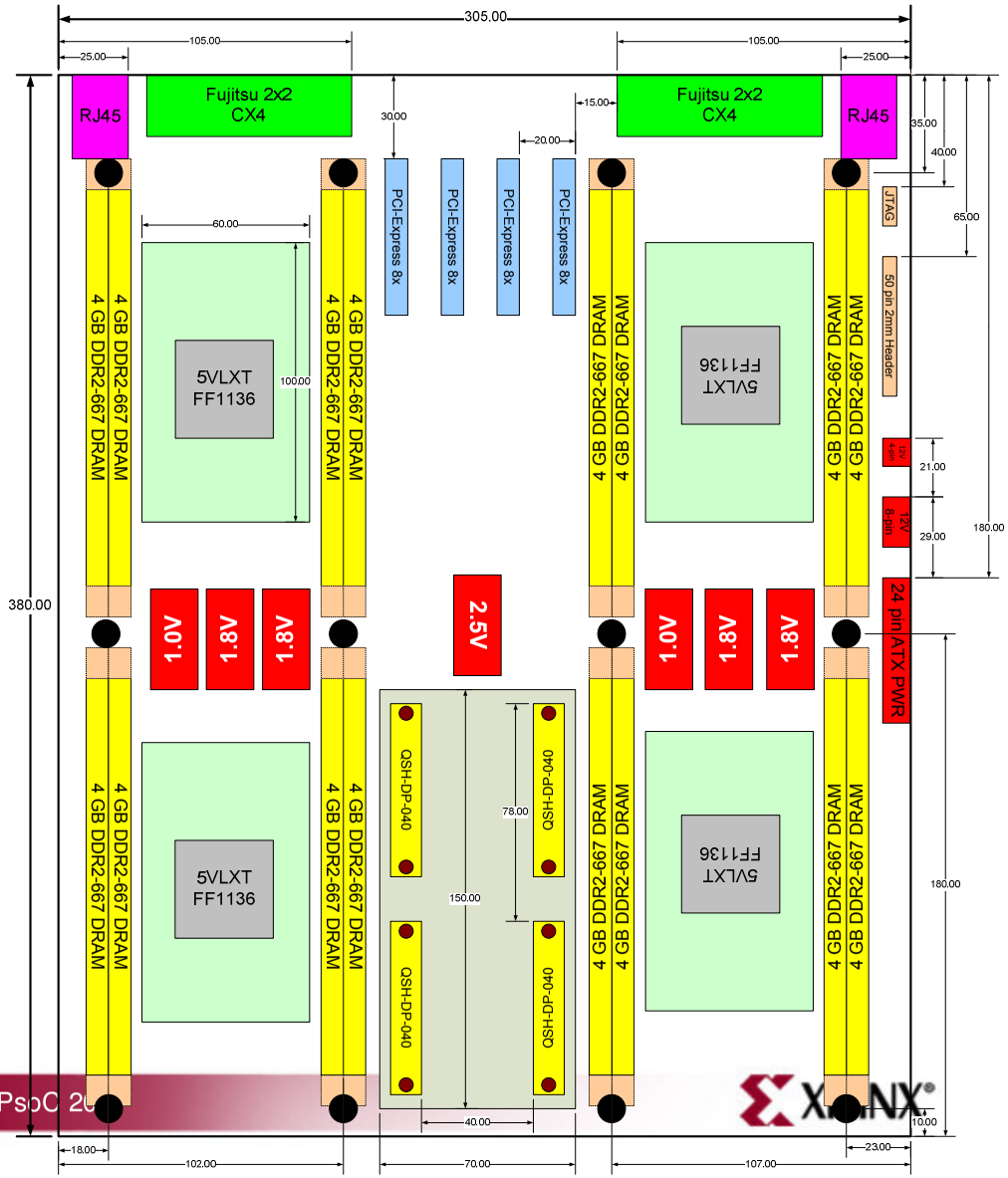
BEE3 Conceptual Overview



- 4 FPGA:
  - Virtex-5 LX110T (FF1136)
- 16 DIMMs
  - DDR2-667/800
  - Up to 16GB each
- 8 10GBase-CX4 interfaces
- EATX formfactor
- 2U chassis

BEE3 board and chassis





Conclusion

- Several layers of technology are used in signal processing systems.
- Control processors and Operating Systems are essential integration technology.
- Modern FPGAs support implementations with several processing subsystems, including several processors.
- Strategic University cooperation with multiple independent partners is a modern research community.
- The Xilinx University Program is here for you: www.xilinx.com/univ