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A Case Study in Reliability-Aware Design: A Resilient LDPC Decoder Architecture

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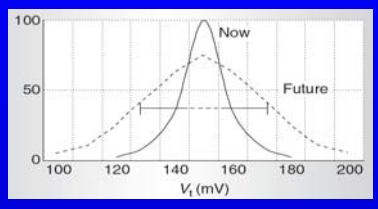
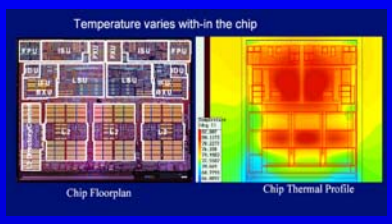
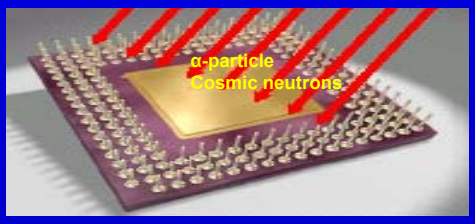
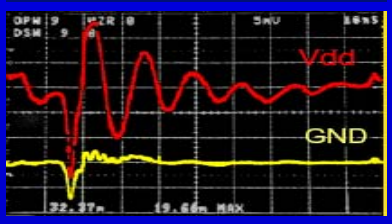
Motivation

- Extreme static & dynamic variations will result in unreliable components
- How to build reliable systems with „physical layer“ ?
- Resilient architectures tolerating variabilty and sporadic errors







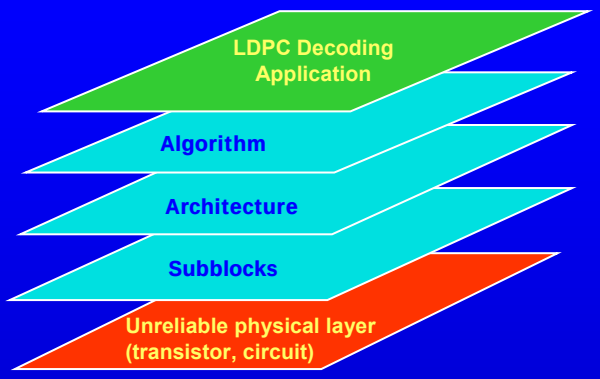


Case Study: LDPC Decoder

- Emerging Killer Applications
  - Recognition, Mining, Synthesis (RMS)
  - Probabilistic belief propagation algorithms
- LDPC decoding representative for RMS algorithms
  - Hot topic in wireless communications (WiMAX, DVB-S2, WiFi, space applications)
  - High troughput, low latency requirements, large flexibility
- Communication and memory centric architecture
- Sources of unreliability
  - E.g. timing errors in communication network due to cross talk and voltage noise
  - E.g. soft errors in memories and communication network

Goal: Increase LDPC decoder reliability for a given system performance with minimum hardware overhead and throughput degradation

Error Resilient LDPC Decoder



- Large design space for resilient architectures
  - Spatial- and time redundancy e.g. TRM (space), ARQ (time)
  - Error detection/correction codes e.g. CRC, Hamming codes
- Application resilience (probabilistic & iterative)

Algorithm/Architecture/EDC Codesign

- ALGORITHM: investigation w.r.t. fault-tolerance, error sensitivity e.g.
  - Single/two phase belief propagation, layered belief propagation algorithms
  - Sum-Product, 3-min, Min-Sum
- ARCHITECTURE: select robust architecture e.g.
  - Single-Phase, Two-Phase
  - Sign-magnitude, 2K
  - Critical signals
- SUBBLOCK: identify „reliability sensitivity“ for each subblock
  - Select appropriate technique for each subblock to increase SYSTEM reliability

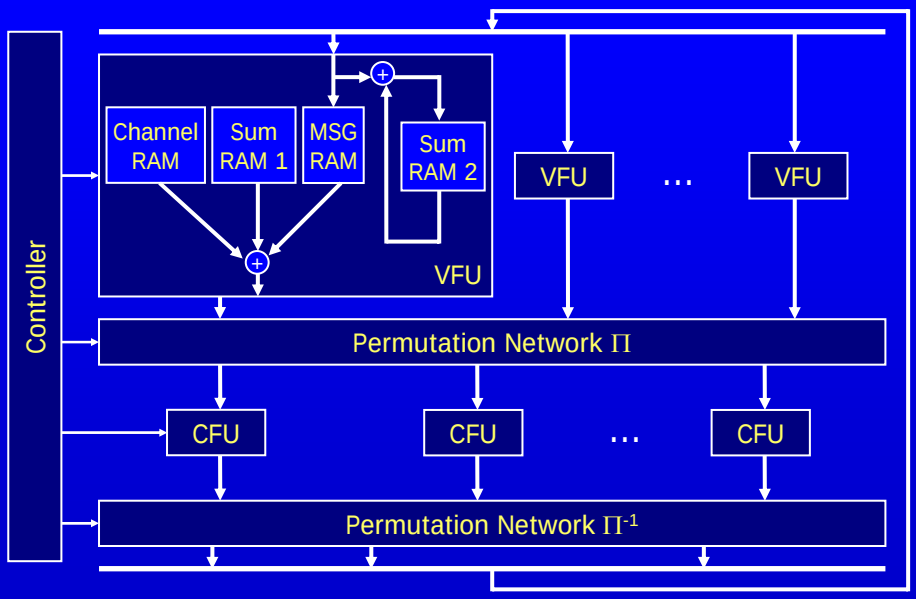
All steps are strongly interrelated!

UKL LDPC Decoder Implementations

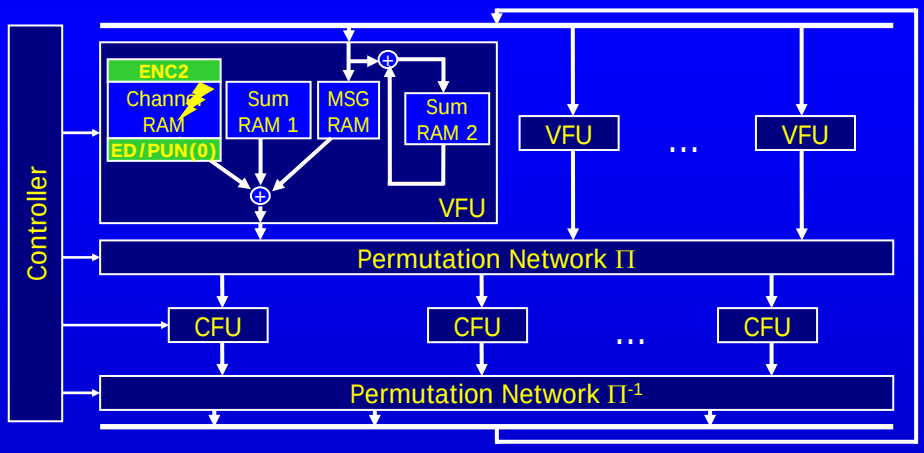
LDPC Code	DVB-S2		WiMax (802.16e)	WiFi (802.11n)	U-S LDPC (UWB)
Codeword Size	64800		576-2304	648, 1296, 1944	9600
Code Rate	1/4-9/10		1/2-5/6	1/2-5/6	3/4
Parallelism	90	360	24-96	27-81	80
Quantization	6 bit				
Algorithm	3-Min				MinSum+MSF/Lay.
Max. Iterations	50-15		25-20	25-20	7
Architecture	1-phase	PN branch	Combined	1-phase	Layered
Area [mm²] 65nm @ 400 MHz					@ 528 MHz
VNP	0.130	0.217	0.110	0.096	0
CNP	0.328	1.200	0.470	0.395	0.212
Network	0.046	0.270	0.206	0.065	0.027
Memory	3.357	4.428	0.551	0.467	0.265
Overall Area	3.86	6.11	1.33	1.02	0.50
Net Throughput	60-708 Mbps	0.23-2.68 Gbps	48-333 Mbps	54-281 Mbps	1.63 Gbps
Latency	270-82 µs	69-21 µs	6.0-5.7 µs	6.0-5.8 µs	4.4 µs
Max. Efficiency	183 Mbps / mm²	430 Mbps / mm²	250 Mbps / mm²	274 Mbps / mm²	3.2 Gbps / mm²
Infobit/Cycle	0.15-1.77	0.58-6.70	0.12-0.83	0.14-0.70	3.08

- Selected WiMax Standard as case study

Single-Phase 3-Min Algorithm

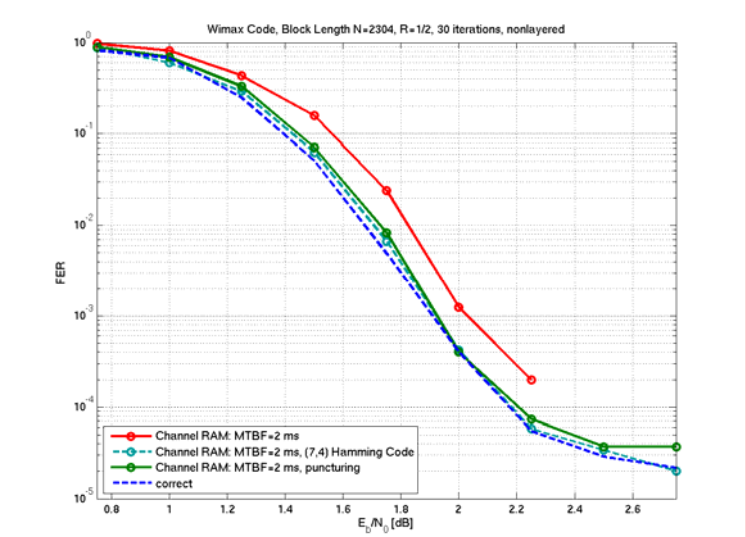


Soft Errors in Memories



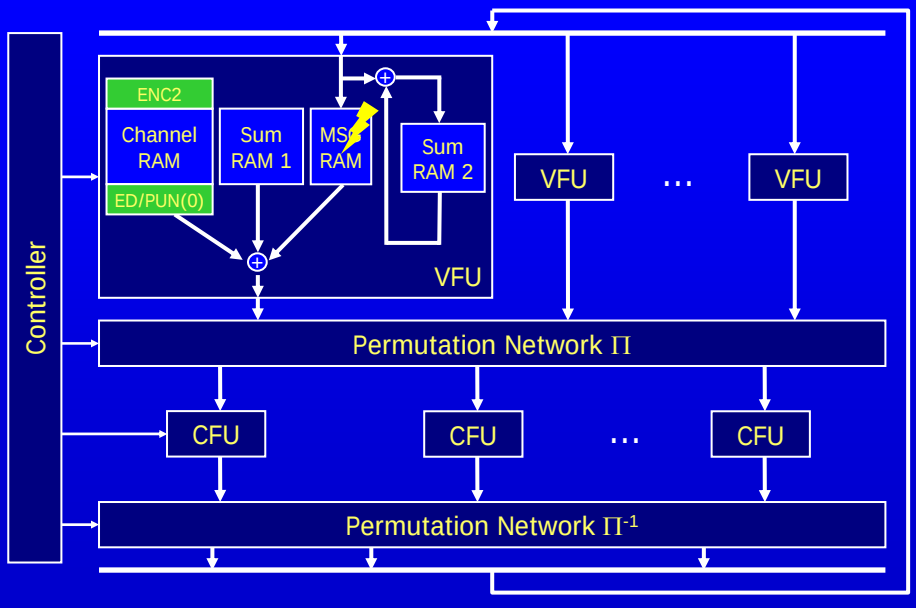
- Encoding (ENC2): MSB of channel values doubled
- Error detection: Comparison of the MSB
- Error correction: Puncturing i.e. channel values are set to 0 (algorithmic fault tol.)

Channel RAM

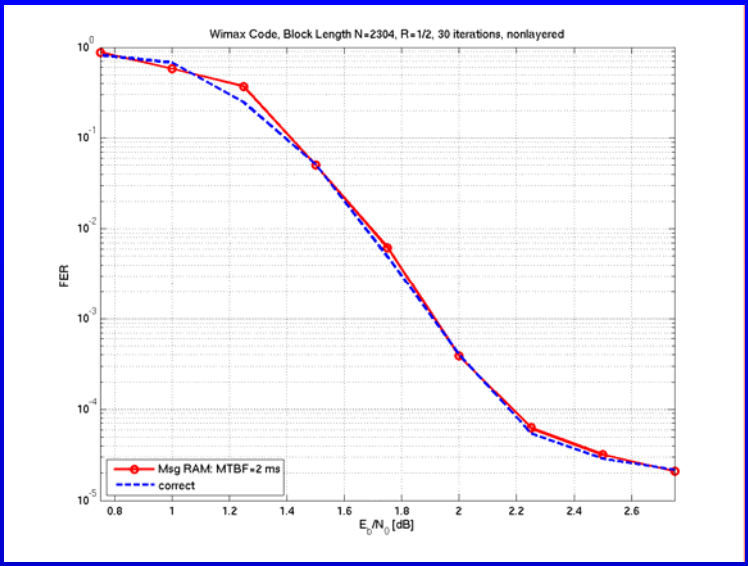


MTBF (bit flipping) = 2ms = 10^{15} FIT

Message RAM

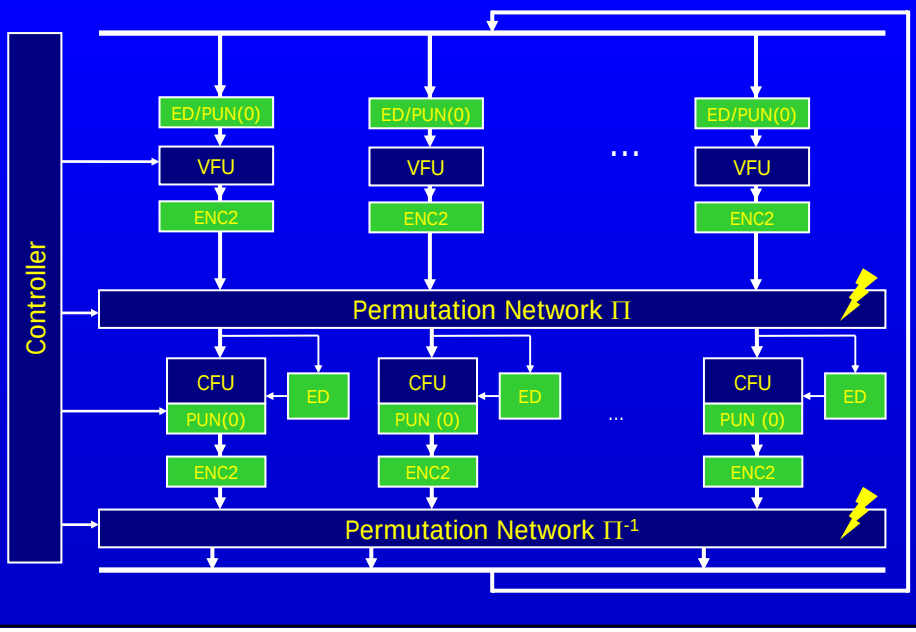


Message RAM



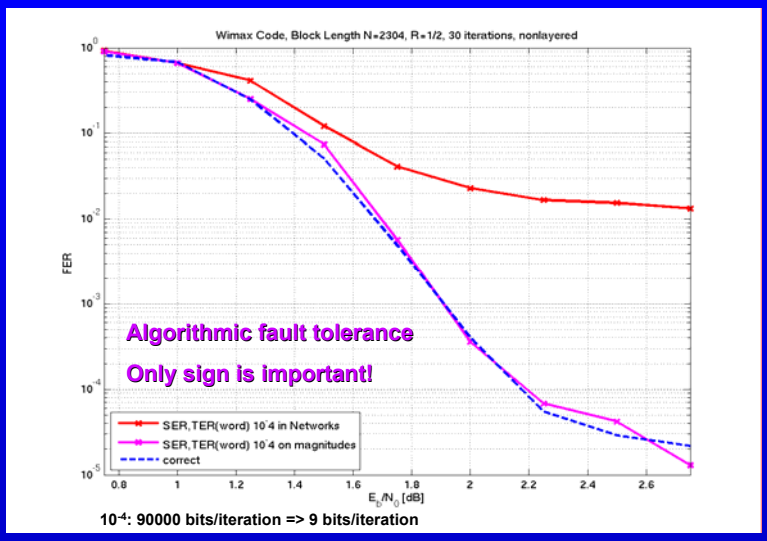
- Inherent fault tolerance of the belief propagation algorithm

Permutation Network: Soft and Timing Errors



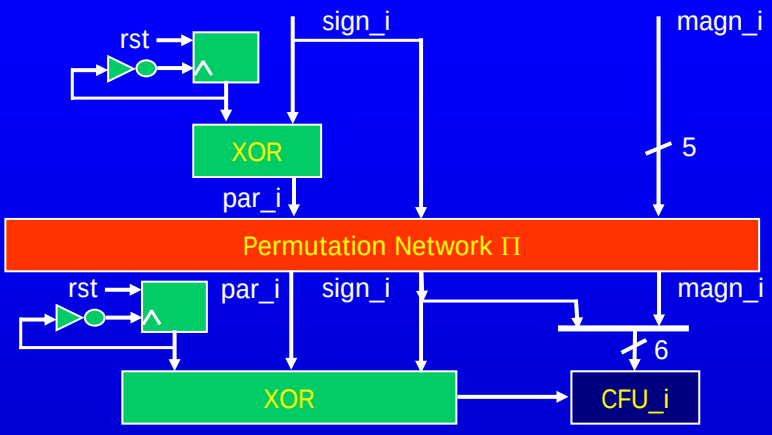
Data Representation

- K2 versus Sign/Magnitude: Sign/Magnitude reduces power and noise



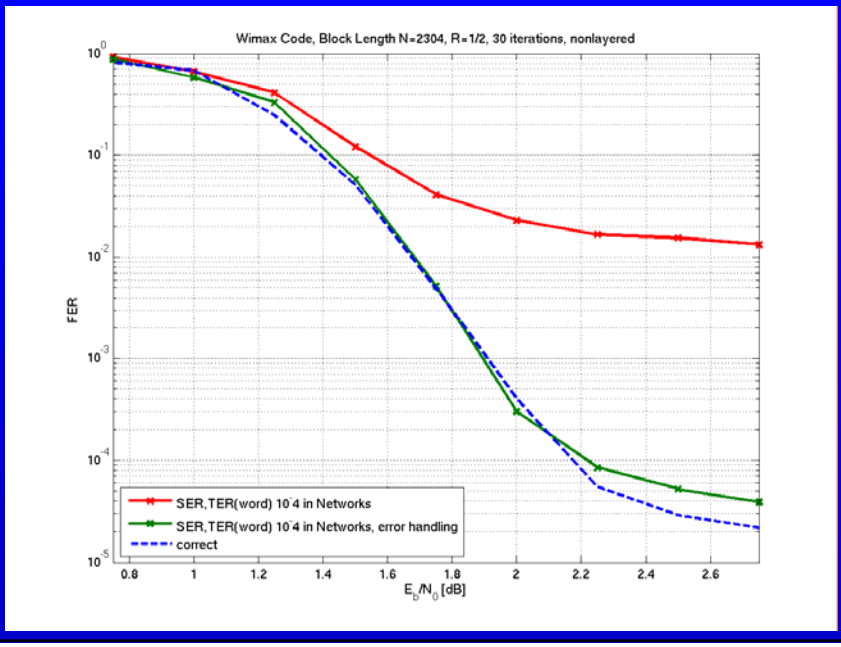
10^{-4}: 90000 bits/iteration => 9 bits/iteration

Permutation Networks

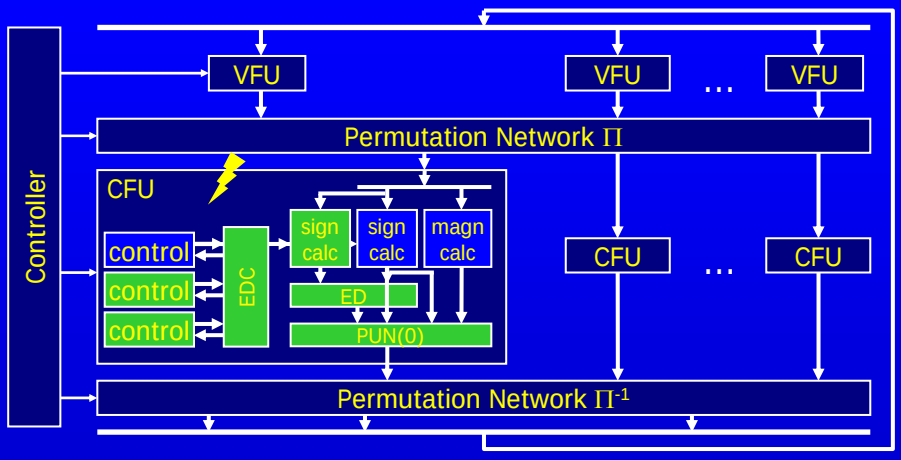


- Encoding
  - Sign bit doubled, toggle redundant sign every clock cycle (timing errors)
- Error detection and correction
  - Error in input message: all output messages of this check node are set to 0

Permutation Networks

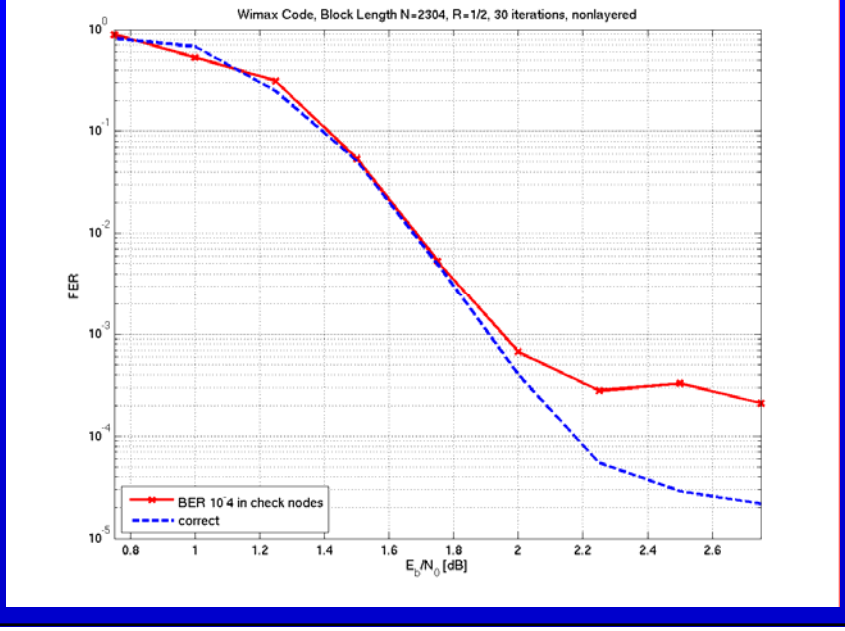


Check Nodes

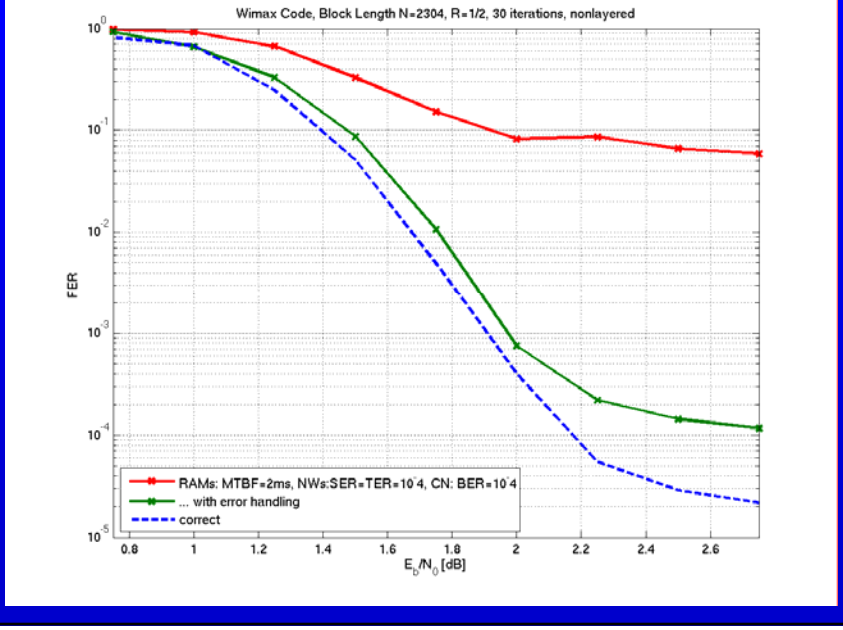


- **Encoding: sign calculation doubled / controller tripled**
- **Error correction**
  - Message puncturing: reuse PUN unit of errors in permutation network
  - Controller: 2 out of 3 voter

Check Nodes



Putting all together



Overhead ~20 %

- WiMAX LDPC code decoder, parallelism degree 96
- Synthesis with 65 nm standard cell library @ 400 MHz

Unit	LDPC Decoder	Resilient LDPC Decoder
Controller (including address and permutation ROM)	0.03	0.09
VFUs (without RAM)	0.11	0.11
CFUs	0.43	0.55
Permutation Networks	0.21	0.25
Sum RAM	0.21	0.25
Channel RAM	0.07	0.09
Message RAM	0.25	0.25
Total Area [mm^2]	1.31	1.59

Conclusion

- Continous CMOS scaling
  - Resilient architectures become mandatory
- Increase of system reliabilty
  - All levels of abstraction have to be considered
  - Application has to be understood
- Algorithm/Architecture/EDC Codesign
  - Wirless communication is a good example