Technological Trends, Design Constraints and some Implementation Challenges in Mobile Phone Platforms

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The year 2009:

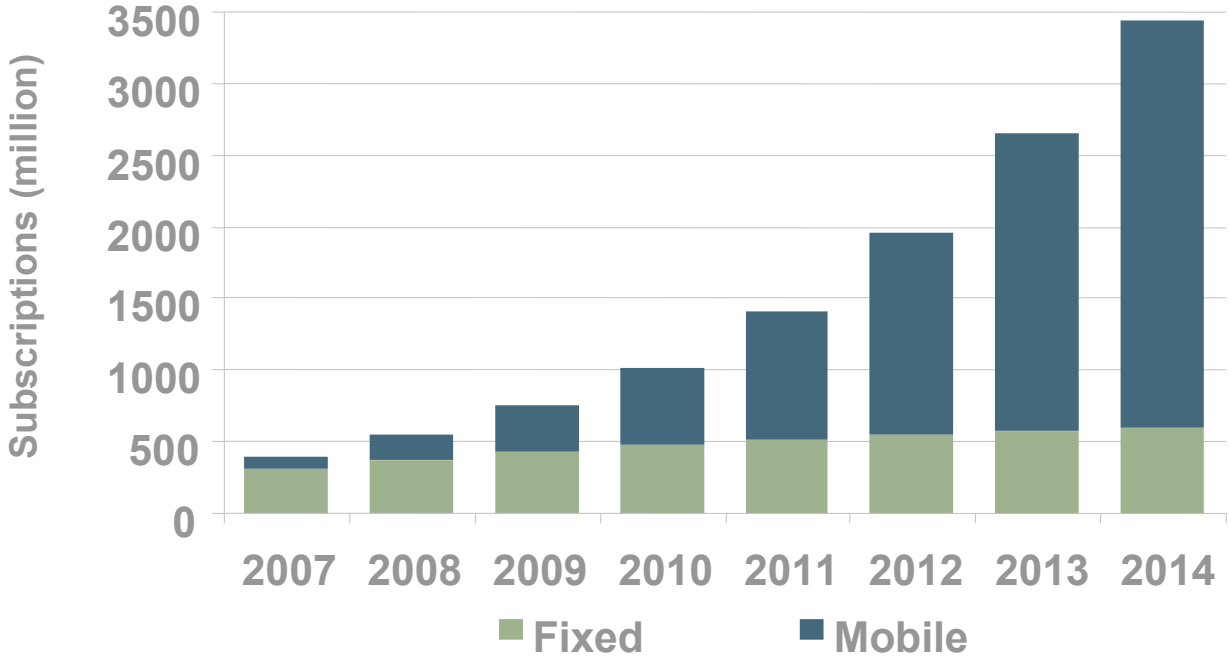
4 billion mobile phone subscriptions
1 billion new phones every year

…but there are only 1 billion bank accounts

The mobile phone is a pretty popular device

Economy of scale:
- BOM-centric cost
- Price pressure

Broadband Goes Mobile



80%
of Broadband subscribers are mobile in 2014

Mobile Broadband includes: CDMA2000 EV-DO, HSPA, LTE, Mobile WiMAX, TD-SCDMA
Fixed broadband includes: DSL, FTTx, Cable modem, Enterprise leased lines and Wireless Broadband

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A New Global Leader in Wireless Technologies

A Joint Venture owned equally by STMicroelectronics and

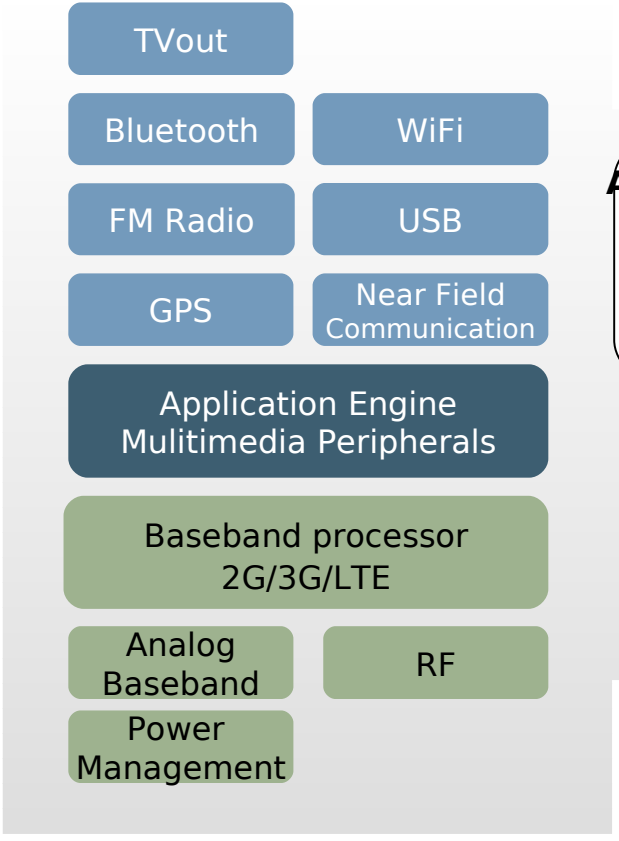
Leadership positions in our entire platform portfolio

- #1 in EDGE
- #2 in 3G
- Top 3 in GSM/GPRS

Leadership positions in wireless components

- #1 in RF from GSM to 3G
- #1 in Power Management and Analog Baseband
- Top 3 in Connectivity and Broadcast for mobile

COMPLETE OFFER



Application Frameworks & OS

Customer Frameworks

symbian

android

Windows Mobile

- Silicon Integration
- SW Integration
- Validation and Testing
- IOT and Field Testing
- Reference Designs

Modems For Connected Devices

Smartphone Platforms

Feature Phone Platforms

Entry Phone Platforms

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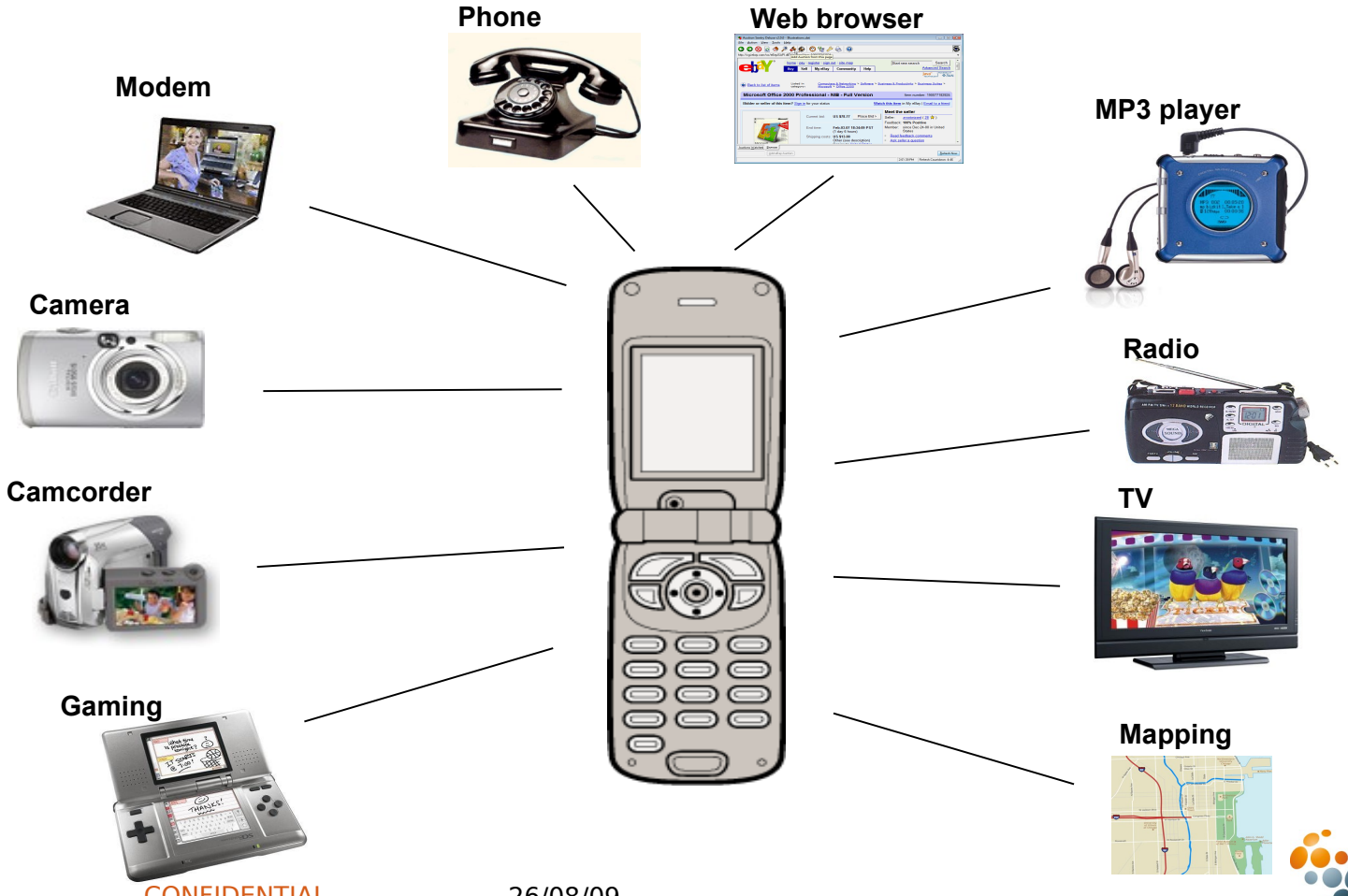
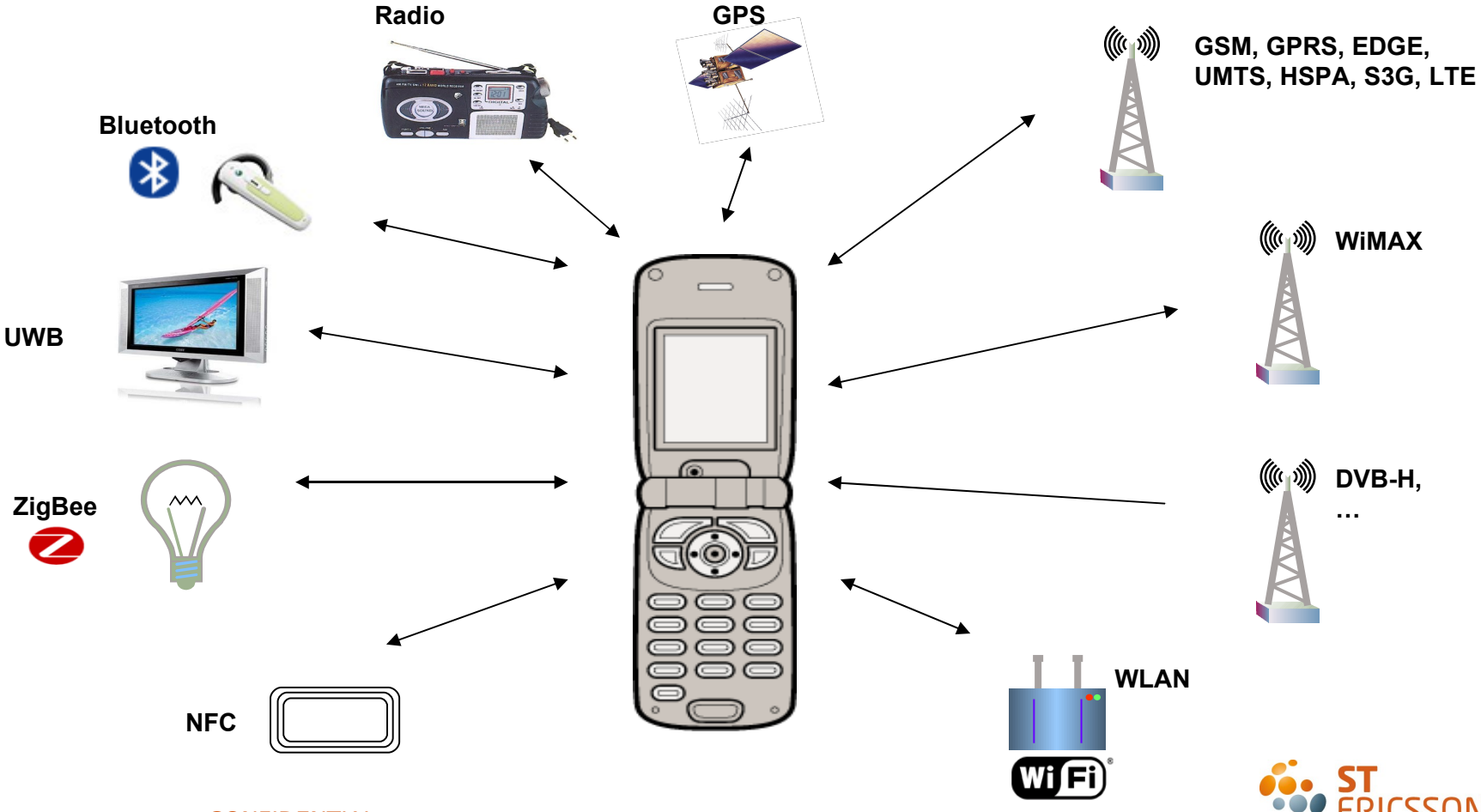
Use Case Perspective

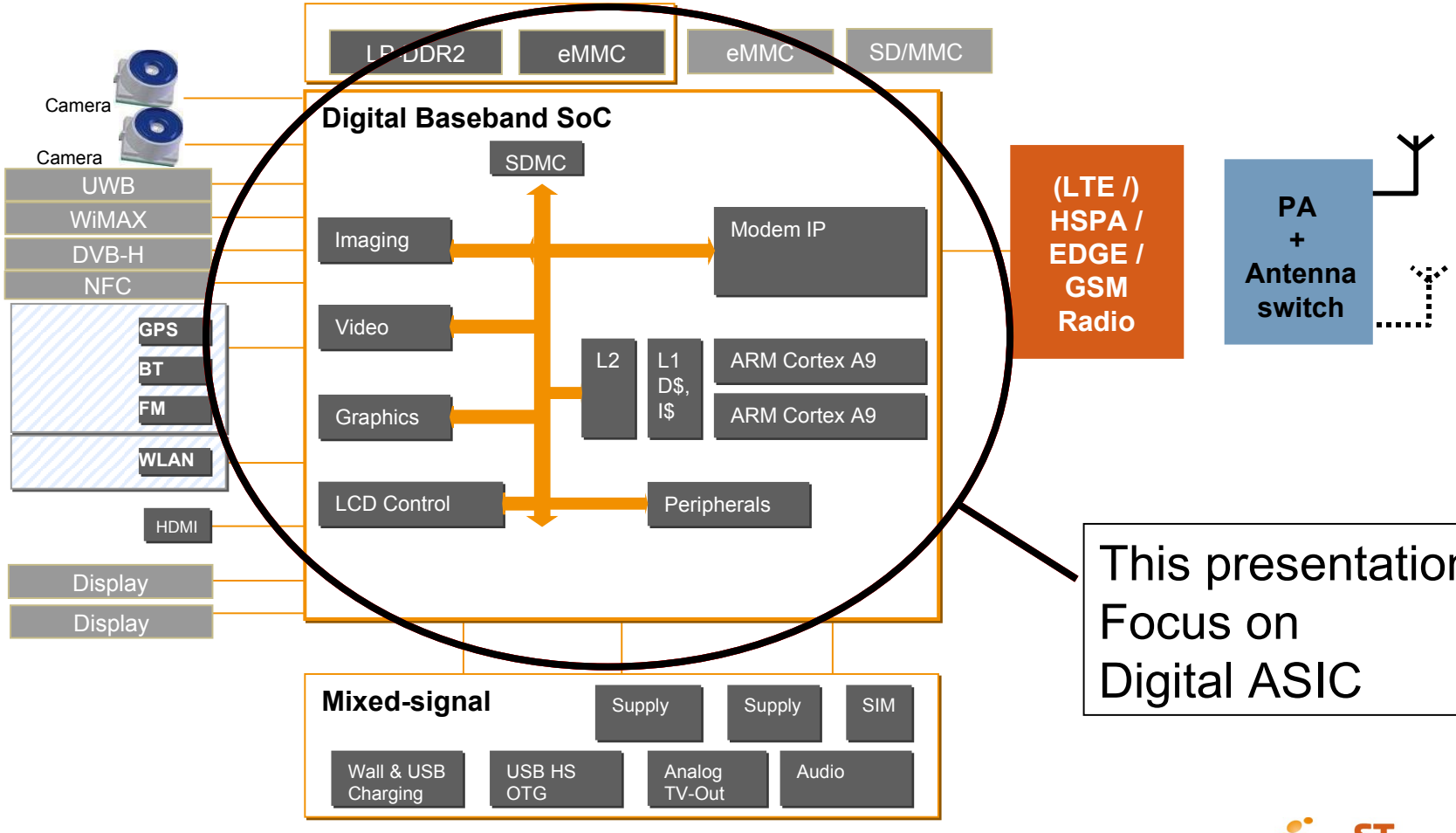


Multi-Standard Terminal of the Future



High-level Block Diagram

Block diagram showing U8500 –
see Er-Rachidi, Fraisse, Darbel MPSoC 2009



This presentation:
Focus on
Digital ASIC

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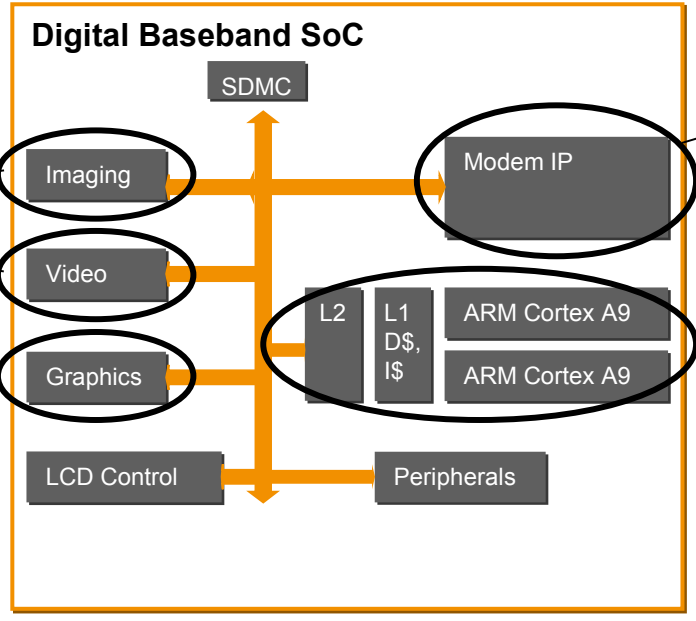
Many Processing Subsystems in Baseband SoC



Video and Imaging:
Careful balance between hardware vs. embedded cores for cost vs. flexibility

Graphics:
Massive dedicated processing needs. Multiple pipelines

Modem subsystem:
Multiple cores + internal memory

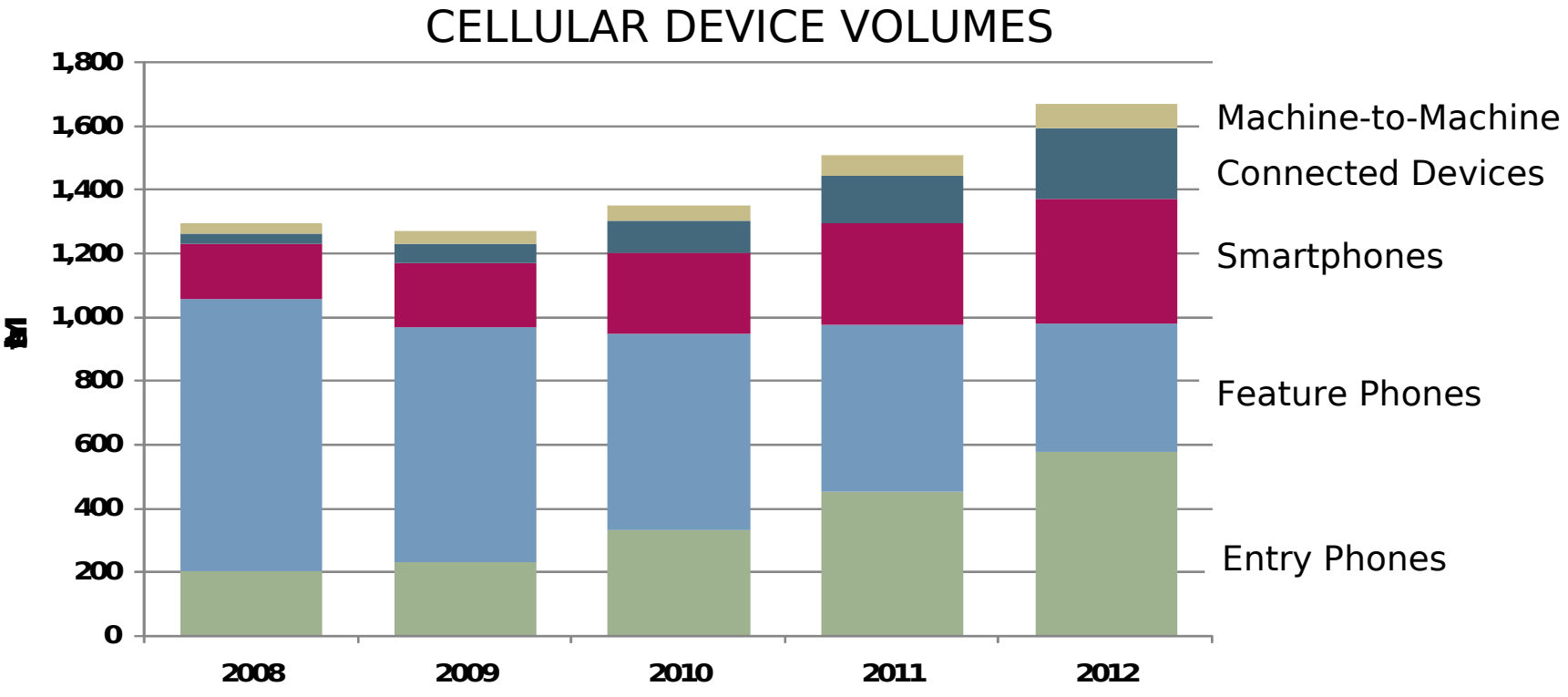
Application CPU:
Already in U8500 a dual-core SMP

Design Constraints: “THE HOLY FOUR”

Performance	Cost	Power Consumption	Size

As with any electronic device…

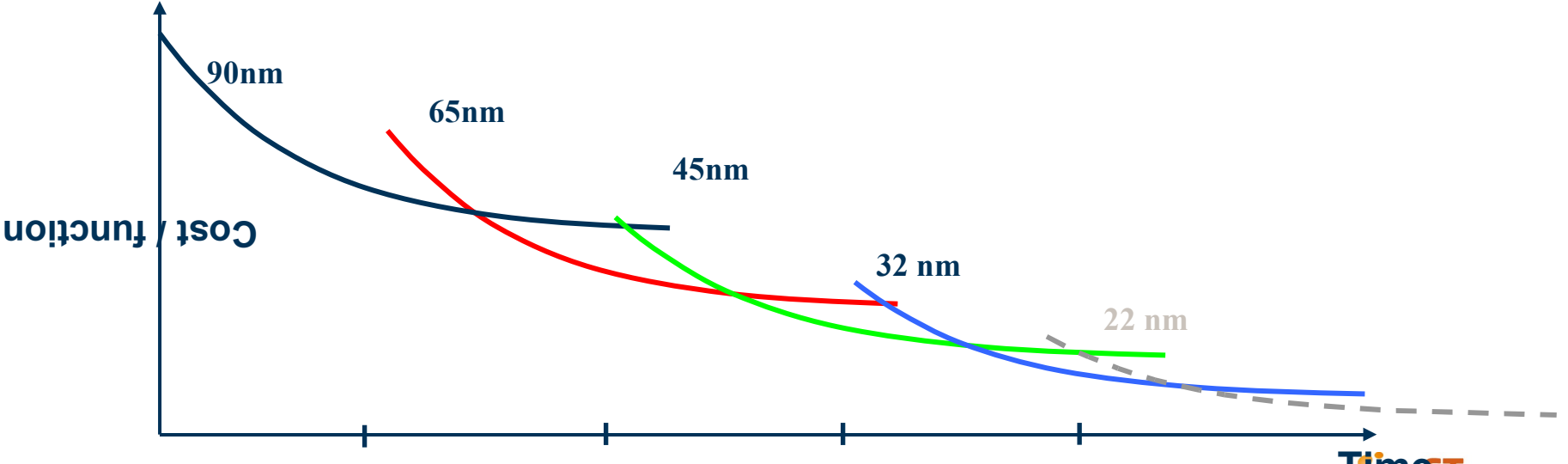
MARKET – SEGMENTS



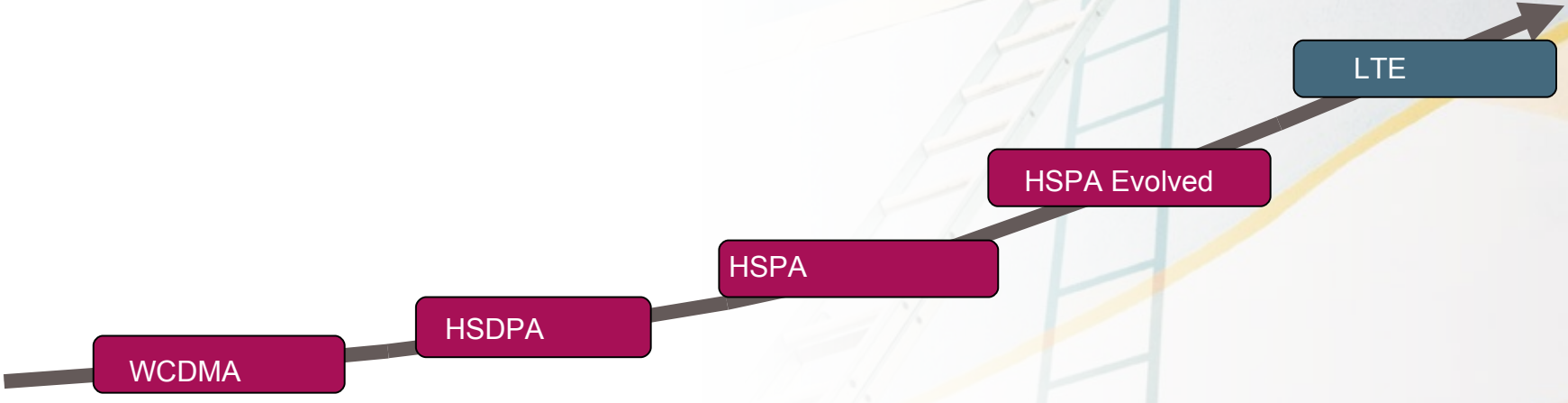
Source: ABI Research 3Q08-4Q08

Design Constraints: Silicon Area

- Overall platform cost: very dependent on silicon size and package
  - Volume is tens of millions
  - No room for un-used flexibility
  - Business case for latest Si-geometries
  - Tradeoff depends on Digital vs. Analog content, level of integration, packaging techniques, and partitioning between ASICs



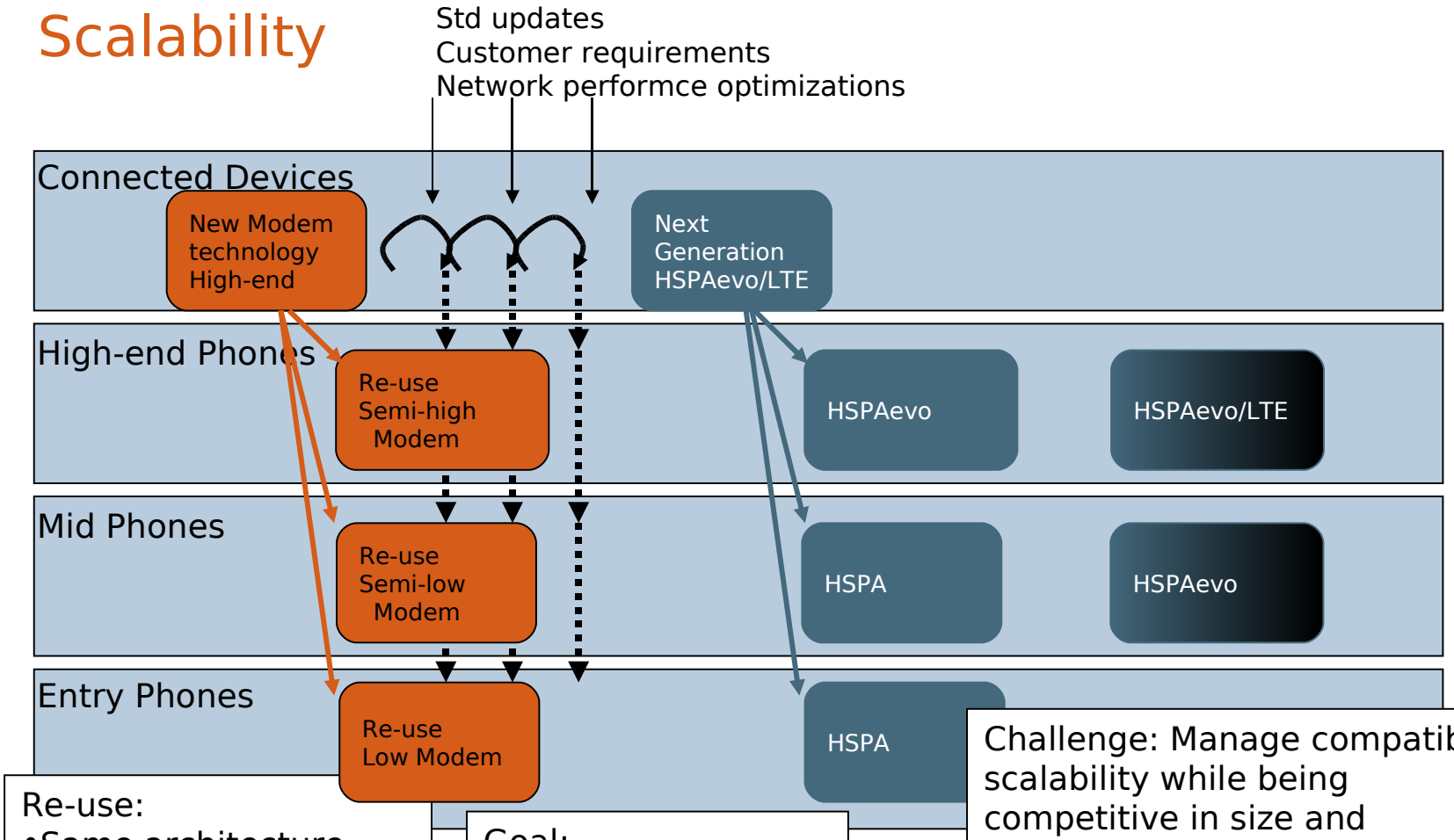
Cellular Technology Evolution



3GPP	R99/1999	R5/2002	R6/2005	R7/2007	R8/2008
Peak rate DL	0.38	14	14	40	100 in 20MHz
Peak rate UL	0.38	0.38	5.7	11	50 in 20MHz
Handset Market	2001-2002	2006	2007	2009	2010 (launch)

~100x higher peak rate in 5 years

Scalability



Re-use:
- Same architecture
- SW compatible
- Different configuration

Goal:
- High R&D efficiency
- High IOT re-use

Challenge: Manage compatible scalability while being competitive in size and performance

Cellular Processing: Architectural trade-offs

- Software solutions bring flexibility, but
  - Silicon-size
  - Power consumption
- Examples of tasks that are computationally very intensive
  and are implemented in accelerators:
  - Turbo Decoder
    - HSDPA 7.2 Mbps 3.5 GOPS
    - HSPAevo 42 Mbps 20 GOPS
    - LTE 100 Mbps 48 GOPS
  - HSPA Advanced Rake
  - LTE Interference Cancellation
- Minimum no. instructions/operations per transmitted symbol
  - Different HW/SW trade-off for GSM vs. WCDMA vs. LTE
  - Demanding real-time requirements
- Architectural approach (see right)
  - Based on ST-Ericssons vast experience and cellular expertise

Higher levels of stack, multi-access:
•Processing in CPU (one or multi)

Processing intensive but required flexibility:
•Highly-efficient Vector-DSP (one or multi)
- ST-Ericsson IP, very efficient for cellular
- Multi-standard, multi-purpose
- Advanced and mature tool-chain

Parts of Physical layer:
•E.g. Turbo –decoding
•Special-purpose IP blocks
•Efficient data-flow
•Efficient memory utilization

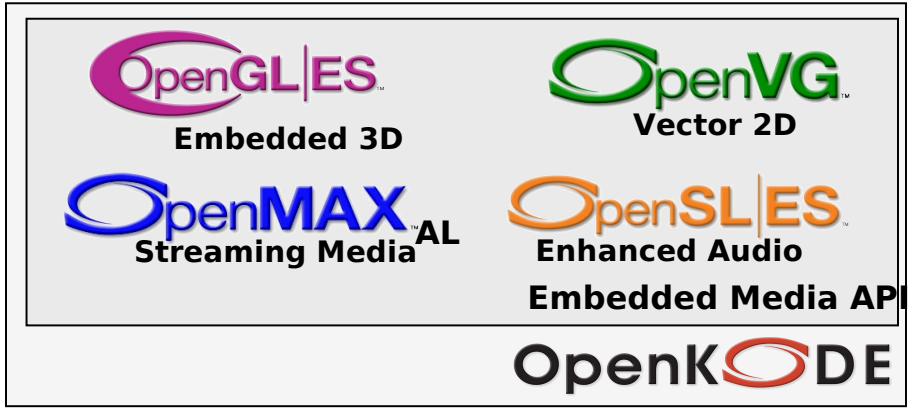
Application Software Trends

Applications:

- PC-Mobile SW platform convergence is accelerating.
- Open OS: Android, Symbian, ...
- The Web runtime is becoming the universal “cross-platform” runtime.
- Powerful eco-systems

Multimedia:

- Compete with dedicated devices:
  - Cameras, camcorders, media players
- Excellent user interfaces
- Needs from SW platform convergence
  - Browser, Application frameworks
- Open API’s: Separate implementation from application usage



Applications and Multimedia Processing

CPU vs. dedicated subsystems (e.g. HW accelerators)?

- Processing density (performance vs. area) for specific functions
- Power consumption
- Flexibility, Use Case concurrency

Dedicated subsystems: how specialized?

- Tailored cores vs. hard-coded accelerators?

When must we peak performance?

Use Case driven analysis for peak performance and thermal analyses.

Examples:

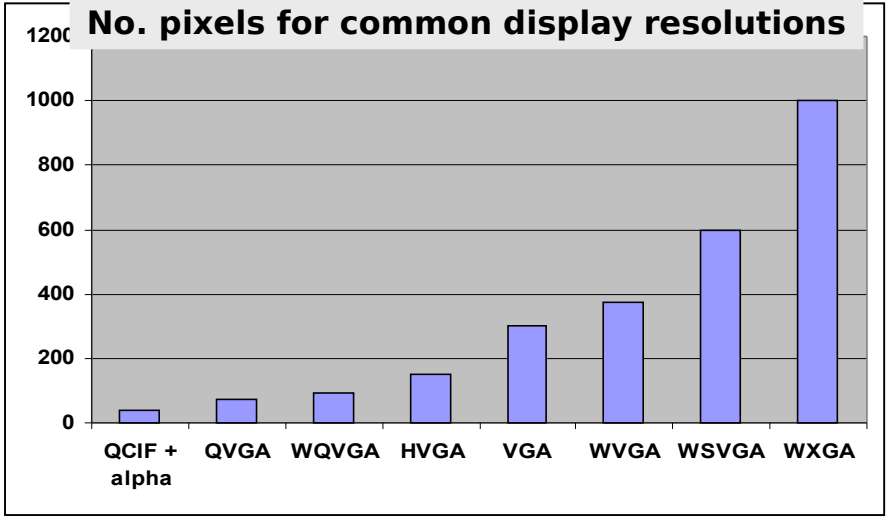
- Play Game
  1. Graphics (3D), potentially Video
  2. Game engine / Java / Browser
  3. Multi-channel Audio
  4. Network signaling & datacom
  5. Potentially VoIP over HSPA
- Video Camcorder
  1. Video encode
  2. Audio encoding
  3. Viewfinder
  4. Graphics overlay

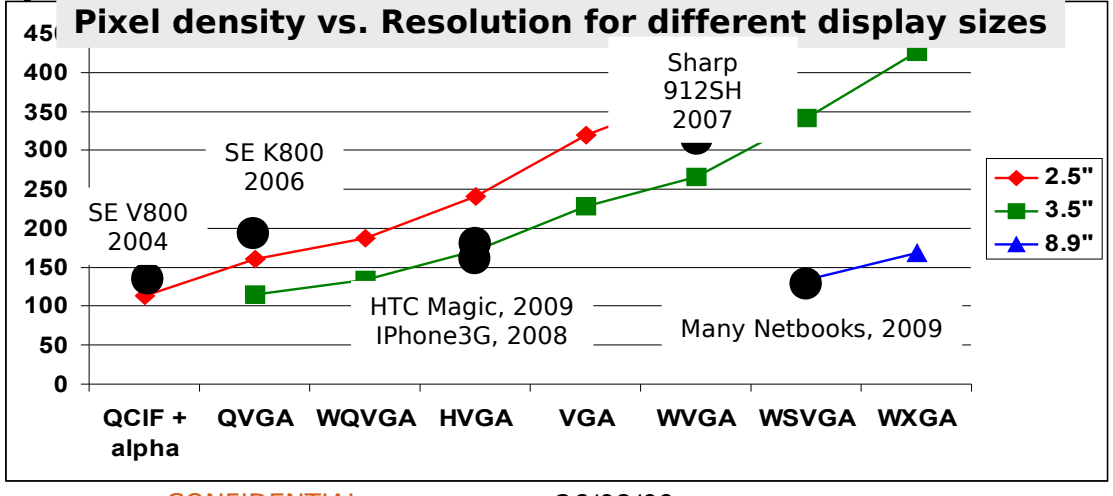
Parallelism Required (all use cases):
- Multi-display: external + internal
- External display: 1080P requirements emerging
- Rotation of display & overlays
- Multi-tasking, multi-frame, touch UI
- Data download/upload with anything else

Some traditional constraints removed:
- Network bandwidth seldom limited
- Memory size (e.g. file system)

Handset Display Resolution drives Processing

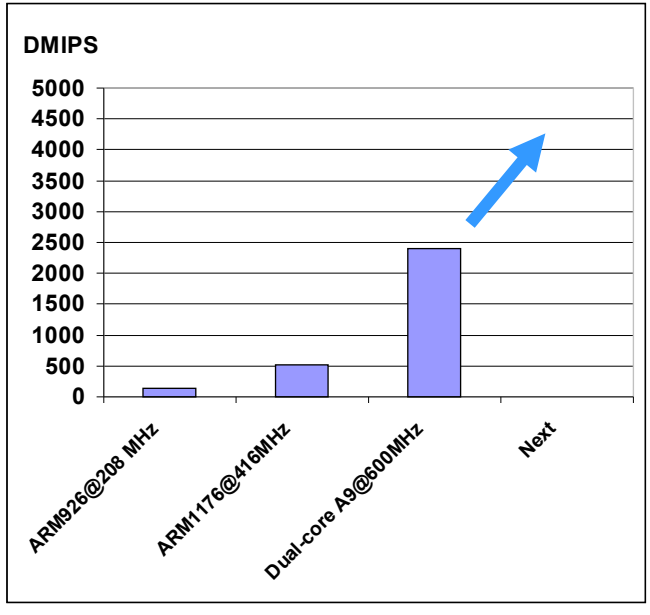
QCIF + alpha	220 x 176
QVGA	320 x 240
WQVGA	400 x 240
HVGA	480 x 320
VGA	640 x 480
WVGA	800 x 480
WSVGA	1024 x 600
WXGA	1280 x 800 (768)





Application Processor

- ST-Ericsson Phone SoC design: Integrated in same die
- Trend: processing behavior increasingly similar to desktop/laptops
  - But much of multimedia handled by dedicated subsystems
- SMP – Symmetric Multiprocessor emerging with U8500
  - Samples Spring 2009
  - Dual-core Cortex A9, 600 MHz,
    Neon SIMD extensions
- Scalability:
  - SMP:s will rapidly go down in segments
  - Lowest segments still single-core
- Next generation: x2 effective performance



Architectural Challenges:

- Software efficiency on SMP – especially towards quad-core
- Memory system and latency

Video

- Camcorder: Resolution
  - Resolution race up to 1080P
  - Frame-rate race at 1080P: from 30 fps to at least 60 fps
  - A few key encoding standards
- Streaming, Video clip, Movie
  - Many different formats, bit-rates, resolutions, and frame-rates
  - Resolution race up to 1080P for key codecs
  - Driven by content
- Challenge #1: Processing and Flexibility
  - Encoding very processing demanding
  - Processing density too low on CPUs
  - H.264 SD resolution demands 500MHz Cortex A8 or A9 with Neon
  - 1080P 30fps would demand ~6 times higher performance
  - Dedicated accelerators substantially smaller and lower power
  - Certain many-core solutions show promising processing density
- Challenge #2: Memory bandwidth
  - LP-DDR2 has substantially lower bandwidth than DDR3
  - Video memory traffic in worst-case use cases is memory bandwidth dimensioning
    - Worse than graphics
  - Dual memory interfaces – significant cost impact
  - Memory hierarchy and management imperative

32-b LP-DDR2 400MHz:
•Burst/Peak: 3.2GB/s

1080P 60fps
Video subsystem: 1-1.5GB/s
(Peaks get higher)
+ camera processing
+ overlays
+ applications

Graphics

- 2D and 3D graphics acceleration in all high-end phones today
- 3D accelerators for mobile platforms:
  - 100’s of Mpixel/s fill rate
  - 10’s of Mpolygons/s
  - Large and costly IP blocks
- GP-GPU:s to be introduced long-term
  - OpenCL software API

Architectural and Implementation Challenges

Platform architecture must be scalable to lower segments

- Software compatibility essential for R&D efficiency
- Families of IP blocks
- Critical: support software API:s impacting platform as well as application code
  - E.g. graphics

Memory system

- High impact on performance but also silicon area (= cost)
- Level-3 memory on-chip in higher segments
- Multimedia subsystems drives bandwidth but are often less sensitive to latency

GALS - Globally Asynchronous Locally Synchronous

- Many high-performance subsystem
- Solution to clock alignment and timing-closure complexity
- Impacts latency across asynchronous regions

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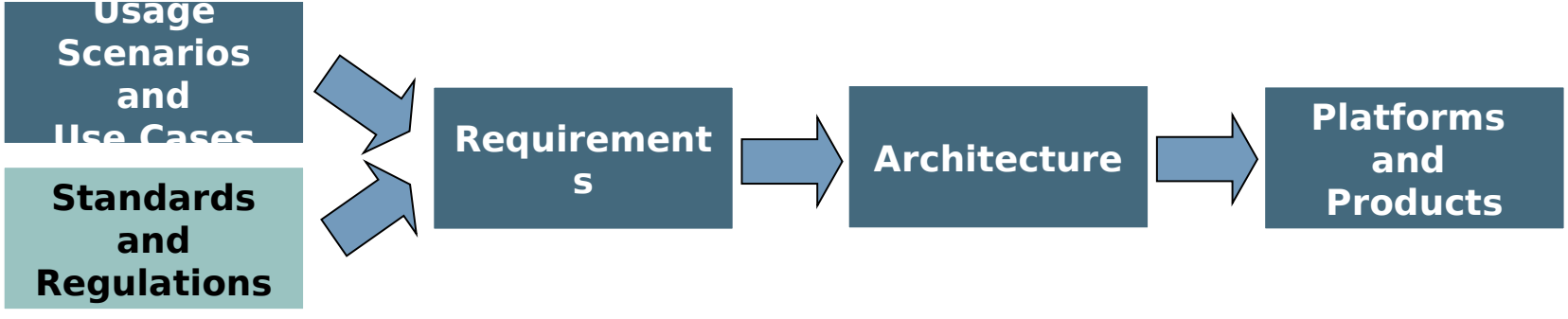
Other tradeoffs that set HW requirements

- Package size shall be small
  - Limits number of I/O:s
  - Package-on-package stacking of memories, constant packaging innovation

- Integration vs. Flexibility
- Standard interfaces
  - Cheaper components
- Power consumption
  - Standby, Voice call, Play music, Watch Video/TV
  - Compare phone with dedicated devices, e.g. mp3 players
  - Multiple power regions and voltage domains
- Heat
  - No fan, little space for heat dissipation
  - Thermal issues

Use Case Driven System Design

- More than just functionality
- A means to articulate requirements
- Usage Scenarios - Concurrency



Summary

- The internet is going wireless
- Mobile phones and PC:s are converging
- Multi-core SoC:s have been around for long time
  - Now SMP:s are emerging for application processing
  - Sub-systems increasingly multi-core
- Multimedia and Cellular:
  - Certain parts still benefit from the higher performance density and lower power consumption from hardware acceleration
- Some key challenges:
  - High demands on performance and programmability
    - Yet no margins for in-efficient silicon area
  - Scalability to low-cost segments with software compatibility
  - Efficient software for SMP
  - Power management and clocking integrity, yet high performance
  - Integration and packaging: both for high-end and low-cost platforms

LET'S
CREATE
IT

THANK YOU

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