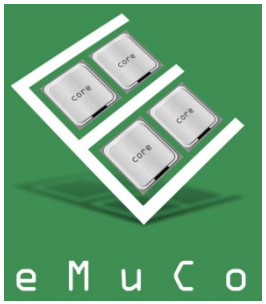

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Low-Power Leadership

MPSoC 2009

Targeted execution enabling increased power efficiency

Anirban Lahiri
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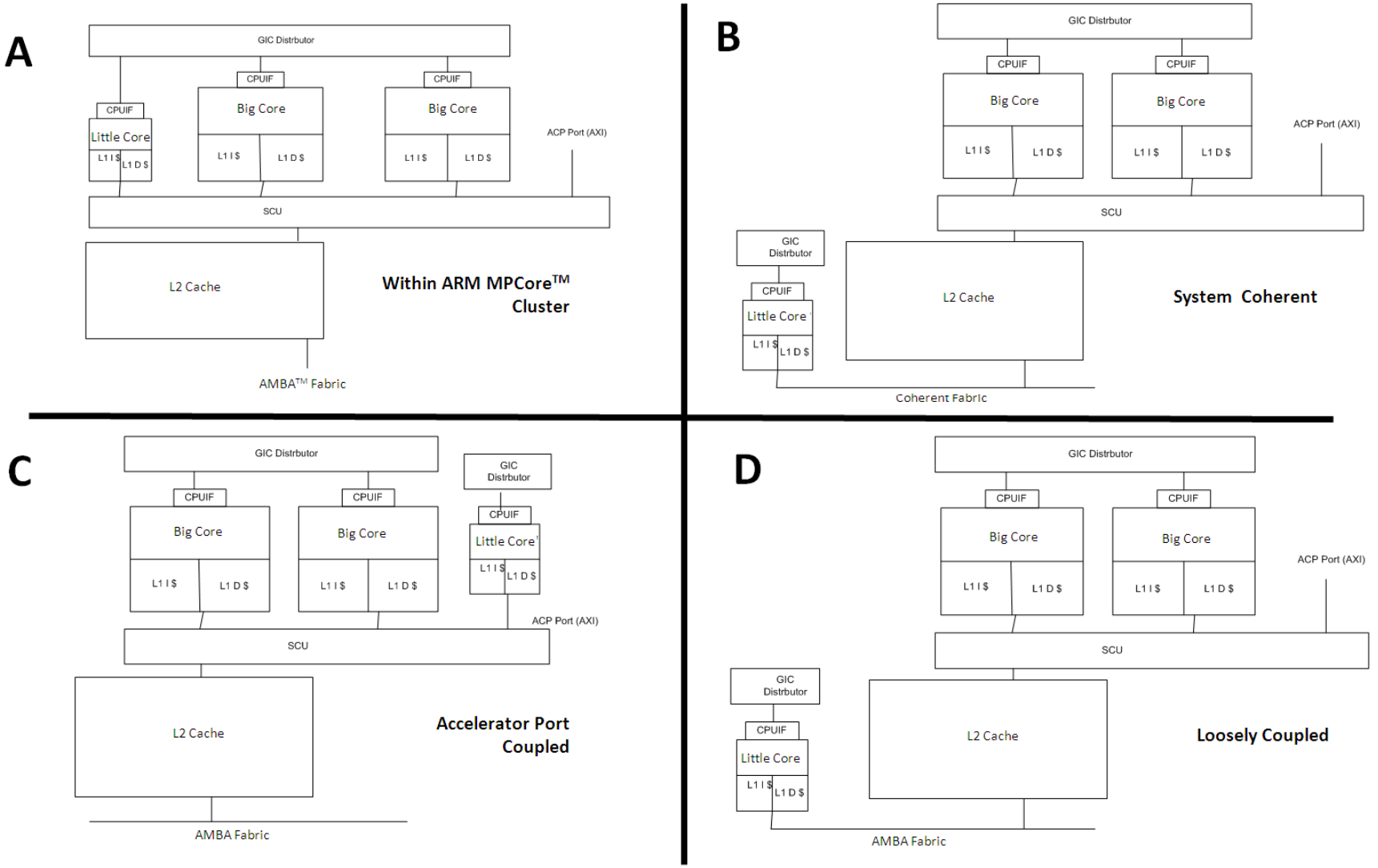
Director, Program Management
ARM Processor Division

August 2009

Interesting System Configurations…



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Background

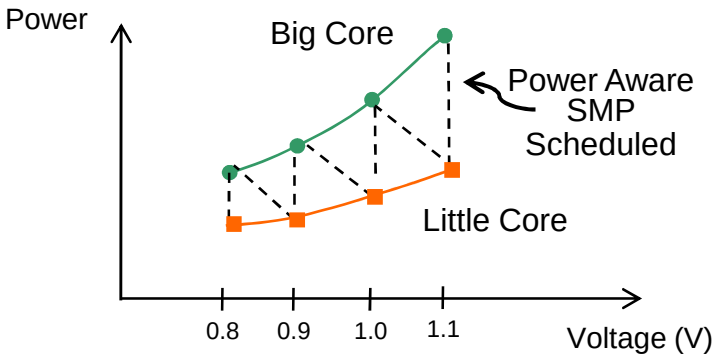

Fig 1a : Power at Peak performance per Operating Voltage

- Smooth transition between energy and performance levels
- Reduced loss due to leakage power as cores can be switched off
- Addresses the application performance diversity

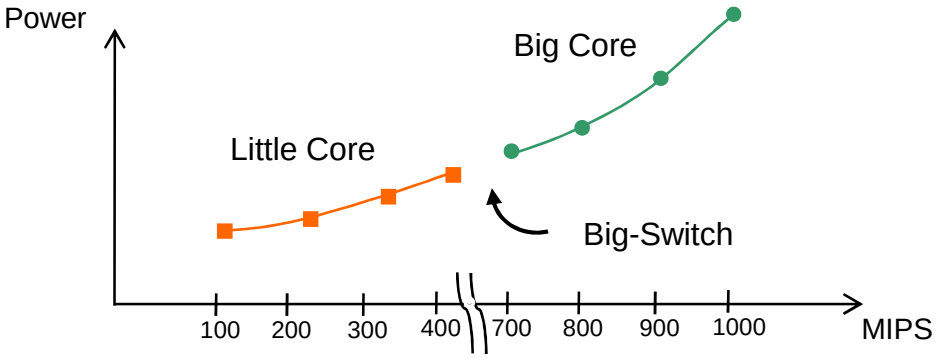

Fig 1b : Power-Performance Diversity of Single Task Workloads

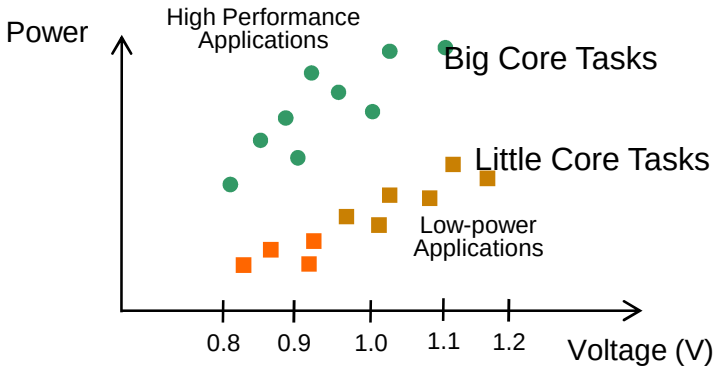

Fig 1c : Diversity of Multitask Workloads

Disclaimer : The plots are indicative of practical architectures and systems.

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Analyzing Diversity

- Code compatibility (due to uniform ISA) ensures easy dynamic task migration (Fig 2a)
- Task migration for power efficiency based on required performance (Fig 2b). Example shows a set of tasks T_1 – T_5

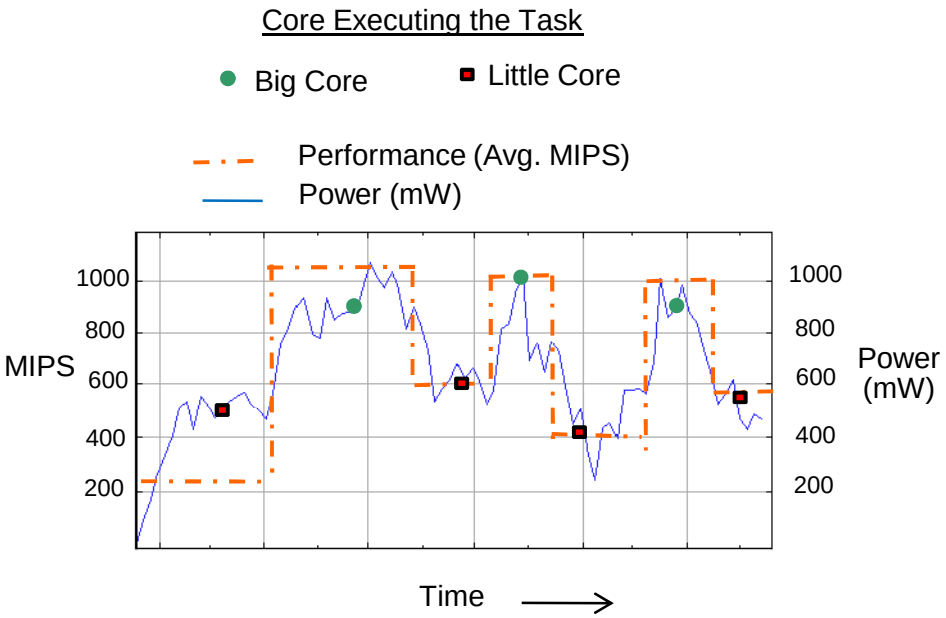

Fig 2a : Single task migrating across cores over time

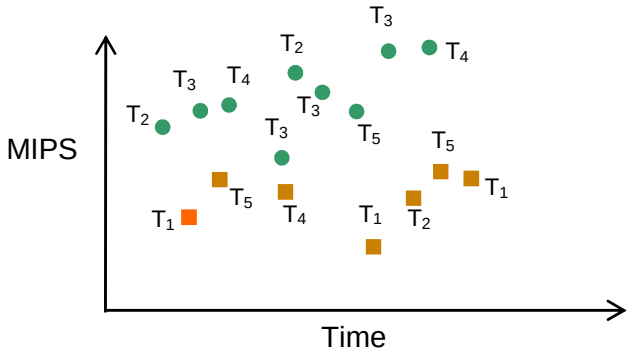

Fig 2b : Task migrations over time based on performance requirement in a Multitask Workload

- Prevents smaller tasks from corrupting high performance task execution. E.g. Task T_1 in Fig 2b.
- Important to further analyse temporal effects of SoC power

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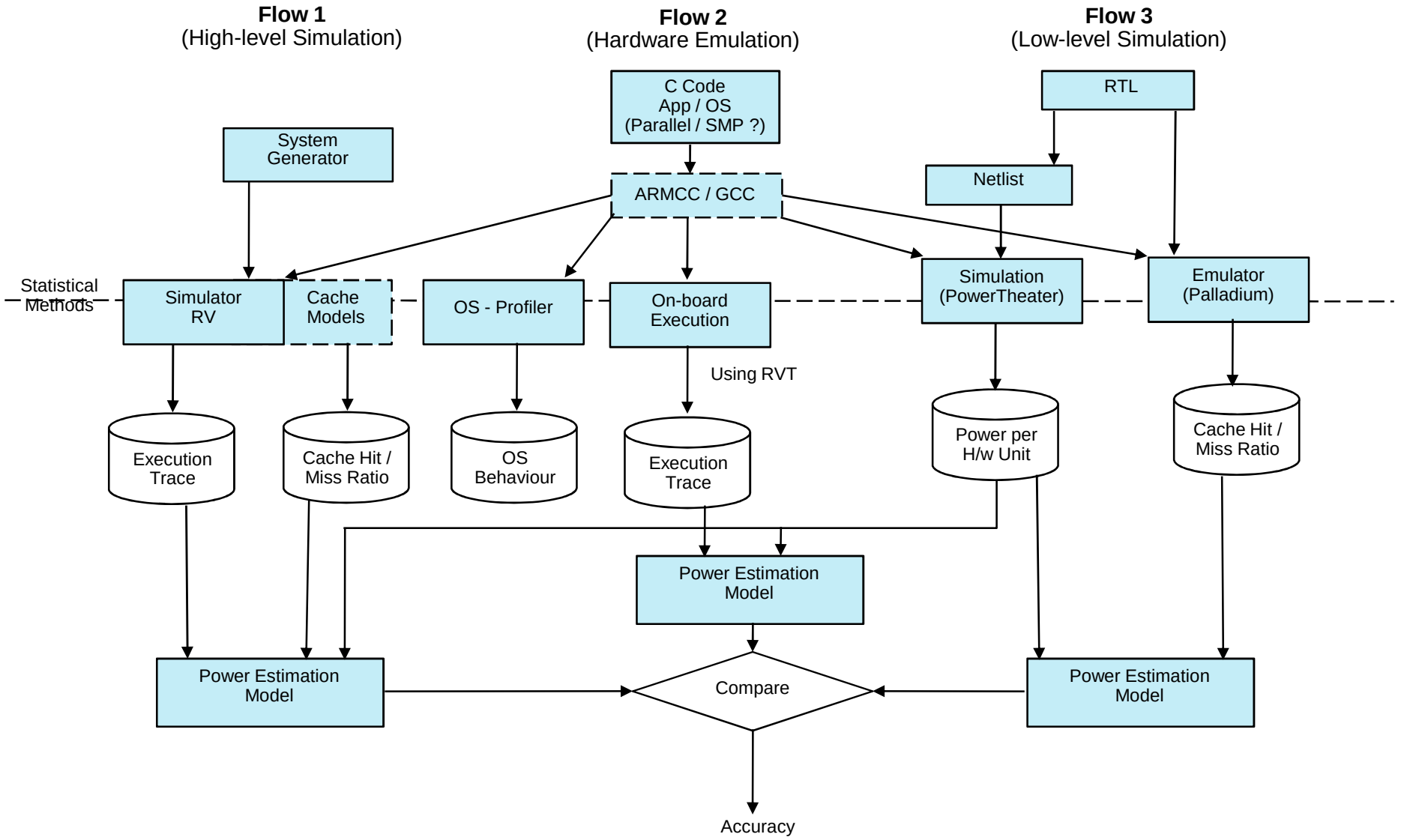
Methodologies Being Utilized



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Software Model Considerations

	Power Aware SMP	Big-Switch
Level of OS modification	Requires affinity to be driven by performance requirement	Potentially no changes required
Maximum power save	Can operate as big-switch too	Little and big core need performance continuum
Level of task diversity and peak performance	Enable better scalability	Limited to performance of single CPU
Implementation complexity	OS needs a speculative understanding of performance demands	Invisible to OS, operates similar to interrupt service routine
Management Responsibility	OS performance monitor	Application dependent
Flexibility	SMP / AMP designs	Single CPU only

Summary Expectations

Application Scenario	Power-Aware SMP Scheduled	Big-Switch	Big-Core Only	Little Core Only
Big-Task (700MIPS)	520mW Big-Core (500mW @ 0.8V) + Little-Core (20mW Leakage)	Big-Core (500mW @ 0.8V)	Big-Core (500mW @ 0.8V)	-
Small-Task (350MIPS)	250mW Big-Core (50mW Leakage) + Little-Core (200mW @ 0.8V)	Little-Core (200mW)	Big-Core (500mW)	Little-Core (200mW)
1 Big-Tasks + 3 Small Tasks (1100MIPS)	700mW Big-Core (500mW @ 0.8V) + Little-Core (200mW @ 0.8V)	Big Core (750mW @ 1.1V)	Big Core (750mW @ 1.1V)	-
3 Big-Tasks + 5 Small Tasks (1400MIPS)	950mW Big-Core (750mW @ 1.1V) + Little-Core (200mW @ 0.8V)	-	-	-

Operating Voltage (Volts)	0.8	0.9	1.0	1.1
Big-Core MIPS at Peak Frequency	700	800	950	1100
Little-Core MIPS at Peak Frequency	350	400	450	500
Big-Core Power at Peak Frequency (mW)	500	575	600	750
Little-Core Power at Peak Frequency (mW)	200	250	300	350

Possible Power savings up to 50%

Performance enhancements up to 30% seen by reducing corruption of high performance tasks

Key to still understand the costs of migration

Thank you