System-Level Exploration for 3D MPSoCs including Optical Networks-on-Chip

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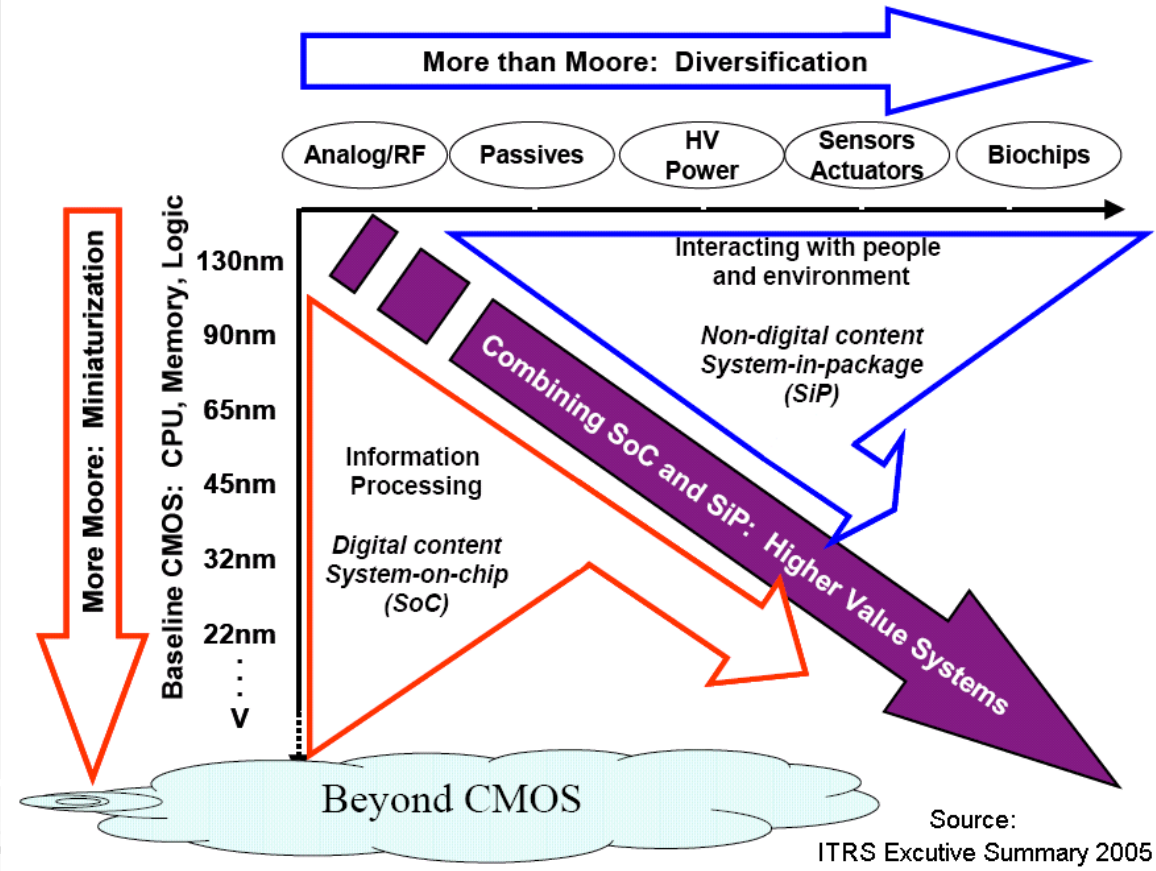
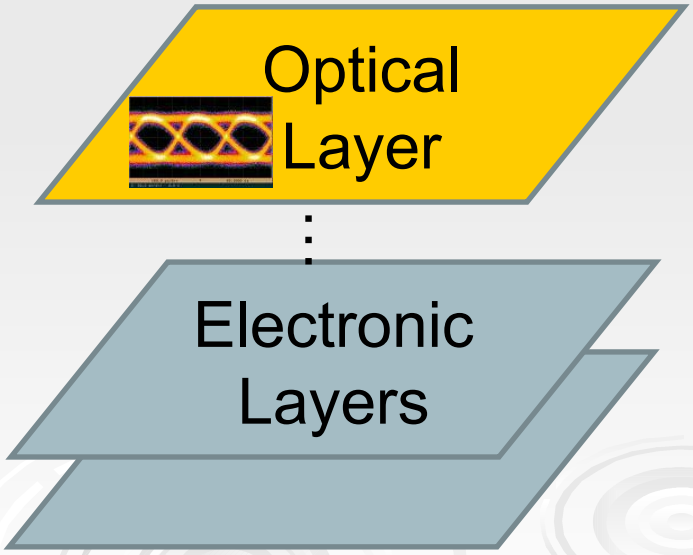
3D Integration Technology

- SoC and System-in-Package Convergence
  - Higher performance
    - More Moore
  - Extended functionalities
    - More Than Moore
    - Equivalent Scaling



3D Integration Technology

- Promising paradigm for Heterogeneous Systems
  - Multiple layers → multiple technologies
  - Functions will use the best technology available
    - Ex. computing → electronics
      communication → optics



System-Level Exploration for 3D

- Research is technology-dominated
  - Physical level research
  - New devices and architectures are defined
- System-level vision required
  - Cooperation between system-level and physical-level designers

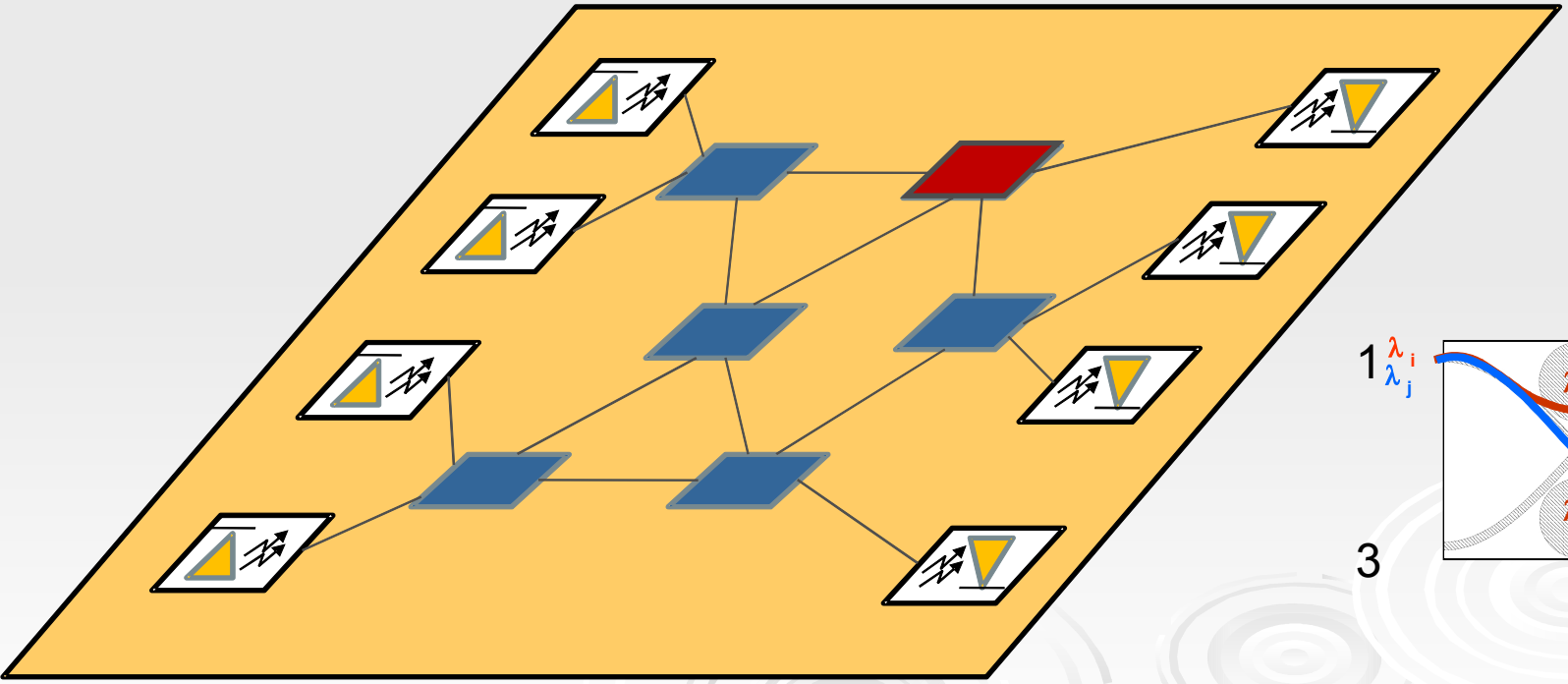
3D MPSoC Including Optical Networks-on-Chip

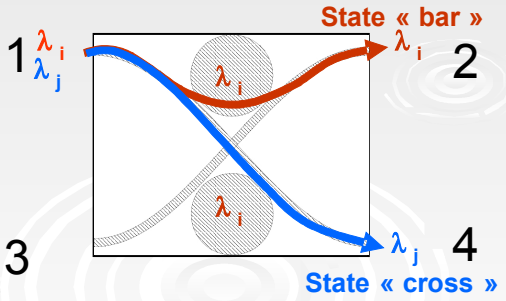
- Architecture defined by extrapolation of 2 planar approches :
  1. Optical Network on Chip
  2. Electrical Network on Chip

3D MPSoC Including Optical Networks-on-Chip

- Architecture defined by extrapolation of 2 planar approches :

1. Optical Network on Chip (ONoC)





3D MPSoC Including Optical Networks-on-Chip

- Architecture defined by extrapolation of 2 planar approches :
  1. Optical Network on Chip
     - Multiple signals of different wavelengths in the same waveguide
       - No contention, high bandwidth density → 20 GB/s
       - Simple, scaleable interconnect
     - Constant latency (<1 ns), function of:
       - Optical index of transmission medium (Si) → propagation delay
       - Waveguide length
     - Frequency limited by optical/electrical interfaces
       - Currently 3.2Gb/s optical (32bits@100MHz electrical)
     - Simpler programming models

3D MPSoC Including Optical Networks-on-Chip

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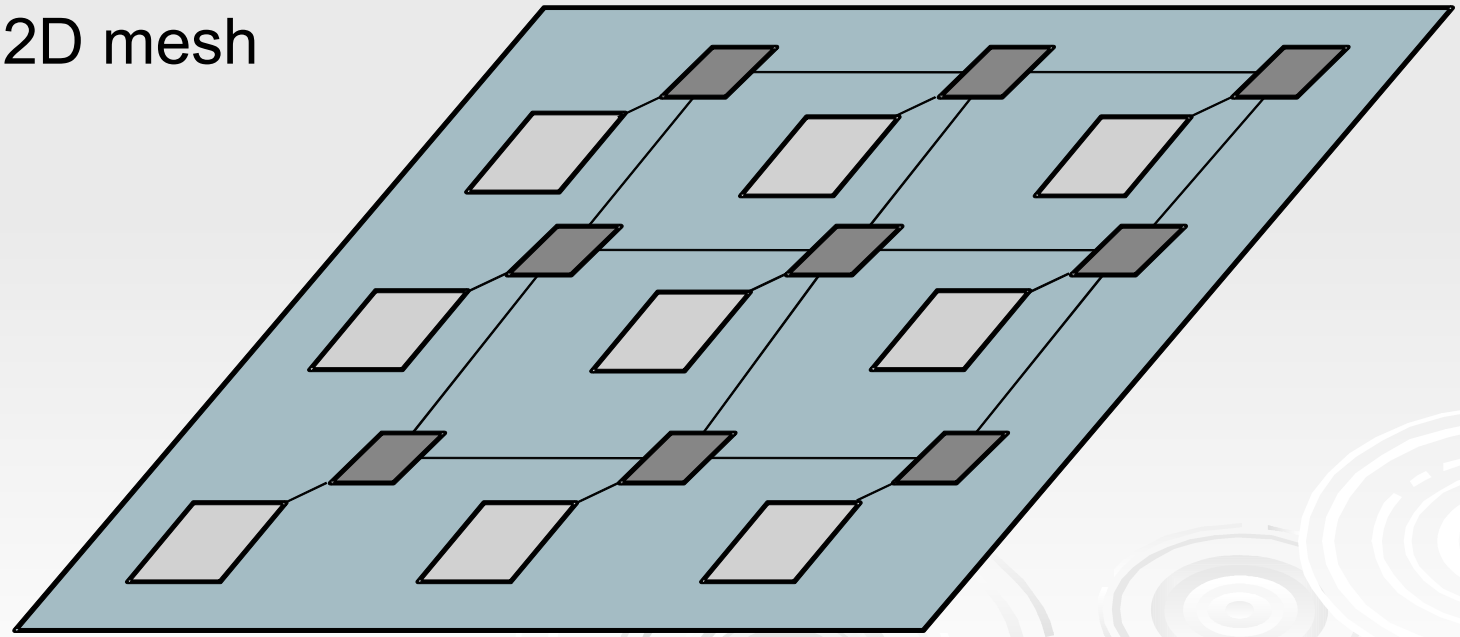
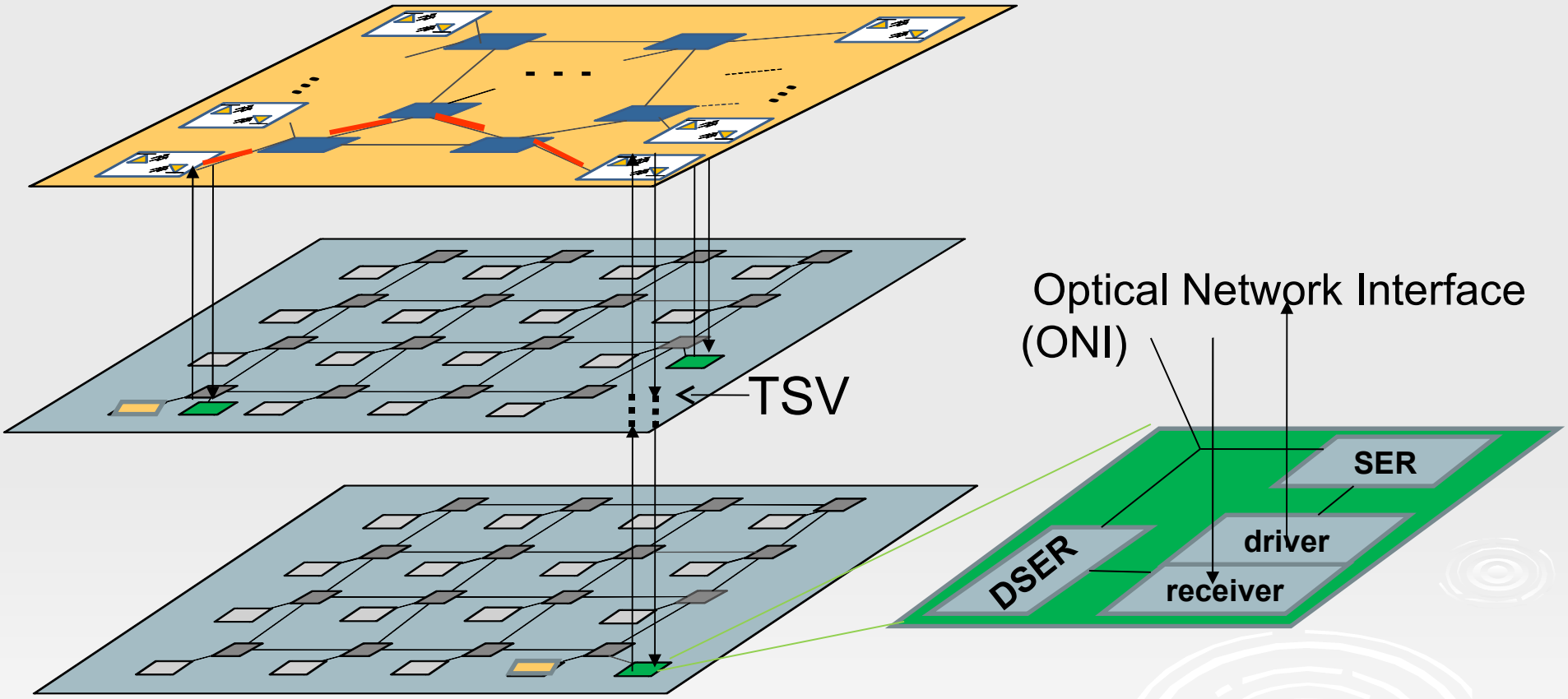
  1. Optical Network on Chip (ONoC)
  2. Electrical Network on Chip

2D mesh



3D MPSoC Architecture



$$\text{Interconnection Strategy (IS)} = \frac{\text{No of Switches Connected to an ONI}}{\text{Total No. of Switches}}$$

System-Level Exploration for 3D MPSoC Integrating ONoC

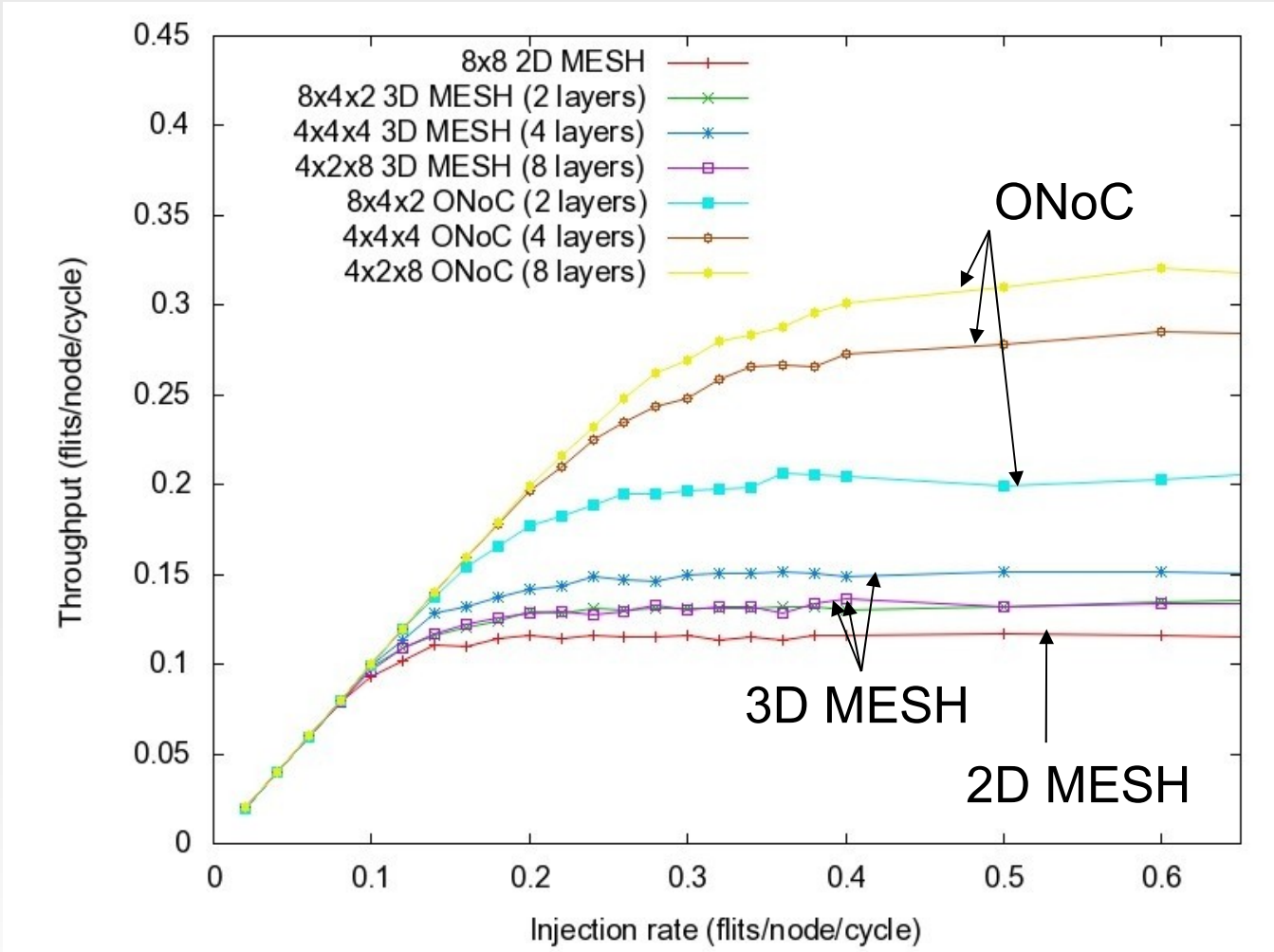
- Internally Developed Event-Based Simulator
  - adapted for 3D MPSoCs
  - Integrating ONoC models
- Electrical routing resources are characterized by bandwidth capability and latency
- Optical Network Interfaces are modeled at transmitter and receiver level and their latency and bandwidth are considered
- Waveguides and optical switches are considered latency free
- Optical switches are characterized by their resonant wavelength

System-Level Exploration for 3D MPSoC Integrating ONoC

- Configuration parameters
  - The number of electrical layers
  - The number of nodes per layer
  - The percentage of switches connected to an optical network interface

Throughput performances

- 64 nodes architectures
- Random traffic generation
- IS = 100%



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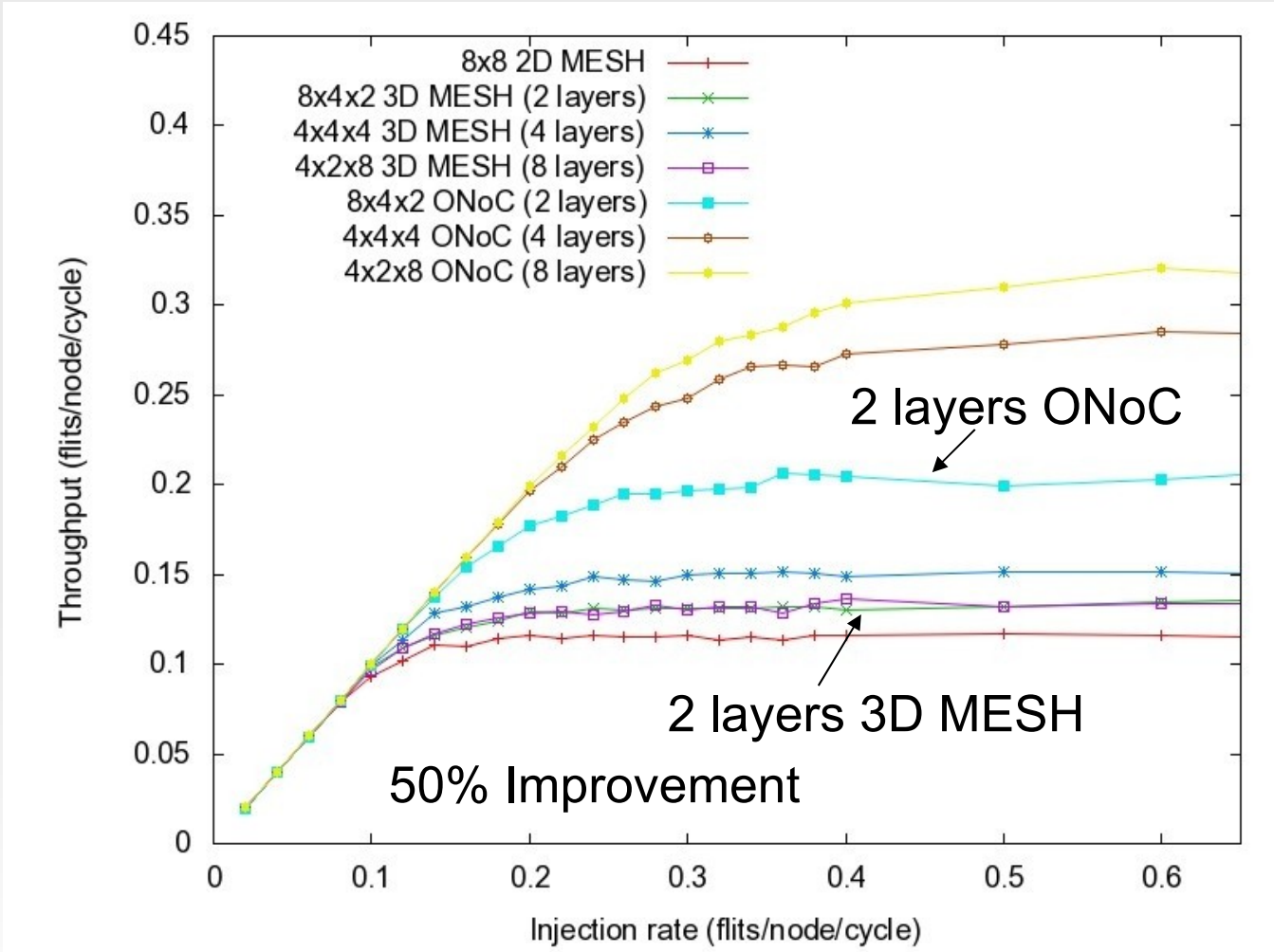
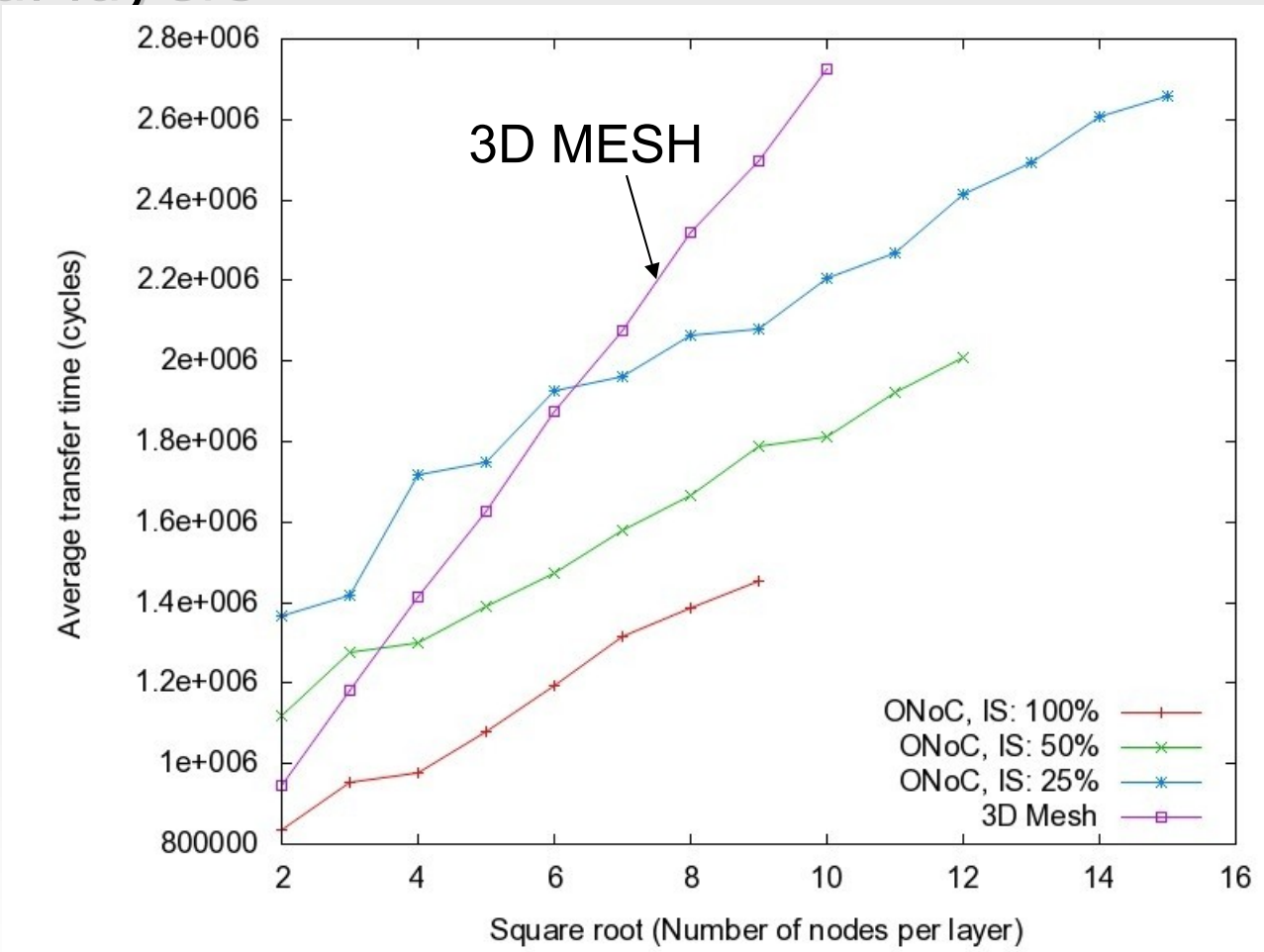
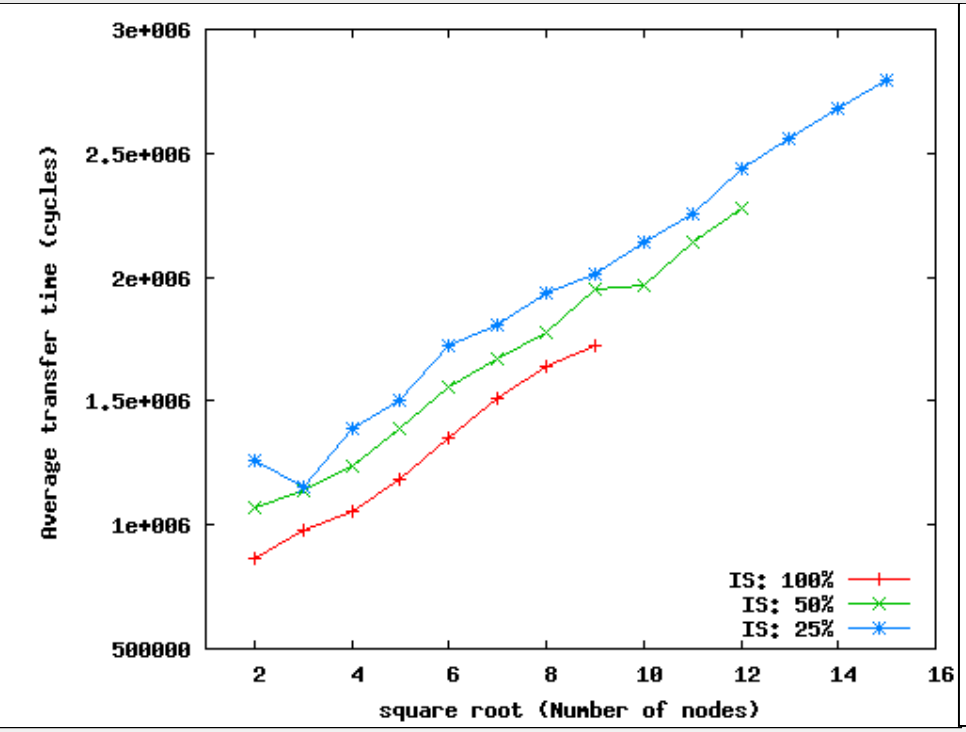


Average Transfer Time

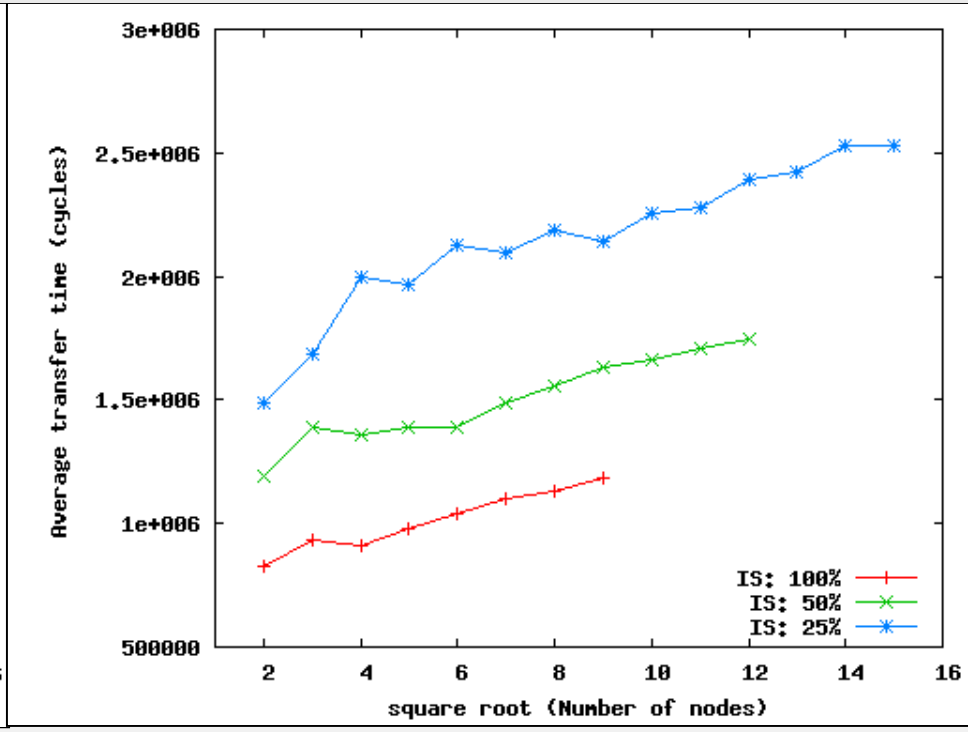
- Injection rate = 1 (i.e. max)
- 2 electrical layers



Throughput (2/2)

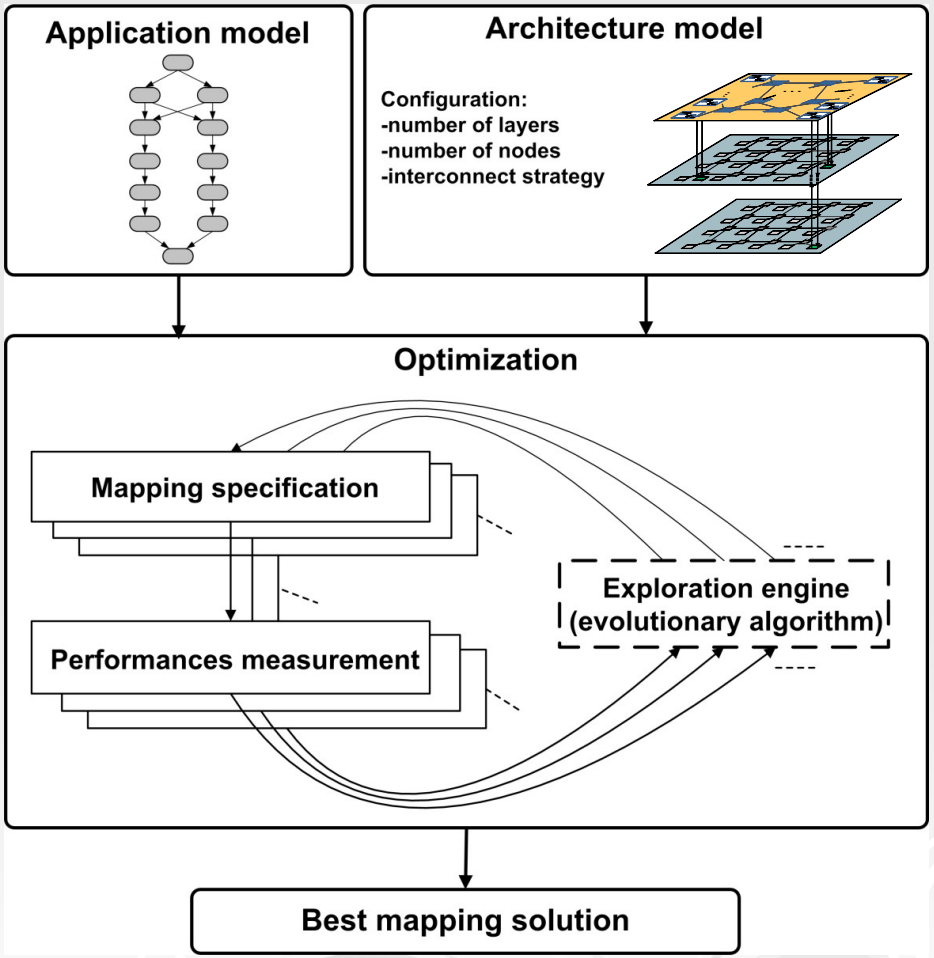


Intra-layers communication analysis



Inter-layers communicatio analysis

Mapping Methodology



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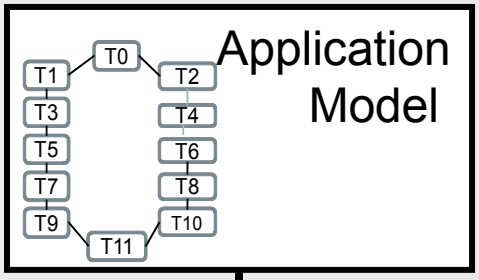
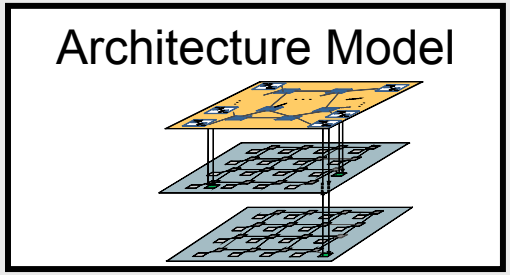
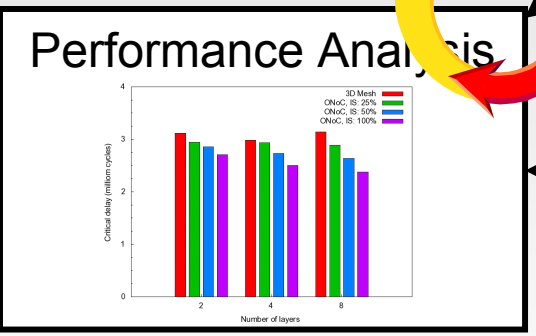
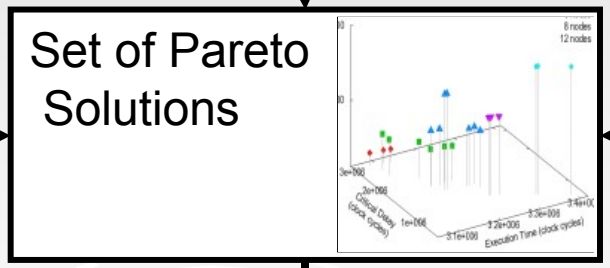


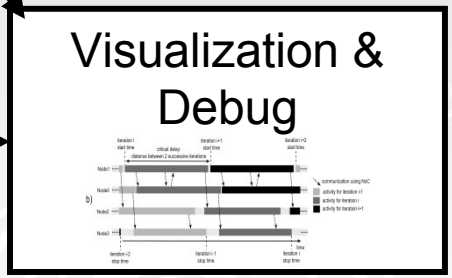
Optimization Metrics



Multi-Objective Optimization
- exploration engine -



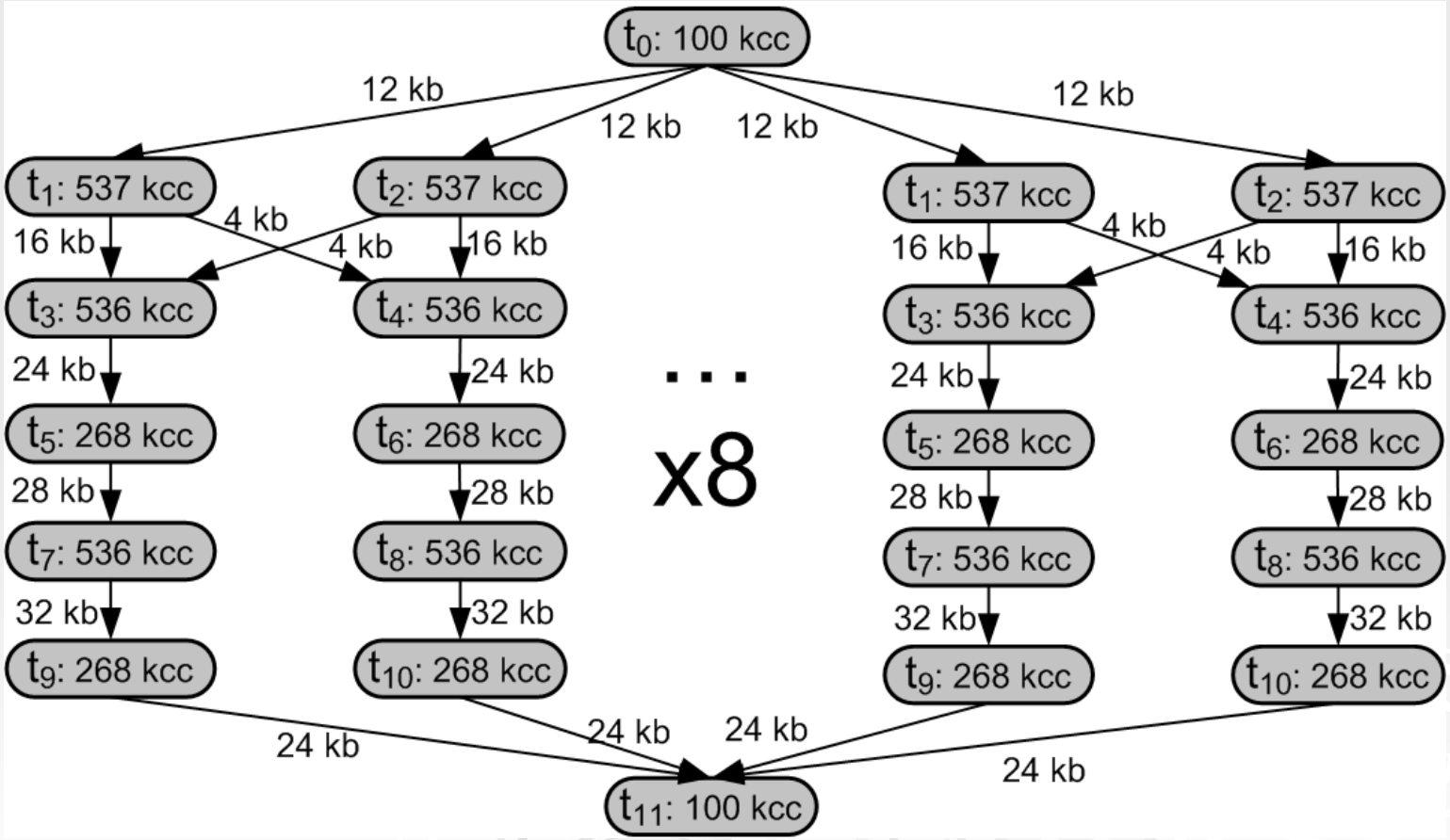




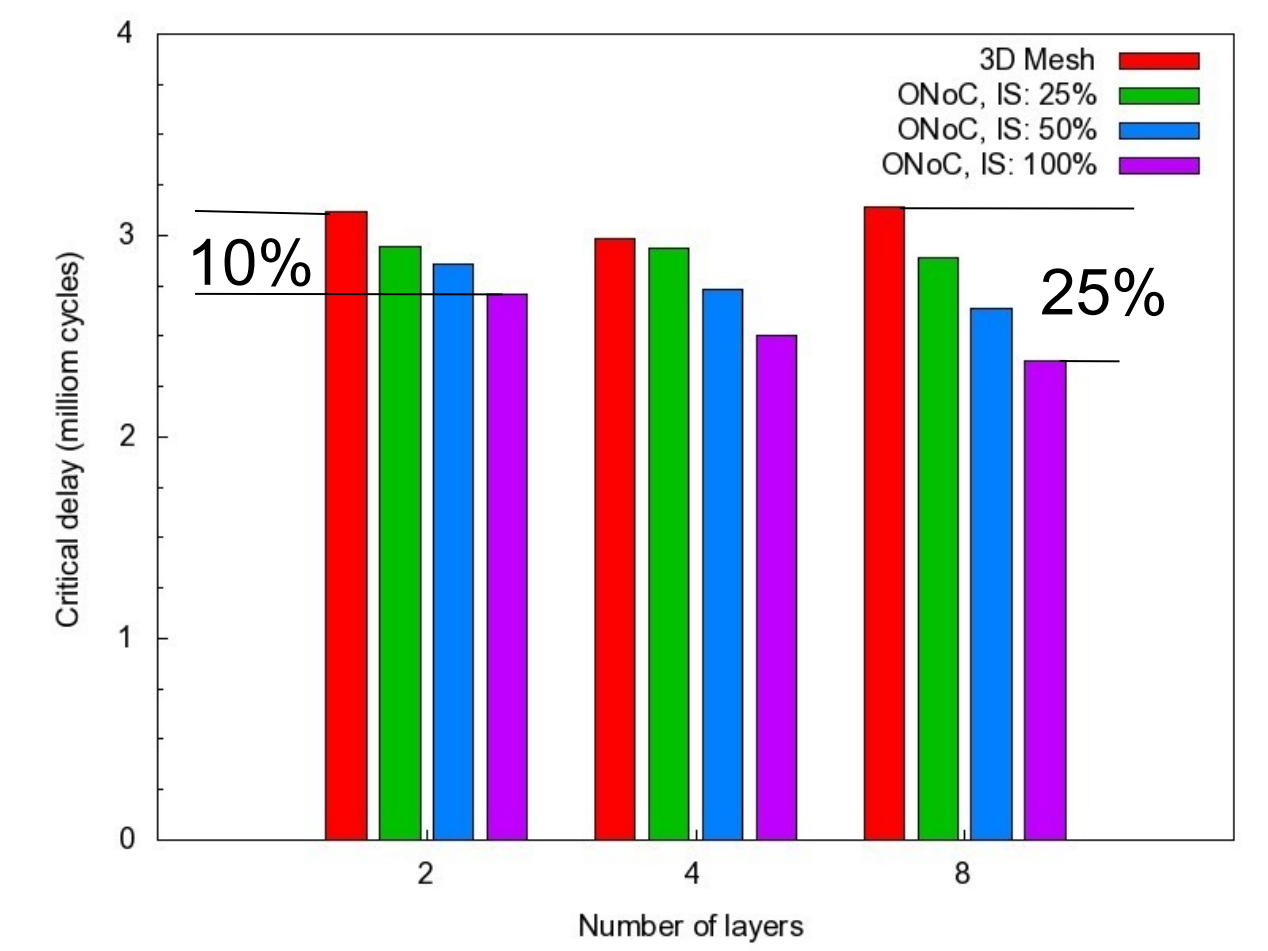
Promising Mappings and Configurations

Exploration for an Image Processing Application

- Demosaic Application



Exploration Results



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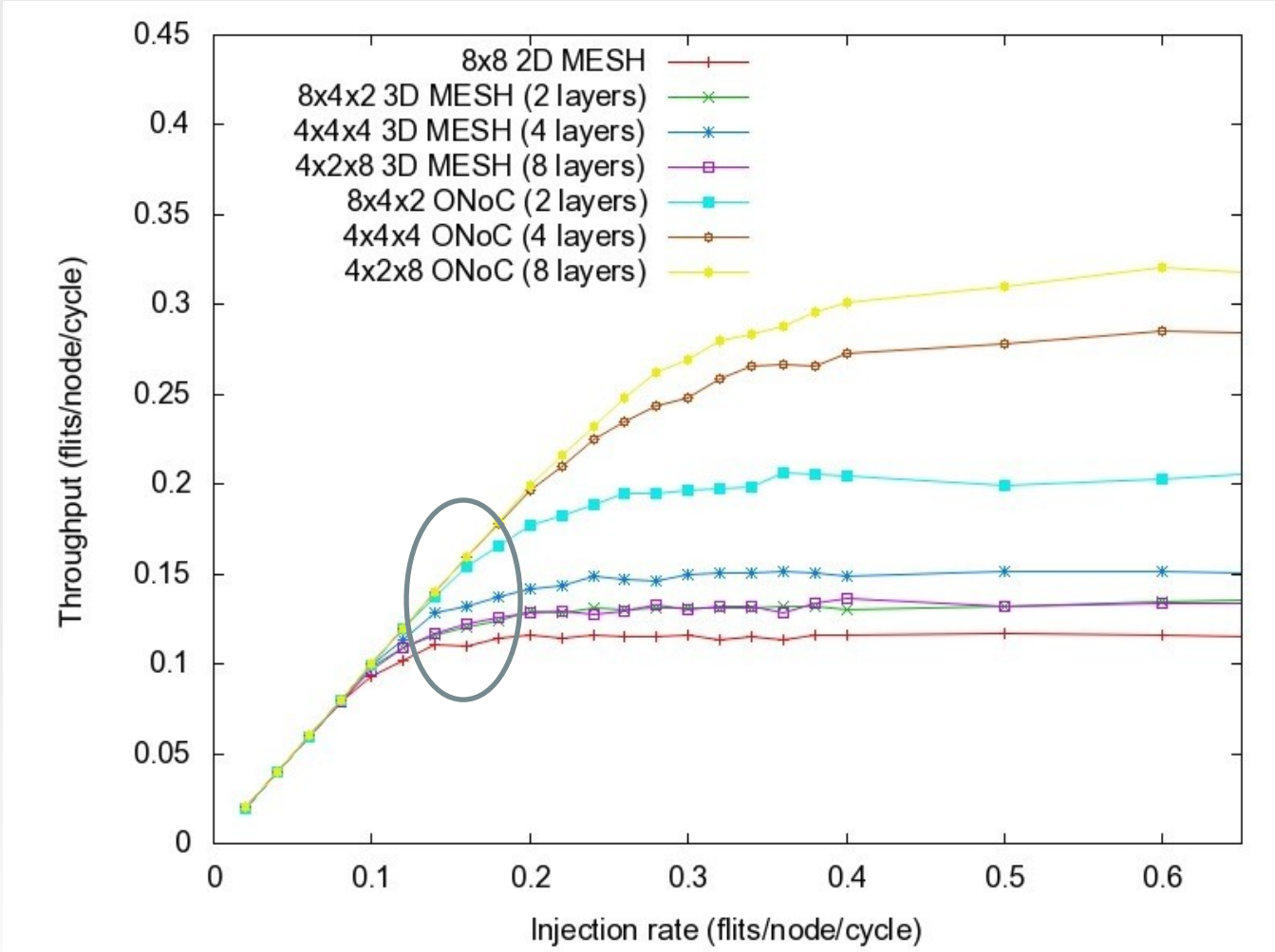

Summary

- 3D technology facilitates heterogeneous systems integration
- Optical Networks on Chip
  - Very Low Latency (<1ns)
  - High Bandwidth (>20GB)
  - Simplifies many-core scaling and programming model support
- System-level exploration for 3D MPSoC integrating Optical Networks on Chip
  - First prototype of a tool enabling configuration analysis
  - Automatic Application Mapping
- Demosaic example shows 10%-25% throughput improvement