Design and Use of Transactional Memory in MPSoCs

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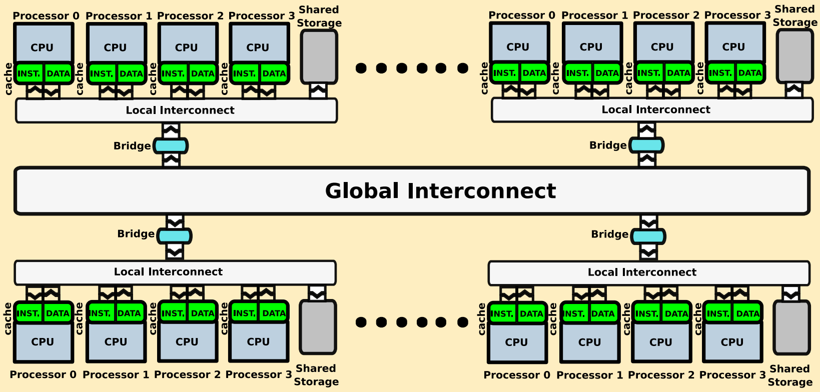
Context: Foreseeable architectural template

Logicically shared, physically distributed memory architecture



- Non-uniform memory access times
- Caches for programming simplicity
- Coherent memory

Context: Efficient exploitation of the available parallelism

Few programs written to exploit parallelism effectively

- Often limited to large parallel workloads
- But may change with the generalization of multi-core PCs

Popular programming model: Threads

- Coordination of execution:
  - Spin Locks
  - Mutexes, Semaphores, Read/Write Locks, Barriers, ...
  - Condition

Limits

- Experience shows that these programs are difficult to:
  - Design, Implement, Debug, Maintain
- ...and often do not perform or scale well

$\longrightarrow$ Need for other programming constructs

Outline

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Transactional Memory (TM)

Transaction API

- Several queries must *appear* as to execute atomically

```
begin_transaction();
 /* All actions taking place here occur in Atomicity
  * and in Isolation */
end_transaction();
```

TM Programming Model ensures

- Atomicity:
  Intermediate state of the transaction hidden from the perspective of other processors
- Isolation:
  Concurrent executing threads cannot interfere with the executing transaction

Example

Thread t1 :

Example Description with Locks

- Several shared structures, one lock per structure
- Modify a structure s1:

```
lock(s1.lock);
    // modify s1 fields
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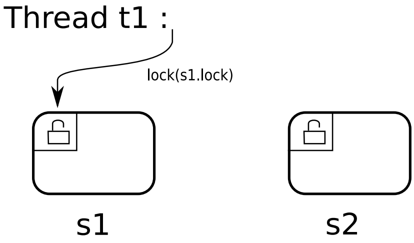

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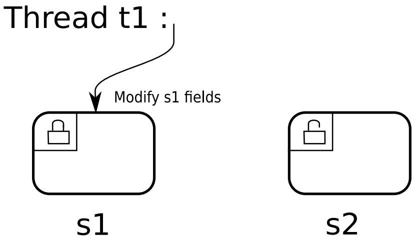

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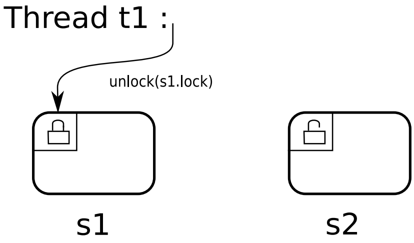

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- Now suppose we want to do atomic operations between two objects
    - Risk deadlock (or impose a total order on structures)
    - Or requires additional locks on tuples of objects
      ⇒ New interface

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With Transactions

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Example

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With Transactions

- Modify a structure:

```
begin_transaction();
   // modify s1 fields
end_transaction();
```

- Modify two structures atomically:

```
begin_transaction();
   // modify s1 fields
   // modify s2 fields
end_transaction();
```

Types of Transactional Memories

Software Transactional Memory (STM)

- Limited hardware support required: only atomic operations
- Many do not believe in STM, controversial subject:
  Software transactional memory: why is it only a research toy? [CBM+08]

Hardware Transactional Memory (HTM)

- Specific support to transactions in hardware
  requires modifications of the whole memory hierarchy [HM93]
- No existing machine currently provides such a support
  Sun Microsystems *Rock* multicore was said to be canceled June 15th, 2009[a]

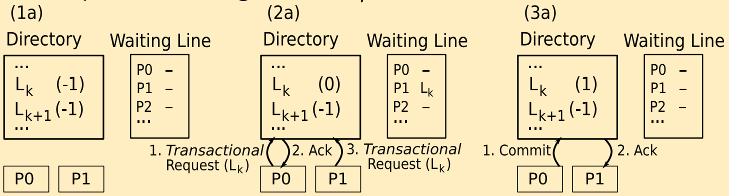
[a]Sun did not confirm or infirm officially

HTM Systems

General Characteristics & Problems relative to HTM Systems

- Granularity of accesses: cache line
- Need to detected conflicting accesses to a variable:

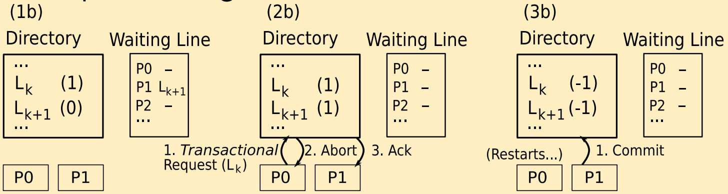
  ⇒ Requires tracking the read/write accesses to a line



HTM Systems

General Characteristics & Problems relative to HTM Systems

- Transaction can abort if there is a conflict:
  i.e. 2 transactions on same line including a write
  ⇒ Requires storing both **old** and **new** values



  - Speculated data (Data that is *computed* but not yet *committed* to memory) have to be stored somewhere
    ⇒ HTM sets can overflow (finite capacity)
- Not so simple architectural support within memory and caches
- Cache-coherence protocol dependent

Very challenging to define and build a working system

Classification of HTM Systems

Main Criteria

- Conflict Detection: when to detect conflicts?
  - Eager: as soon as two concurrent transactions attempt to access the same line
  - Lazy: at commit time
- Version Management: where to store old and new values?
  - Eager: Store the new values in place and the old ones in a log
    Fast commit
  - Lazy: Leaves old values in memory and log the new ones
    Fast abort
- Conflict Resolution: what to do when a conflict is detected?
  - Eager: Stall/Abort the requester(s)
    $\Rightarrow$ Stalling the requester also requires to be able to break potential deadlock cycles by making some processors abort
  - Lazy: Abort the committer

Main Existing HTM Systems Implementations

Main Existing HTM Systems

Short Name	Full Name	Reference
LogTM	Log Based Transactional Memory[a]	[MBM$^+$06a]
TCC	Transactional Coherence and Consistency	[HCW$^+$04]
VTM	Virtualizing Transactional Memory	[RHL05]
UTM	Unbounded Transactional Memory	[AAK$^+$05]
LTM	Large Transactional Memory	[AAK$^+$05]
Bulk	-	[CTTC06]

[a] and its variants: LogTM-SE [YBM$^+$07], TokenTM [BGH$^+$08] and LogTM-VSE [SVG$^+$08]

Standard Design Space Choices and Positioning

LL: Lazy Conflict Detection, Lazy Version Management, committer wins
EL: Eager Conflict Detection, Lazy Version Management, requester wins
EE: Eager Conflict Detection, Eager Version Management, requester stalls

LogTM	→	EE	TCC	→	LL	VTM	→	EL
UTM	→	EE	Bulk	→	LL	LTM	→	EL

Outline

Design Choices & Restrictions for MPSoC

Design Choices: Simplicity

- Use of simple RISC processors, e.g. Sparc V8, Mips 4K
- Write-through, Direct-mapped caches
- Physical address space (no MMU)

Other Design Choices: Still simplicity

- Eager Conflict Detection, Eager Version Management, Resolution scheme based on stalling the requester
- Write-Through Invalidate cache coherence protocol
- Flat transaction nesting semantic

Restrictions: Always simplicity

- One thread per processor, each thread being pinned on a processor
- OS calls and I/O accesses forbidden inside transactions

Architecture and OS Modifications

Architecture Modifications

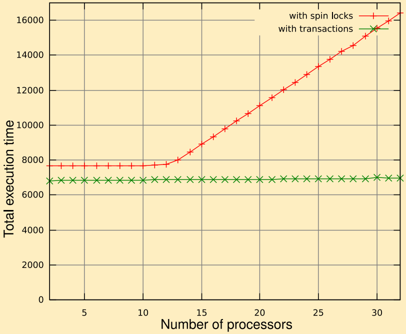
- API
  - `begin_transaction()` and `end_transaction()`: Processor configuration to perform transactional accesses
  - `store_log_address(address)`: Configuration of a specific register in cache
- On processors
  - Addition of a shadow register file in processor, for aborts
  - New instructions or new semantics on existing ones: e.g. `rdasr` on Sparc or `mtc0` on Mips32
- On caches and memories
  - Read and Write sets tracked with R/W bits associated to each cache and memory line
  - Value log: Data Cache
  - Additions to the cache coherency protocol and the interconnect protocol

Status

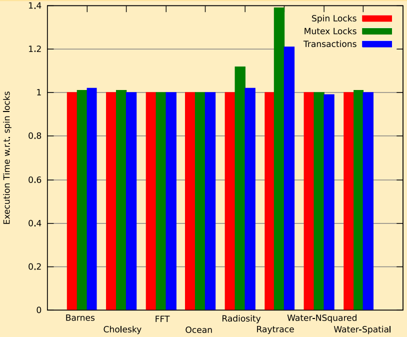
LightTM: HTM System under design

- Cycle Accurate Bit Accurate modeling of the whole system
- 2-32 Sparc V8, Abstract NoC Interconnect, modified SoCLib models
- Kernels and Splash 2 (parallel workloads) benchmarks

Preliminary results



Run times vs Number of processors for Kernel



Run times for Splash-2 benchmarks, 16 procs

Wrap-up

Transactional Memory

- Concept introduced more than 15 years ago[HM93]
- Currently generating a lot of research
  In Computer Architecture and also Parallel Programming conferences
- Proved to be pretty efficient
- Also proved to be quite complex and costly!

Is it useful for MPSoC?

- More and more programmable IPs in High End Consumer MPSoC
- Need of a simple shared memory parallel programming paradigm
- But quite complex to implement and not RT friendly

May be (part of) a solution

DATE 10
Design, Automation & Test in Europe
8-12 March, 2010 - Dresden, Germany
The European Event for Electronic
System Design & Test

A8: Multi-core Platforms

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