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Thermal Modeling and Active Cooling for 3D MPSoCs

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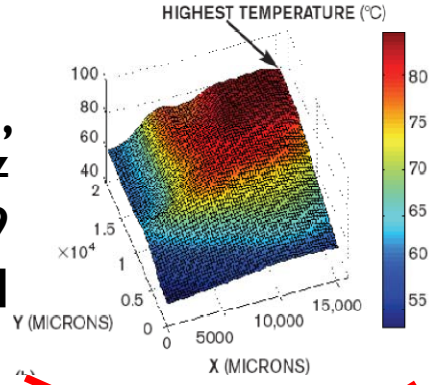
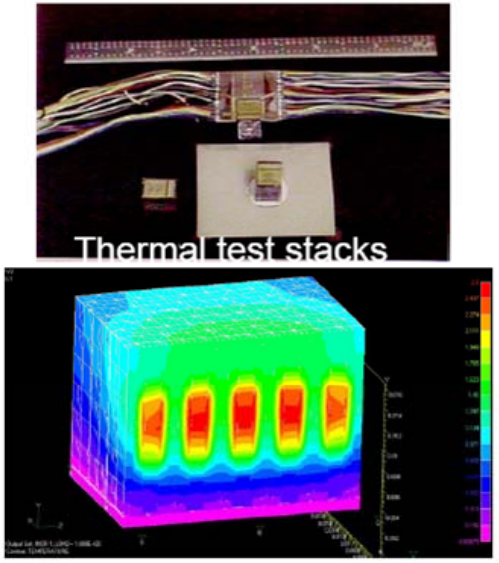
Thermal-Reliability Issues in 3D Chips

- Latest chips increase power density
- Non-uniform hot-spots in 2D chips
- In 3D chips, heat affects several layers! (even more "cool" components)

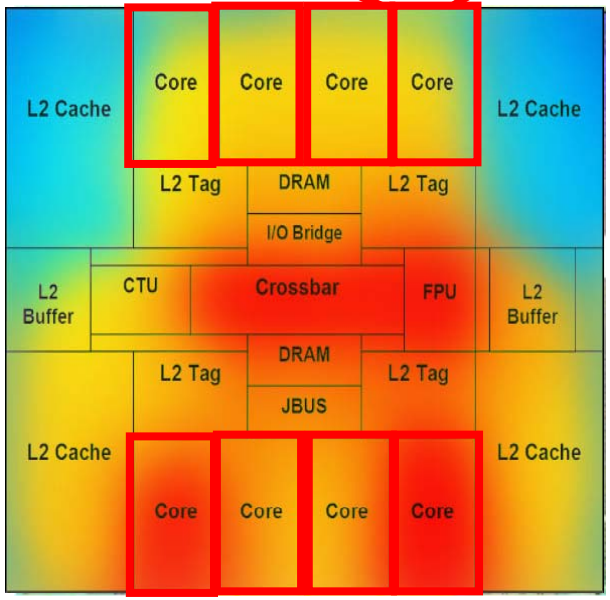
[Sun, 1.8 GHz Sparc v9 Microproc]



Courtesy: [IBM and Irvine Sens.]

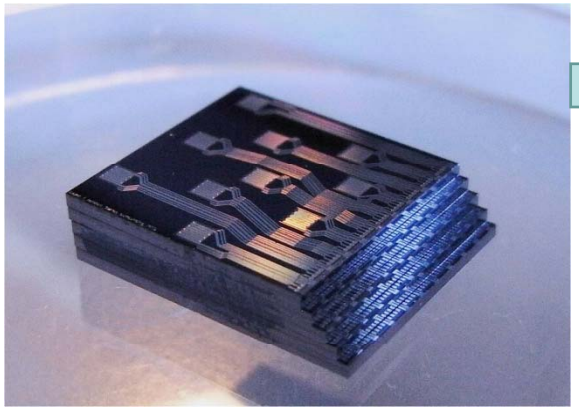


[Sun, Niagara Broadband Processor]

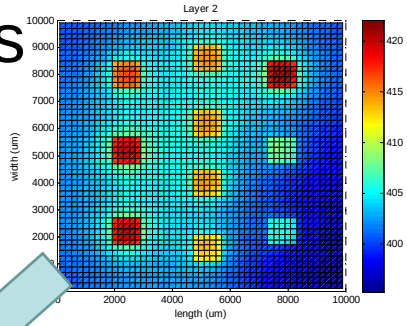


Run-Time Heat Spreading in 3D Chips

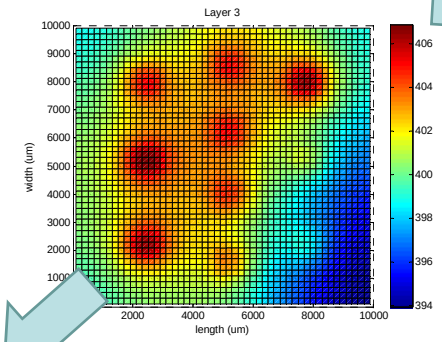
- 5-tier 3D stack: 10 heat sources and sensors



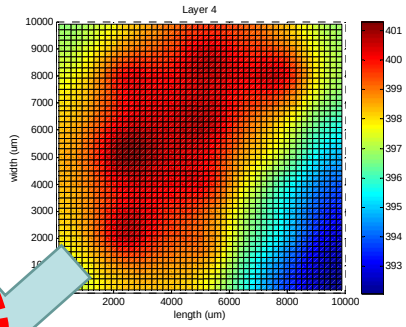
Inject between 4W – 1.5W



2nd Tier

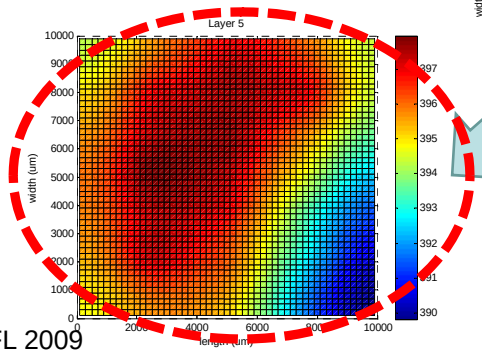


3rd Tier



4th Tier

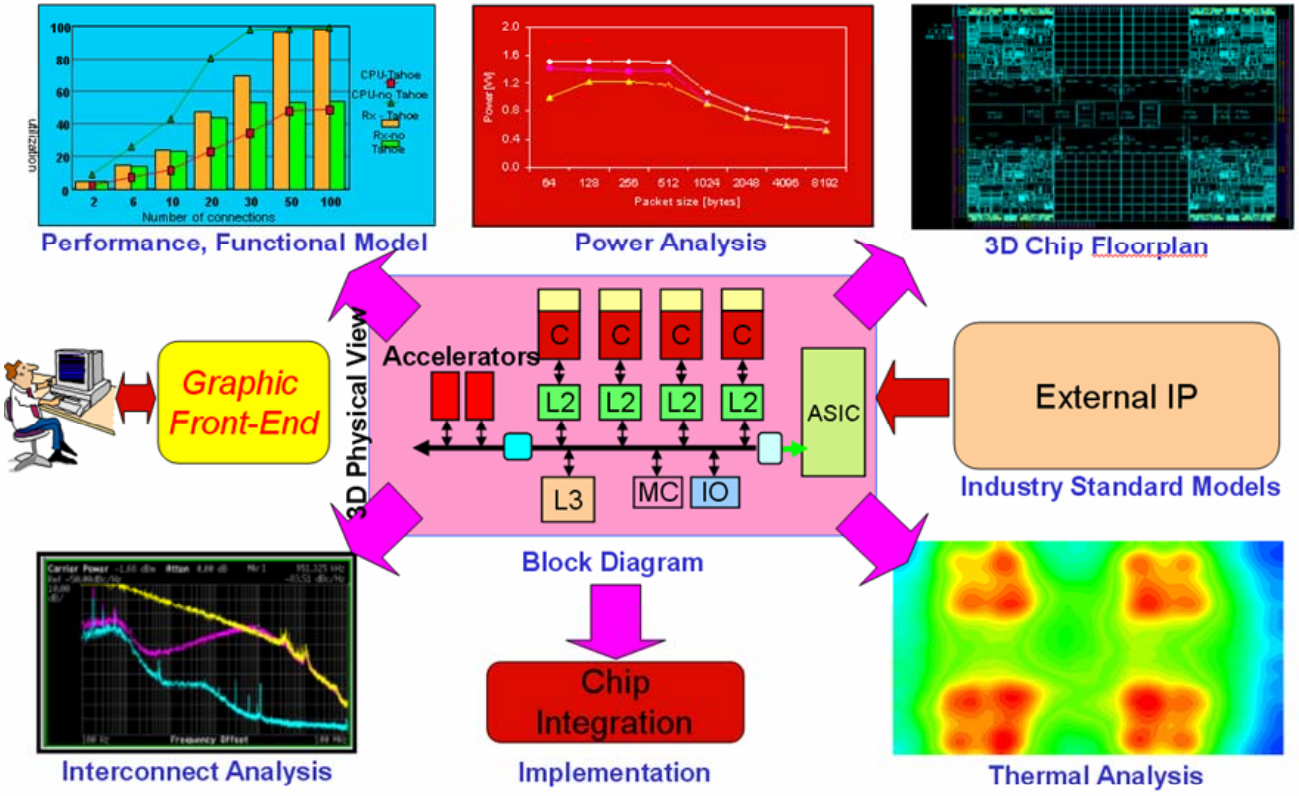
5th Tier



Large and non-uniform heat propagation!
(up to 130º C on top tier)

NanoTera CMOSAIC Project: Design of 3D MPSoCs with Advanced Cooling

- 3D systems require novel electro-thermal co-design
  - Academic partners: EPFL and ETHZ
  - Industrial: IBM Zürich



NanoTera CMOSAIC Project: Design of 3D MPSoCs with Advanced Cooling

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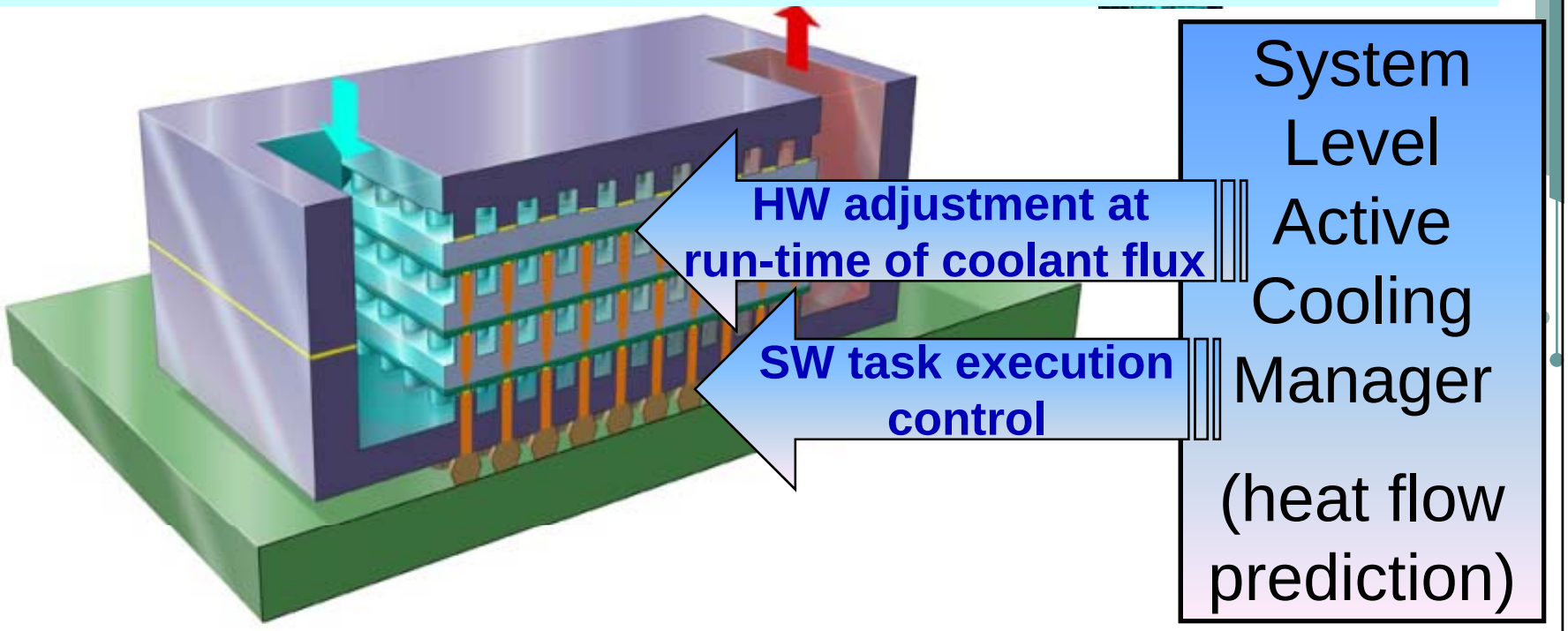
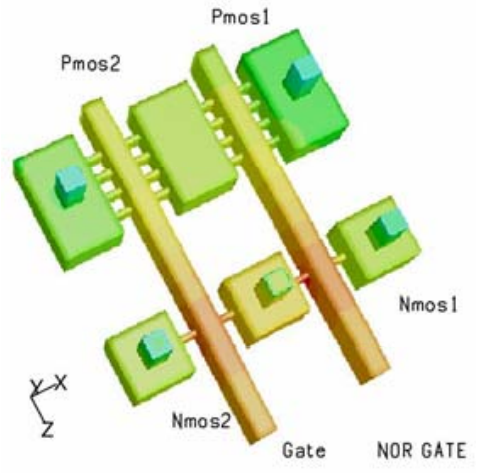
3D stacked MPSoC chips: microchannels etched on back side to circulate liquid coolant



Compact RC-Based Tier Thermal Model

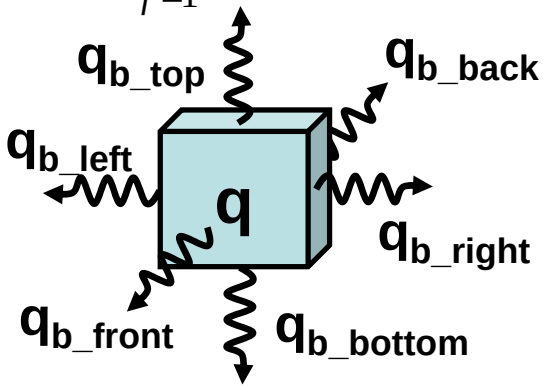
- Gate-level thermal model



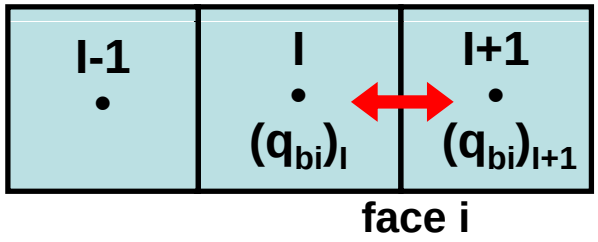
Network of

Si/metal layer cells

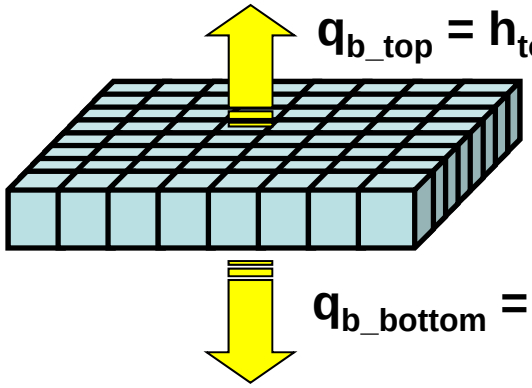
$$q_{bj} = \sum_{f=1}^{6} b_{fj} T_f + b_{0j} \cdot q$$



- 2D tier modeled as heat flux moving between adjacent cells



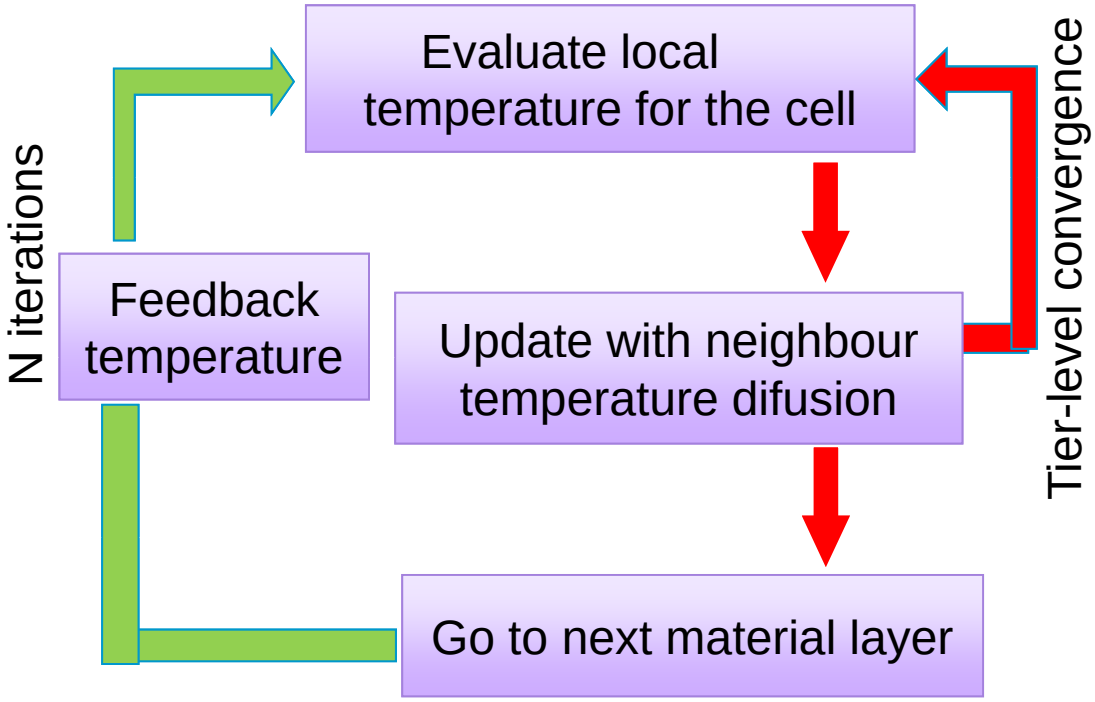
- Convective boundary conditions between layers in tier

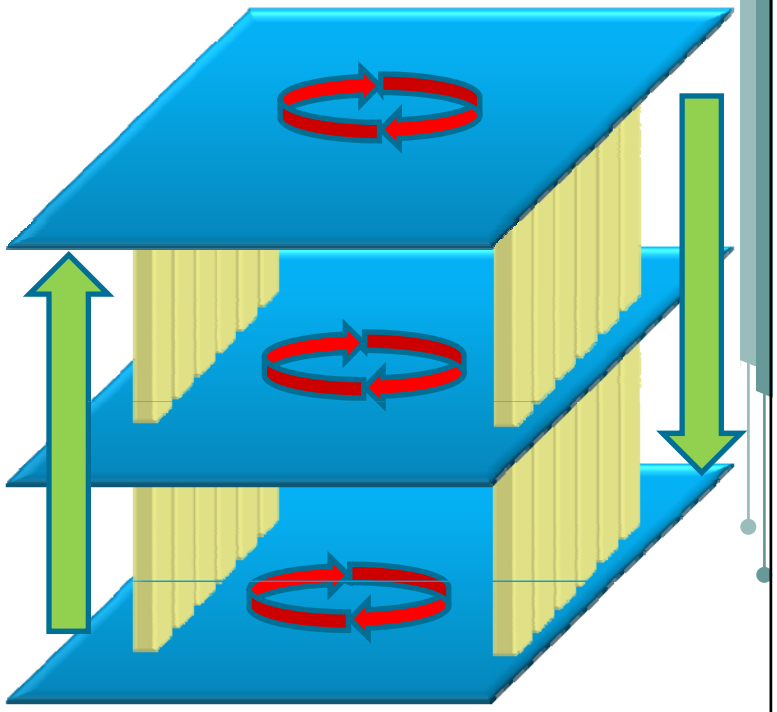


[Atienza et al., TODAES 2007]

Complete 3D Chip Thermal Modeling

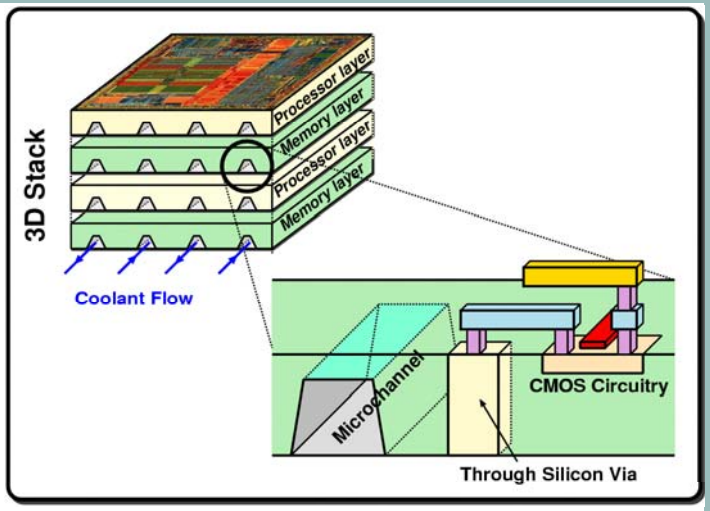
- Multi-level execution for thermal convergence in 3D
  - Local (2D-tier) and then global (3D) propagation

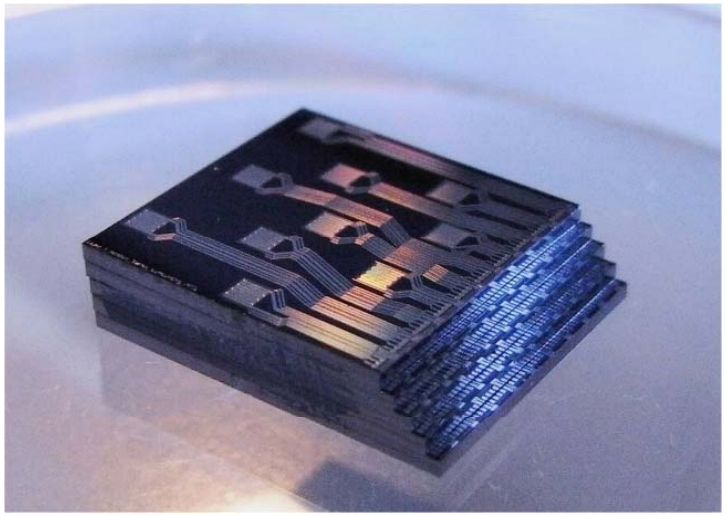


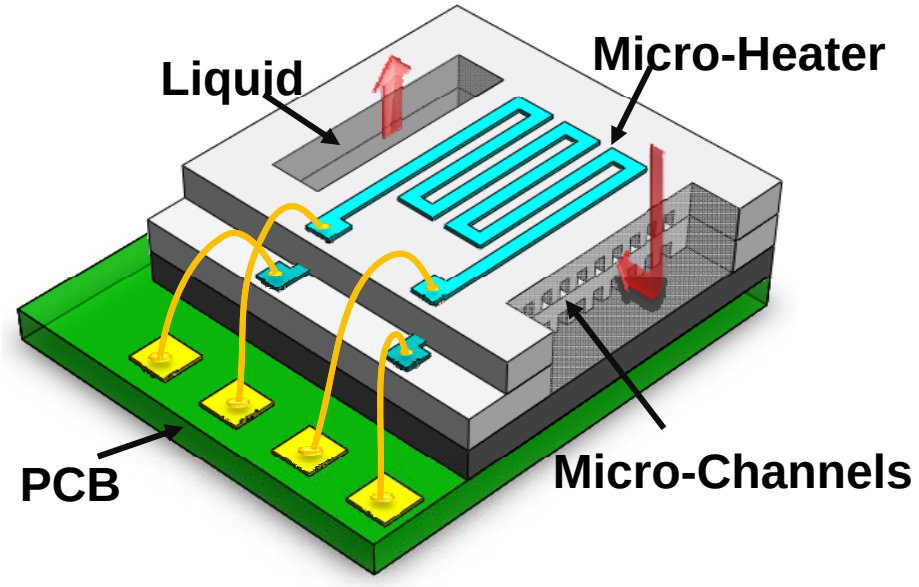


3D Thermal Model with Liquid Cooling

- 3D stack modeled as iterative process
  - Each tier and liquid cooling flow
- Flexible set of layers in 3D stack, extendible
  - 3D stack (up to 9 tiers)
  - Pre-defined layers:
    - Silicon, metal (10 layers), glue, overmold, interposer, bump
- 5-Tier validation stack manufactured at EPFL:

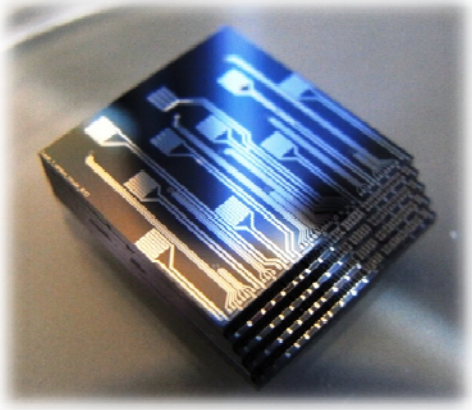


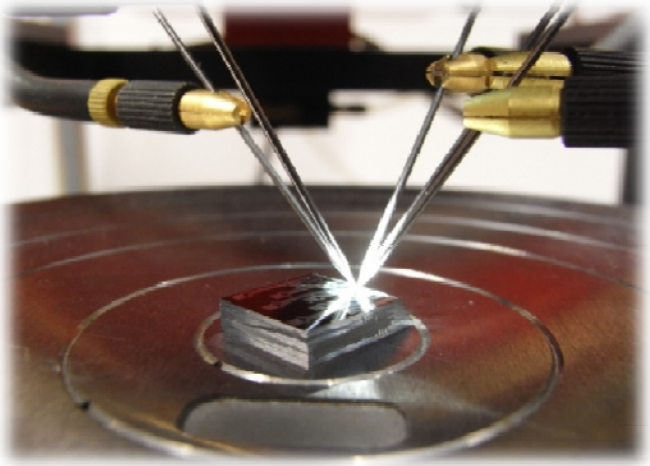


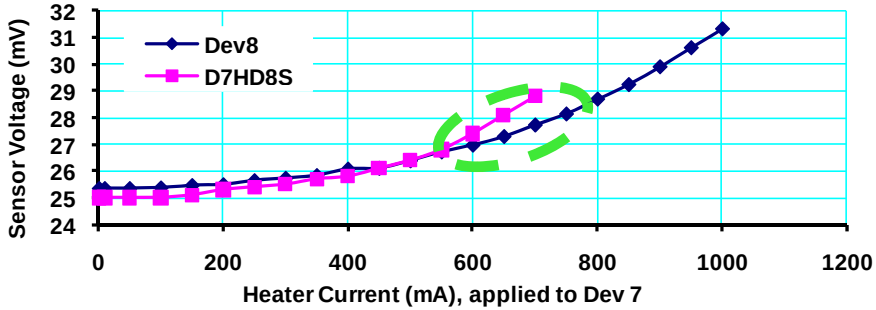


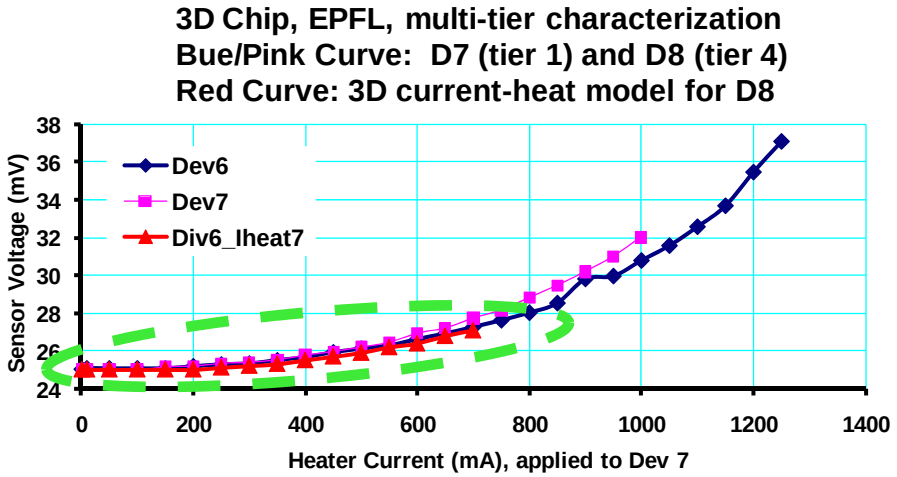
[Ayala et al., NanoNet '09]

3D Thermal Model with Liquid Cooling: Correlation with 5-Tier 3D Stack









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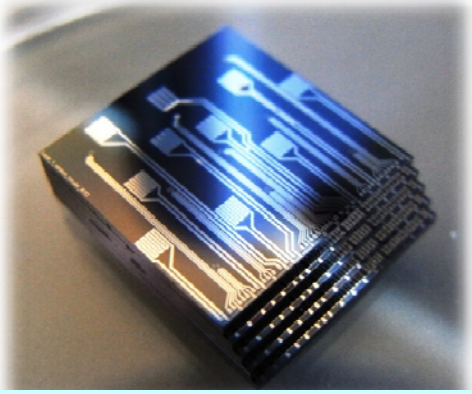
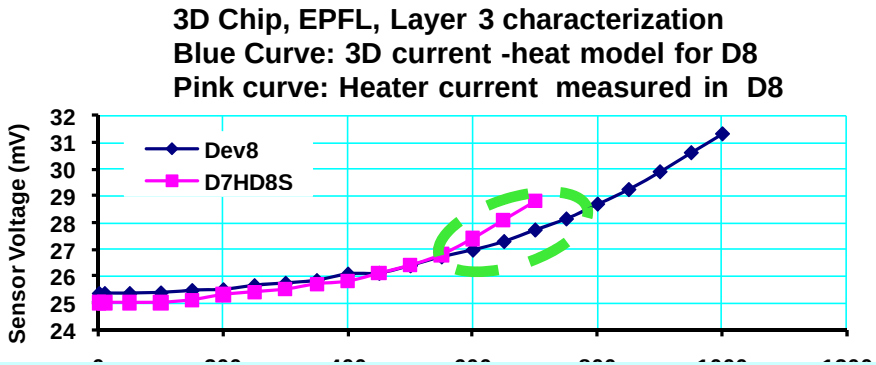
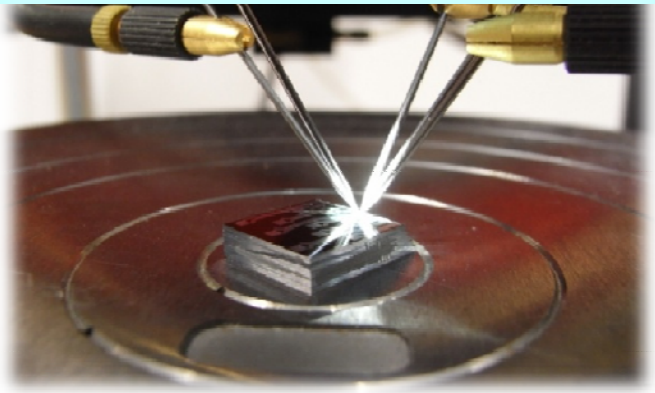
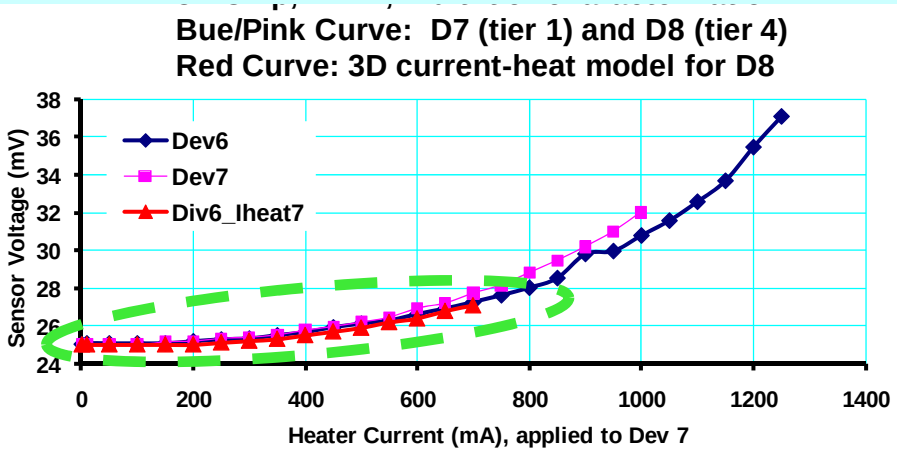




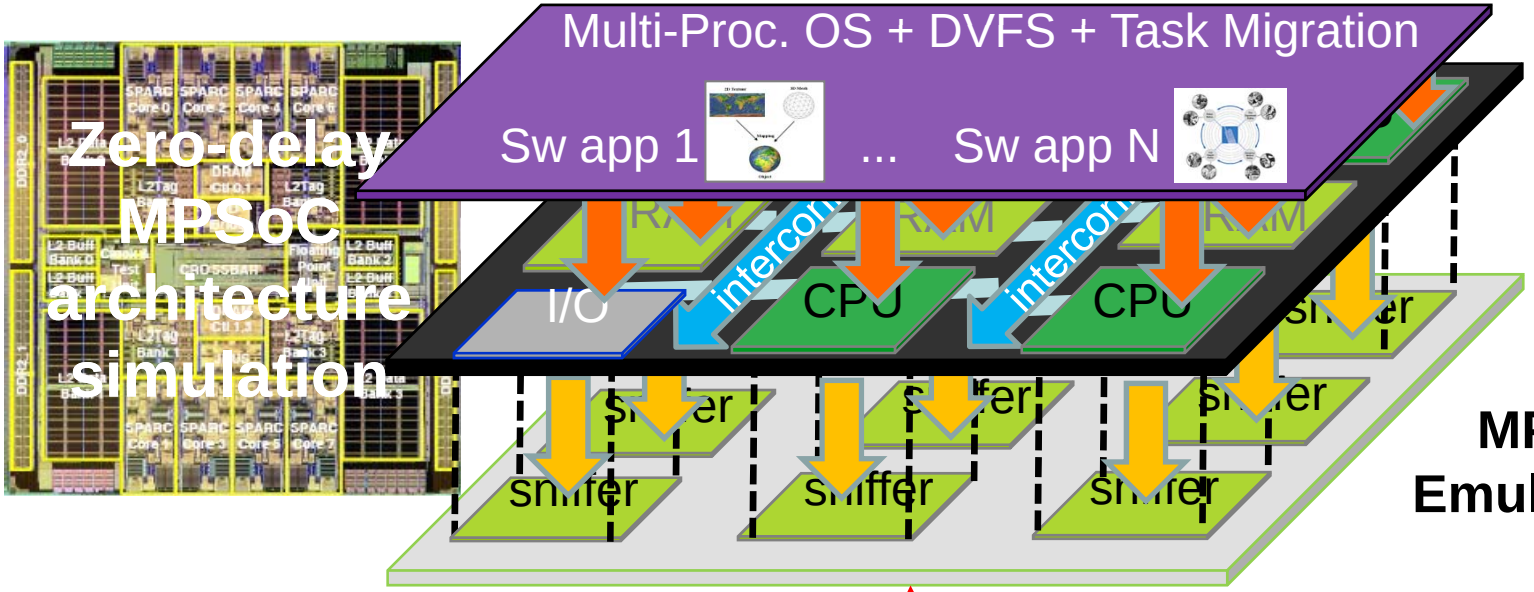
Variations of less than 1.5% between 3D stack measurements and new 3D thermal model

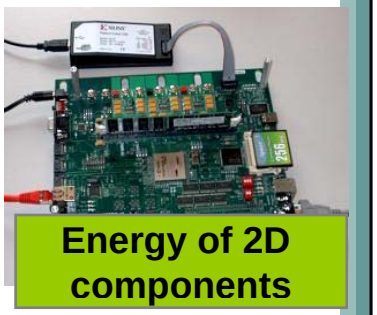




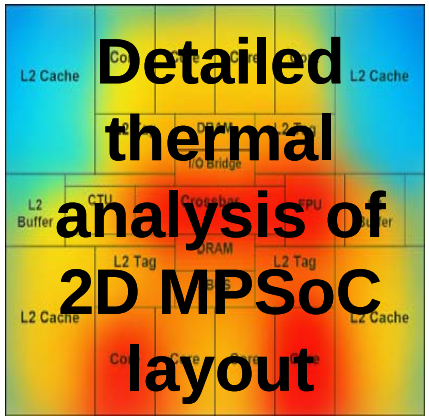
Run-Time HW/SW Thermal Modeling Framework for 2D/3D Chips

- Exploitation HW/SW (Atienza et al.,TODAES 2007, THERMINIC '09)

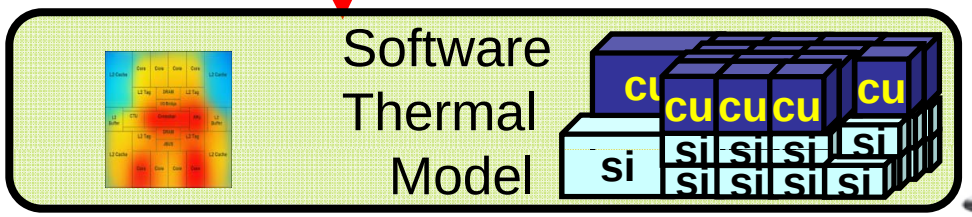




MPSoC Behavior Emulation on FPGA



standard Ethernet connection & dedicated HW monitor

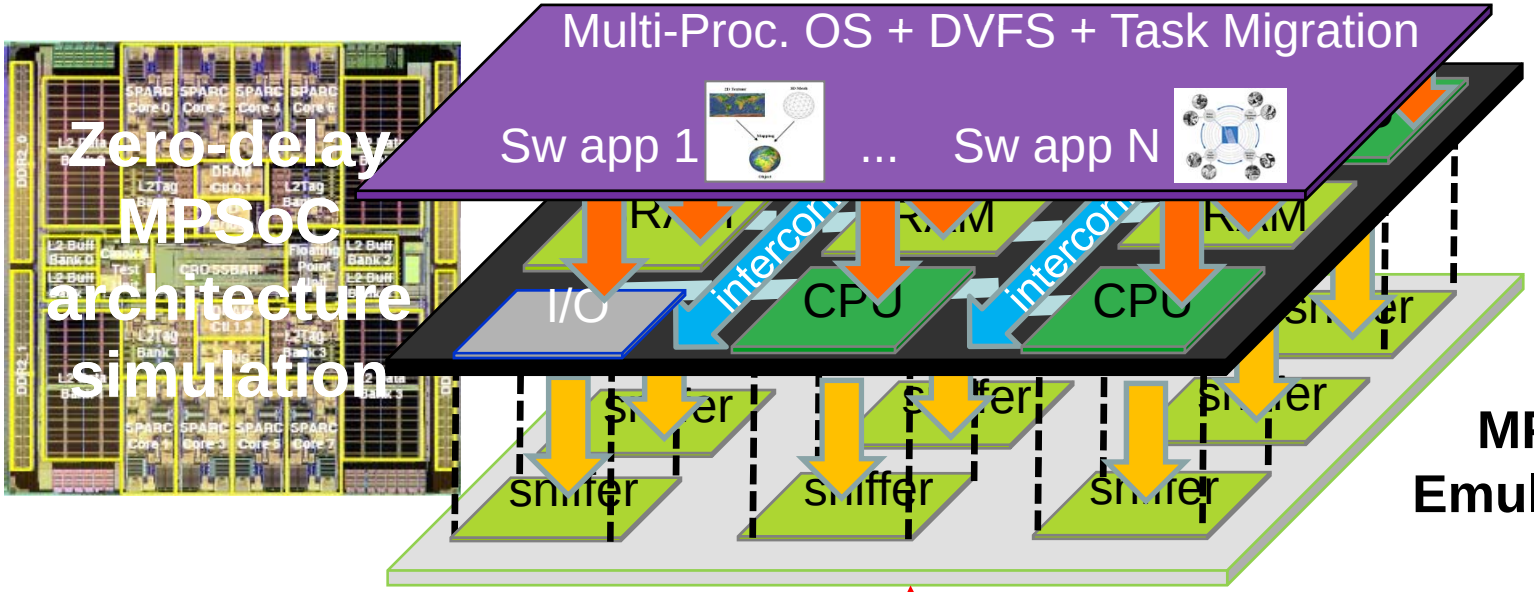


Temp. (T) of 2D components

Host PC

Run-Time HW/SW Thermal Modeling Framework for 2D/3D Chips

- Exploitation HW/SW (Atienza et al.,TODAES 2007, THERMINIC '09)

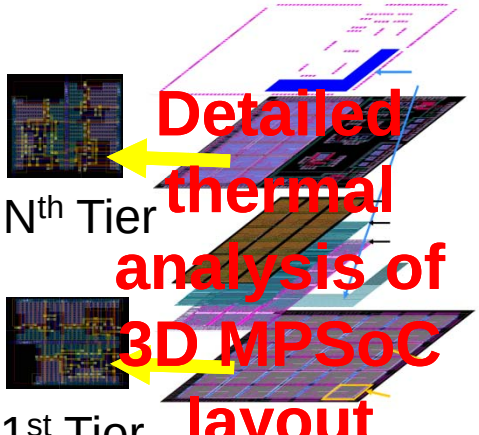


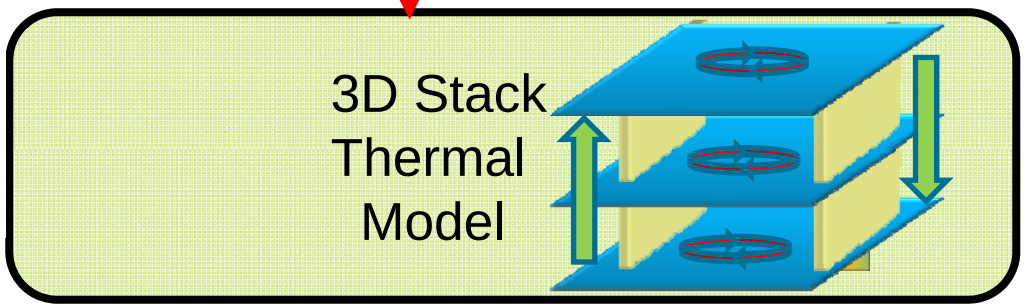
Energy of 3D components

MPSoC Behavior Emulation on FPGA

standard Ethernet connection & dedicated HW monitor

Temp. (T) of 3D components



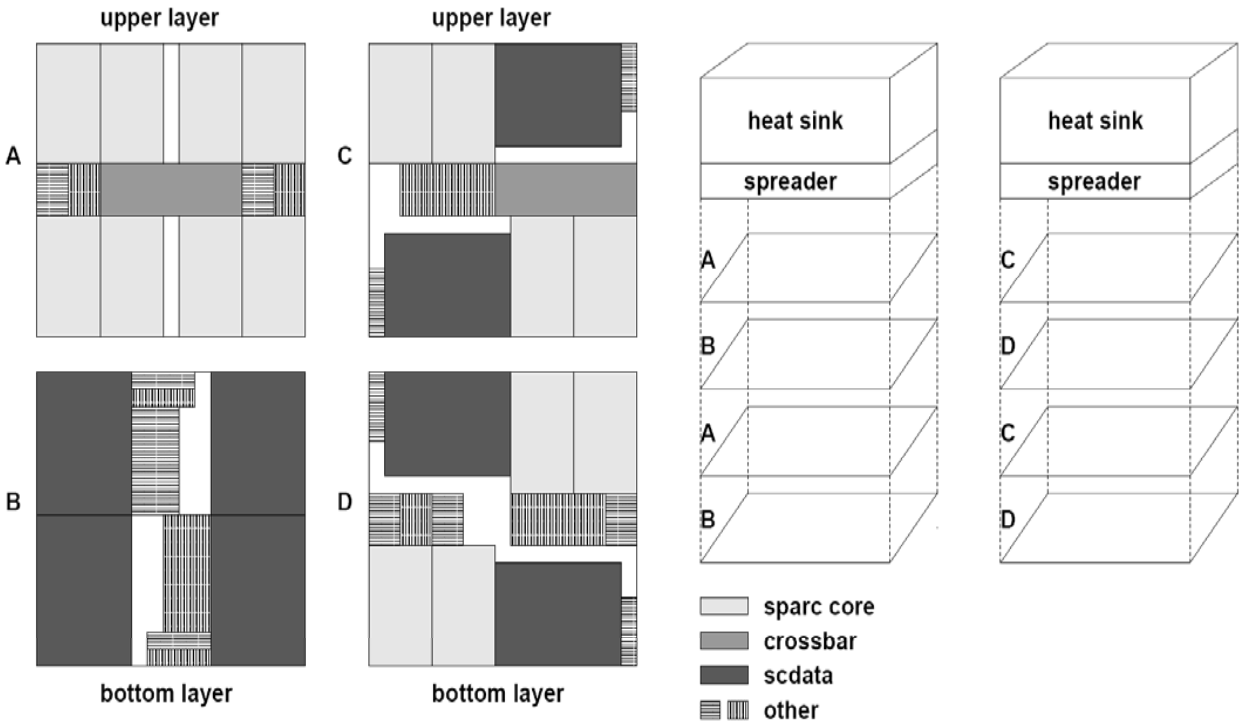


Host PC

Thermal Management for 3D Chips: 3D-Floorplans

- 8-/16-Core Sun Niagara 3D Layouts (2 and 4 tiers)
  - Web and server processing applications

Separ-2 (EXP1) | **Mixed-2 (EXP2)** | **Separ-4 (EXP3)** | **Mixed-4 (EXP4)**

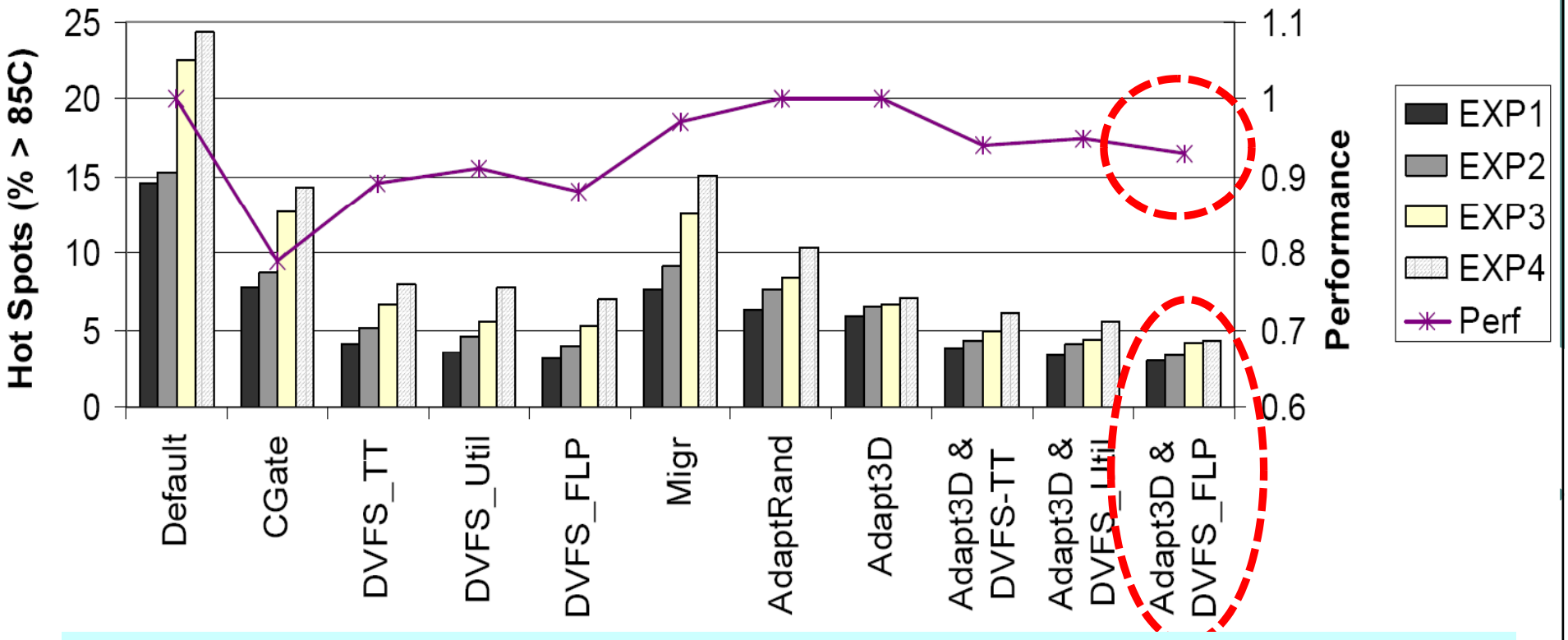


FEATURE	SIZE
Die thickness (1 stack)	0.15mm
Area/core	10mm^2
Area/L2 cache	19mm^2
Convection capacitance	140 J/K
Convection resistance	0.1 K/W
Interlayer material thickness	0.02mm
Interlayer material resistivity	0.25m K/W

[A. Coskun et al., DATE '09]

Thermal Management for 3D Chips: Adapt3D Results

- 3D thermal manager with fixed and variable flow rates
  - Proactive task sched., liquid cooling, floorplan-aware DVFS



Promising figures for thermal control in 3D-MPSoCs

[A. Coskun et al., DATE '09,VLSI-SoC '09]

Key References and Bibliography

- Thermal modeling and FPGA-based emulation
  - "**HW-SW Emulation Framework for Temperature-Aware Design in MPSoCs**", David Atienza, et al. *ACM Trans. on Design Automation for Embedded Systems (TODAES)*, Vol. 12, Nr. 3, pp. 1–26, August 2007.
  - "**Emulation-Based Transient Thermal Modeling of 2D/3D Systems-on-Chip with Active Cooling**", David Atienza, *Proc. of the 15th IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC '09)*, Belgium, October, 2009.
- Thermal management for 3D MPSoCs
  - "**Dynamic Thermal Management in 3D Multicore Architectures**", Ayse K. Coskun, et al., *Proc. of Design, Automation and Test in Europe (DATE '09)*, France, April 2009.
  - "**Modeling and Dynamic Management of 3D Multicore Systems with Liquid Cooling**", Ayse K. Coskun, et al., *Proc. of 17th Annual IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC '09)*, Brazil, October 2009.
  - "**Through Silicon Via-Based Grid for Thermal Control in 3D Chips**", Jose L. Ayala, et al., *Proc. of the 4th International ICST Conference on Nano-Networks (Nano-Net '09)*, Switzerland, October 2009.

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QUESTIONS ?