Real-Time Dynamic Voltage Hopping on MPSoCs

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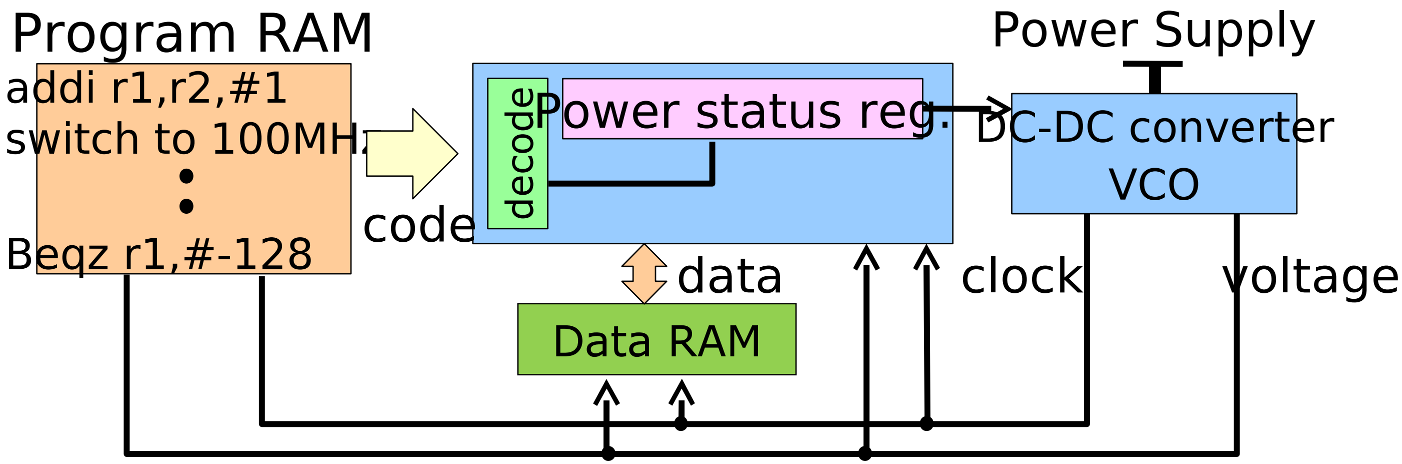
Background

- Low Power / Low Energy
  - Growth of portable electronics market
- Peak Performance
  - Growth of real-time applications

- Scalability and adaptability
  - Energy saving without losing the peak performance
- Real-time DVS on a multi-core processor

DVS Processor

- Processor can dynamically change its clock frequency
- Programmers can specify the clock frequency using an I/O instruction
- The operating voltage is adjusted to the minimum value which guarantees correct operations of the processor

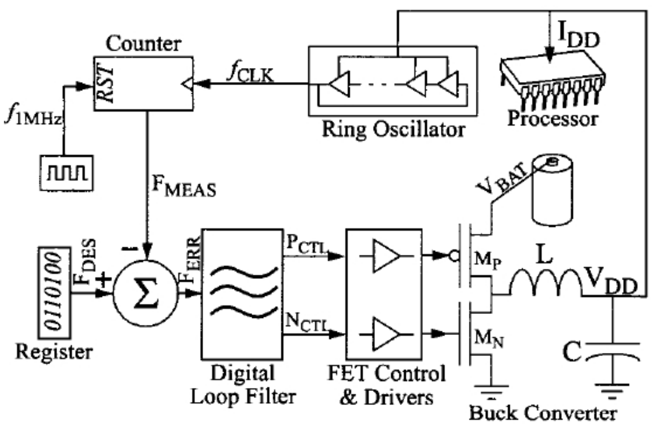


T. Ishihara and H. Yasuura, "Voltage Scheduling Problem for Dynamically Variable Voltage Processor," in Proc. of ISLPED'98, pp.197-202, Aug., 1998.

DVS Pros and Cons

- Pros
  - Quadratic reduction of energy consumption
- Cons
  - Low performance at low operatin
  - Large overhead of DC-DC conv

This prevents real-time control of DVS processors



T. Burd and R. Brodersen, “Design Issues for Dynamic Voltage Scaling”, ISLPED 2000.

$$t_{TRAN} = \frac{2 \cdot C}{I_{MAX}} \cdot |V_{DD1} - V_{DD2}|$$

$$E_{TRAN} = (1-\eta) \cdot C \cdot |V_{DD1}^2 - V_{DD2}^2|$$

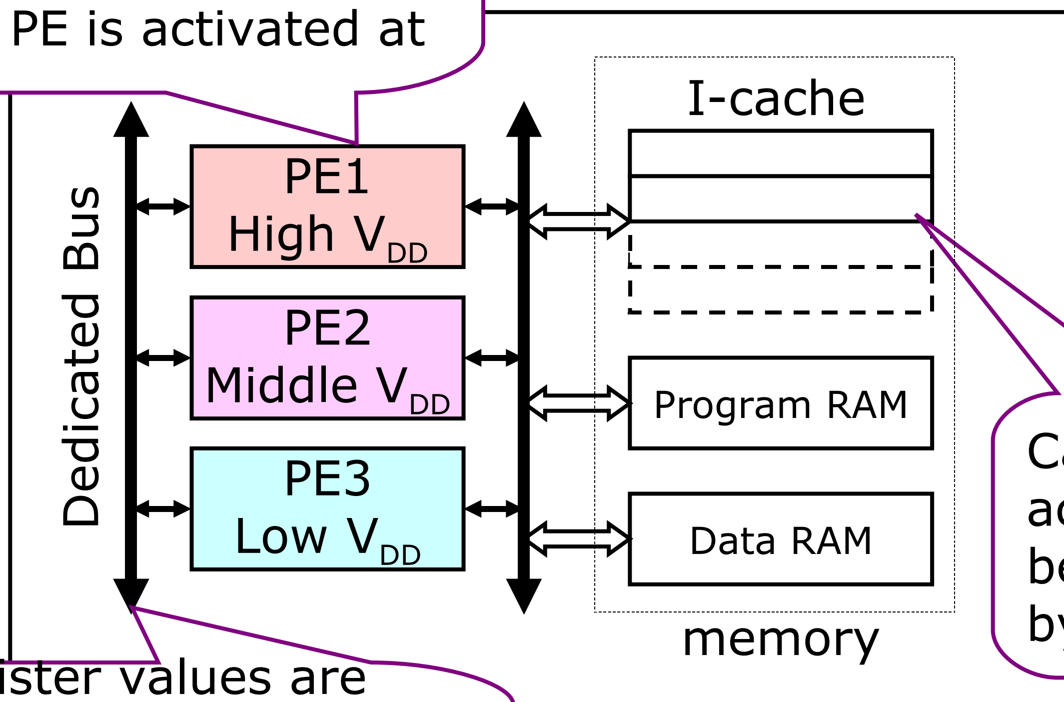
Typically 0.9

- $C=100\mu F$ 、 $I_{MAX}=1A$
- $V_{DD1}=1.0$ 、 $V_{DD2}=0.68$
- $t_{TRAN}=64\mu s$, $E_{TRAN}=4.6\mu J$

Multi-Performance Processor (1/2)

- PEs have the same ISA
- Differ in their clock speeds and energy consumptions
- A single PE is activated at a time

Not an ILP processor nor a multi-core processor

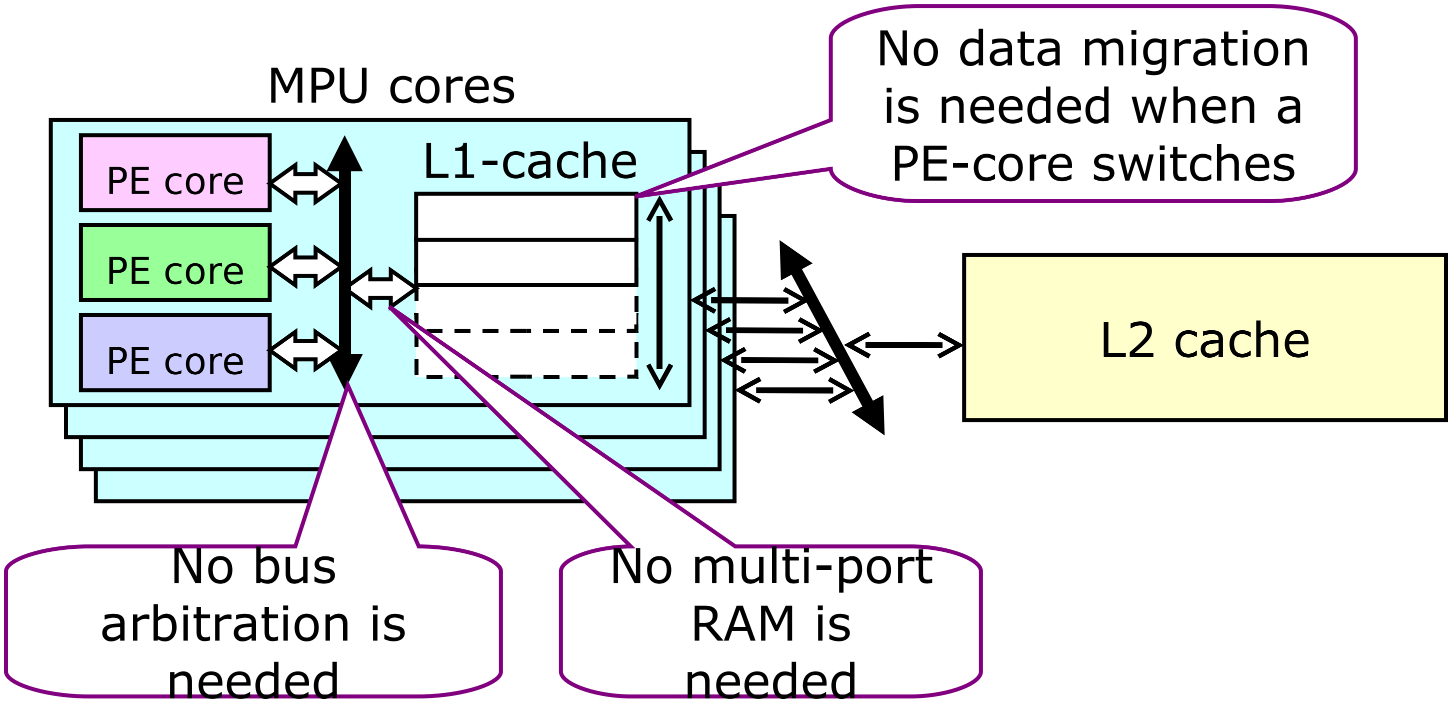


Cache ways activated can be specified by program

Internal register values are transferred through a dedicated bus or a stack located in a data RAM before switching PEs

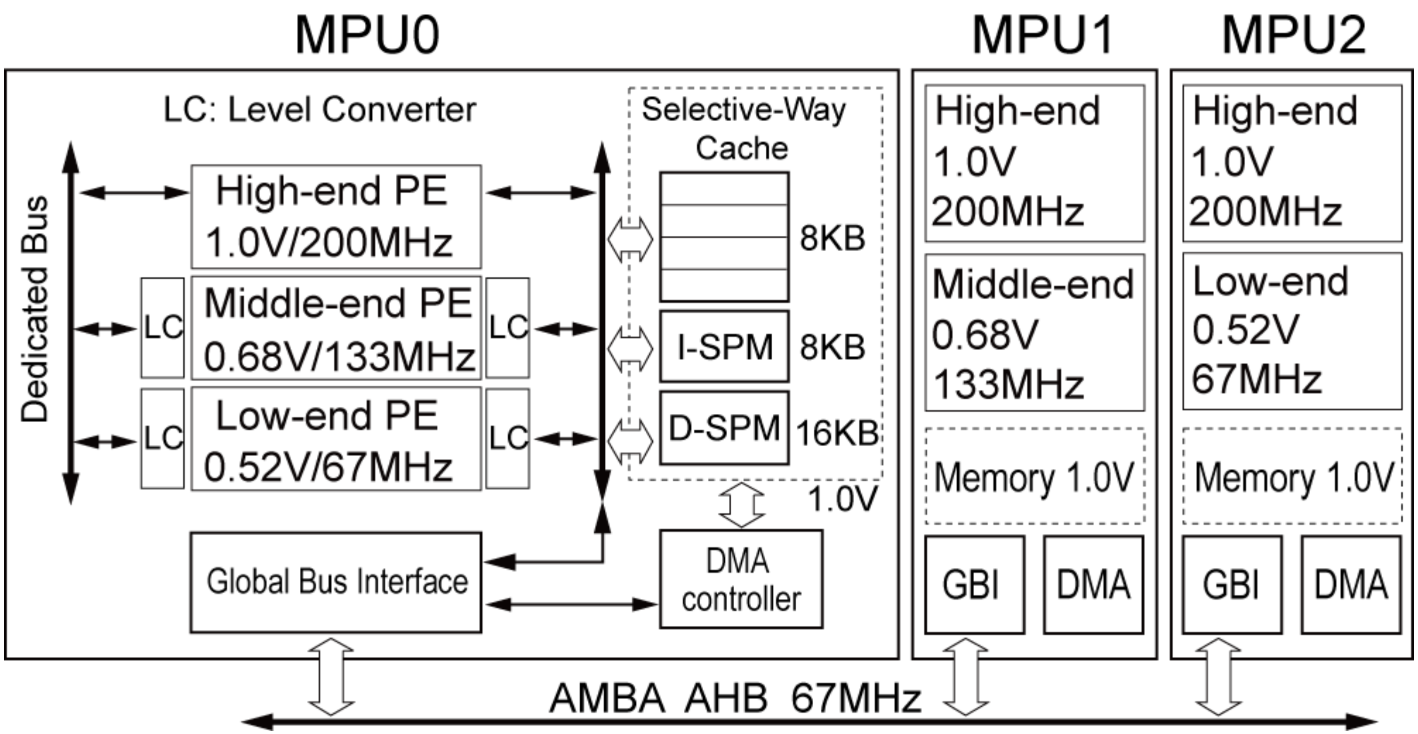
Multi-Performance Processor (2/2)

- Inter MPU cores: multiple MPU cores run concurrently
- Intra MPU core: a single PE core runs alternatively



Overview of Prototype

- Based on Media embedded Processor (MeP) originally developed by Toshiba
- Designed with commercial 90nm process technology



Synthesis Flow

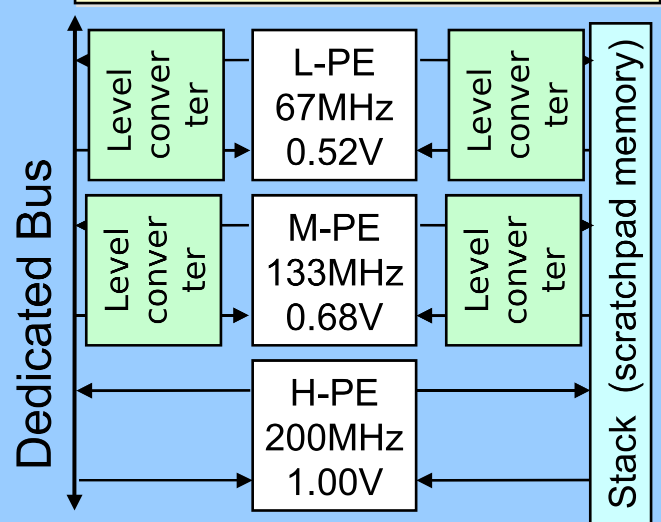
- Characterize cells using different voltages
  - 1.0V, 0.75V, 0.72V, 0.7V, 0.68V, 0.55V, 0.52V, 0.5V
- Determine clock frequency of H-PE
  - 200MHz with 1.0V
- Determine bus clock frequency
  - 66MHz which is a quotient of 200MHz
- Determine clock speed and V_{DD} of L-PE
  - 66MHz@0.52V which minimizes the energy of L-PE
- Determine clock speed and V_{DD} of M-PE
  - 133MHz@0.68V which minimizes the energy of M-PE

Comparison with DVS (1/2)

- 15 GP registers are transferred through stack
- 16 SP registers are transferred through dedicated bus
- The other registers like pipeline registers are flushed

Ours

Transition time	*1μs*
Energy overhead	*13nJ*



Commercial DVS processor

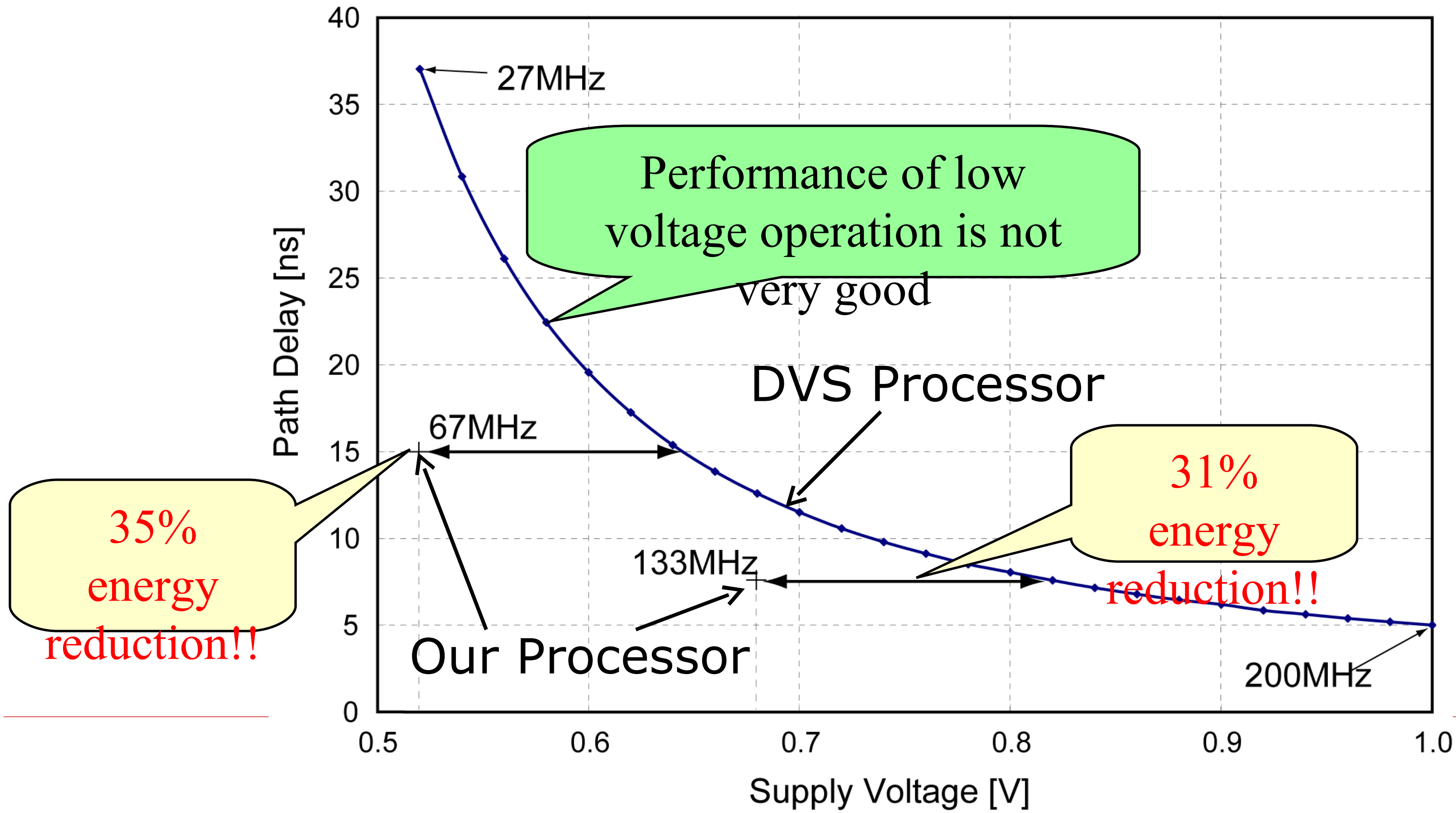
Processor	RTOS	Transition time
AMD Mobile K6 [1]	PowerNow!	200 μsec
StrongARM SA-2 [2]	Embedded Linux	150 μsec
Transmeta Crusoe [3]	LongRun	> 20 μsec

~10 μJ energy overhead is involved

[1] AMD, “AMD PowerNow! Technology Dynamically Manages Power and Performance”
[2] “Compaq iPAQ H3600 hardware design specification ver.0.2f”, http://www.handhelds.org/Compaq/iPAQH3600/iPA
[3] M. Fleischmann, “Reducing x86 operating power through LongRun” IEEE 12th Hot Chips Symposium, August 15, 2000

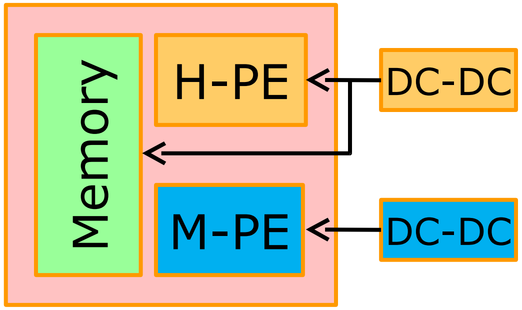
Comparison with DVS (2/2)

- Extract a critical path from our 1.0V design
- Measure the delay of the path using HSPICE for different operating voltages



MPP Pros and Cons

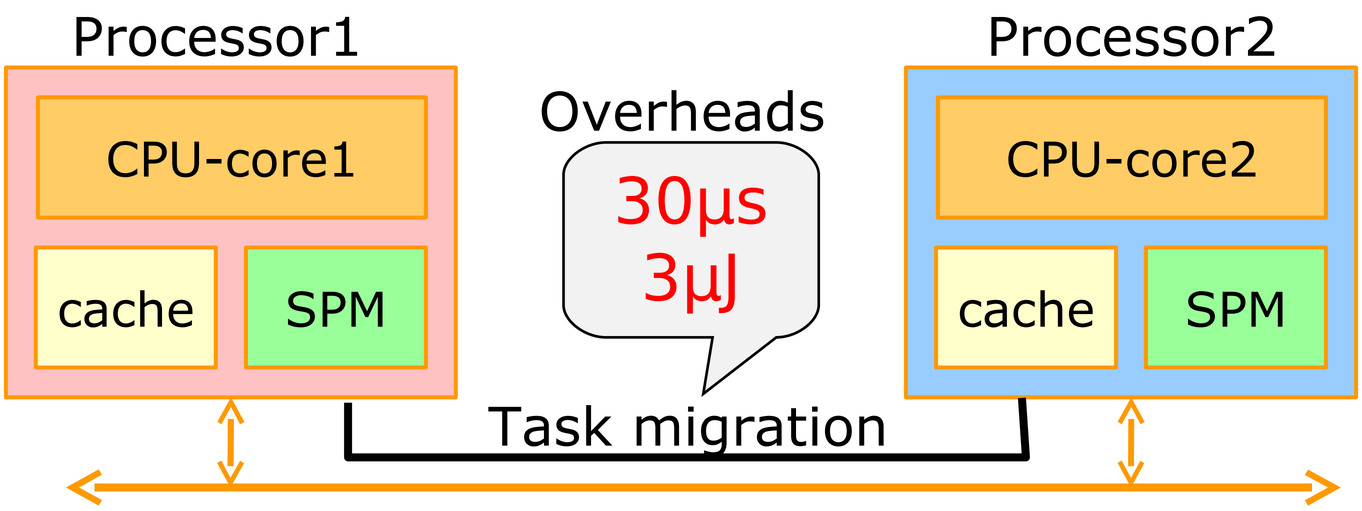
- Pros
  - Low transition overhead
    - Two orders of magnitude less than that of DVS
  - Higher performance at low operating voltage
    - Each PE core is optimized for the target supply voltage
- Cons
  - Large area overhead
    - Limited number of clock speeds
  - Need multiple voltage sources



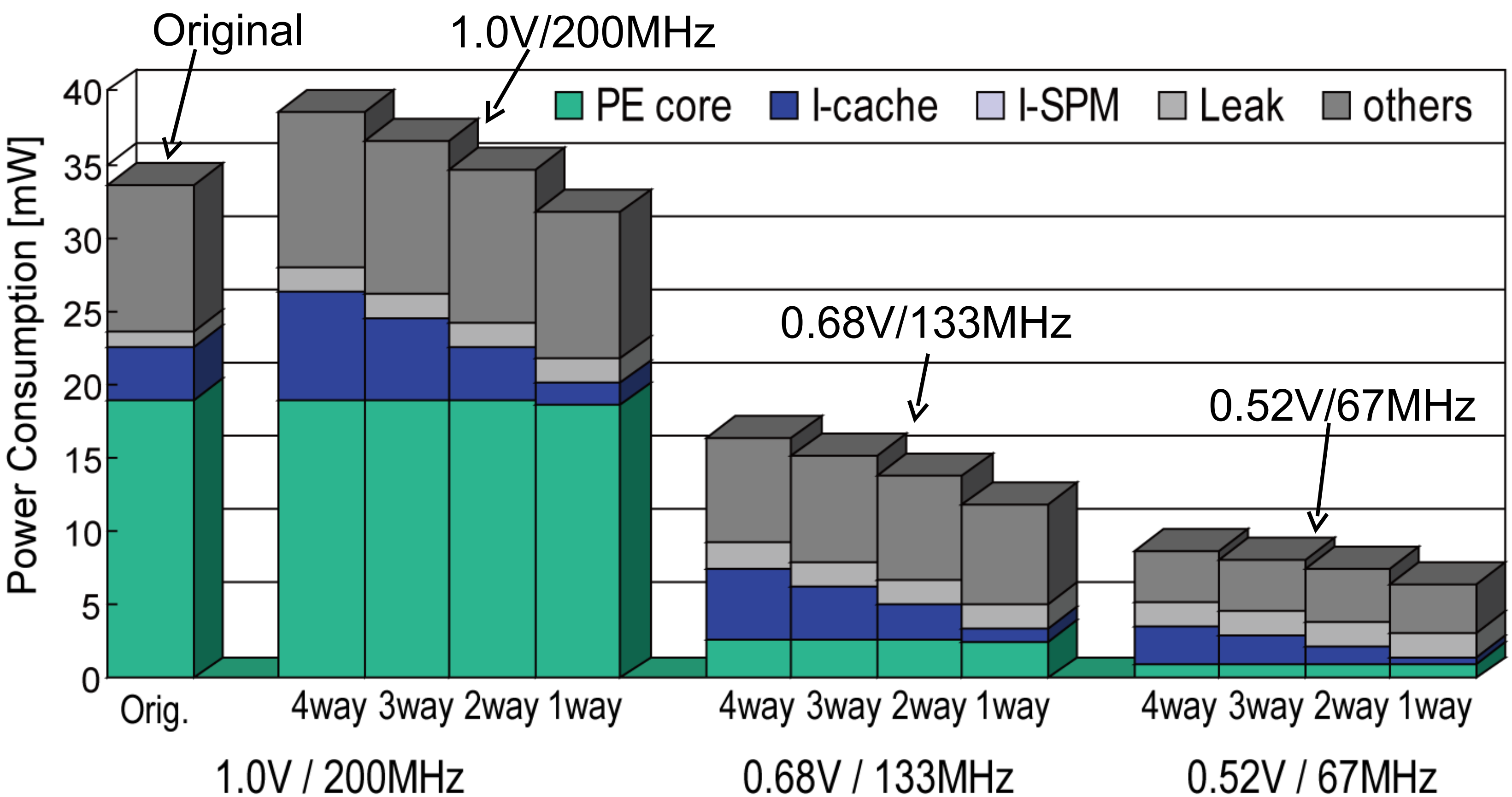
Comparison with CMP

- Heterogeneous chip multi-processor (CMP)
- Processor1 runs faster and consumes higher energy than Processor2

Task migration can be a better solution if it reduces the energy w/o violating a real-time constraint



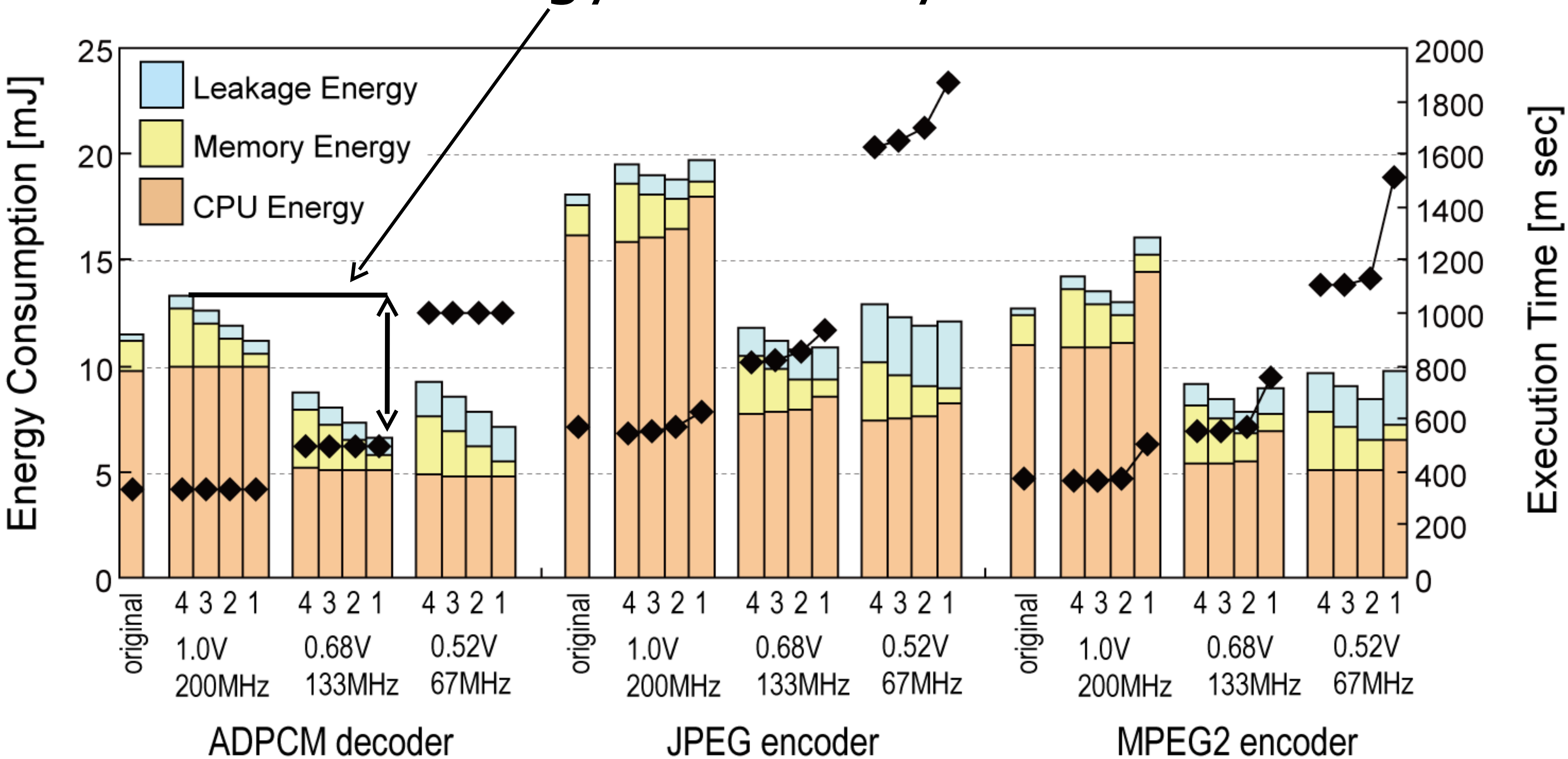
Power Results of MPEG2 encode



- Stack is placed in the data scratchpad memory
- HW configuration is fixed before entering the main routine

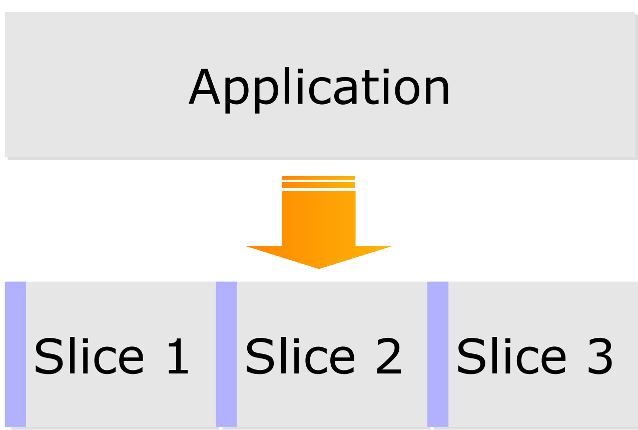
Energy and Execution Time

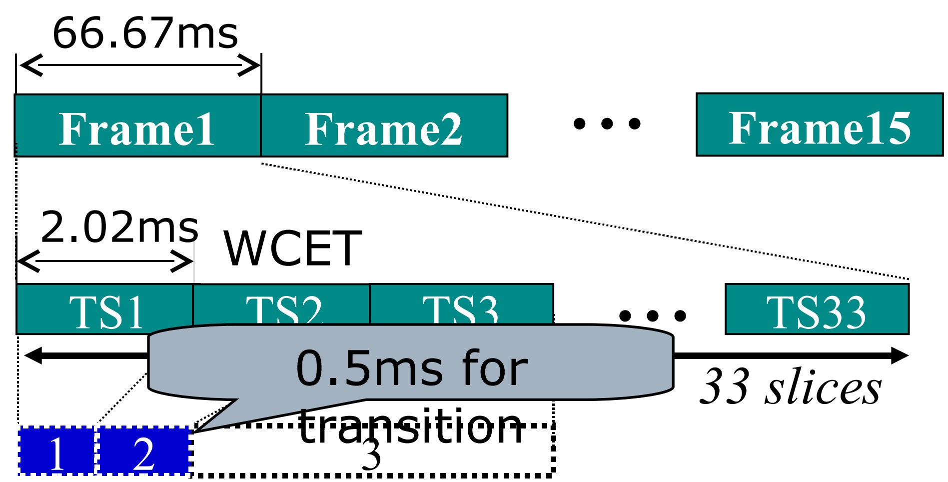
2x energy scalability



Application of DVS Processor

- Motivation
  - Most tasks complete much earlier than their WCET
- Approach (for periodical tasks only)
  - Divide a 1-frame video encoding task into 33 slices
  - Exploit slack time of previous slices in the current slice

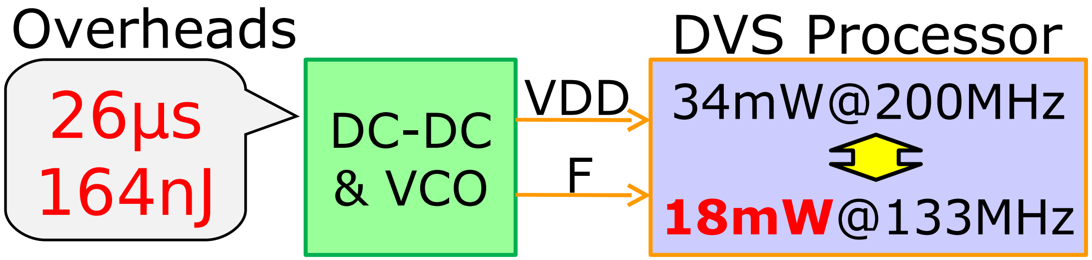




S. Lee and T. Sakurai, "Run-time voltage hopping for low-power real-time systems," in Proc. Asia South Pacific Design Automation Conference., Jan. 2000, pp. 381-386.

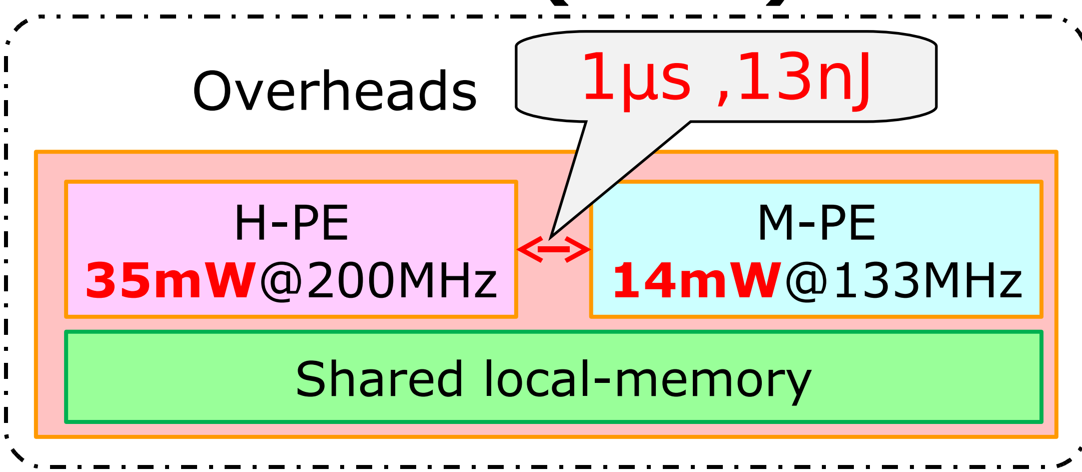
Experiments

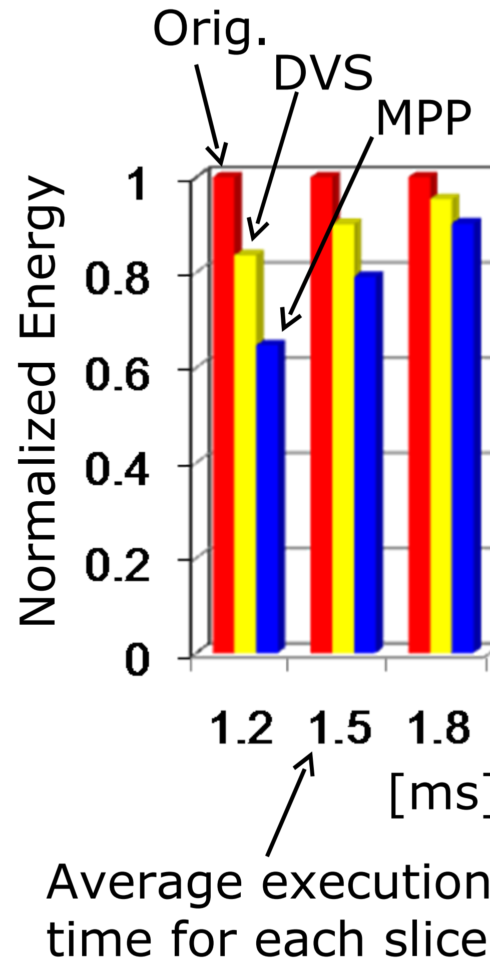
DVS



T. Burd and R. Brodersen, "Design Issues for Dynamic Voltage Scaling", ISLPED 2000.

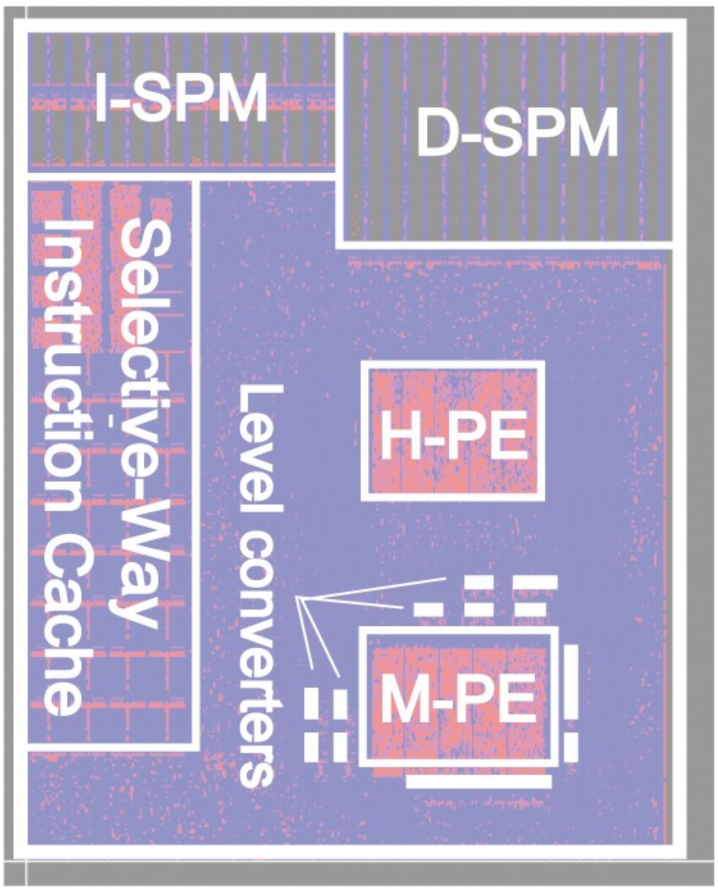
MPP (ours)





Layout Image of MPU-core1

Designed with commercial 90nm CMOS technology



D-SPM	0.62mm²	15.0%
I-SPM	0.40mm²	9.5%
I-Cache	0.74mm²	17.5%
High-end PE	0.19mm²	4.5%
Middle-end PE	0.21mm²	5.0%
Others	2.07mm²	48.5%
Total	4.23mm²	100%

Summary

- Small overhead compared with DVS
  - Transition time :   100x smaller
  - Transition Energy :   1000x smaller
- More energy efficient at low voltage
  - Clock frequency :   30% more efficient
- Large area overhead
  - ~25% area overhead

Thank you!!

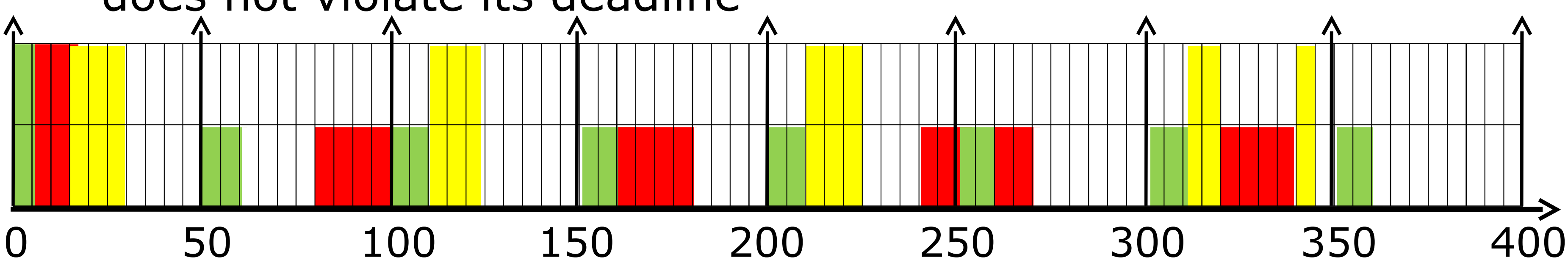
Real-Time Voltage Hopping (1/2)

ACET: Average Case Execution Time   WCET: Worst Case Execution Time

	Period	Deadline	Priority	ACET1 (Energy)	WCET1	ACET2 (Energy)	WCET2
T1	50us	50us	1	5us (200nJ)	10us	10us (100nJ)	20us
T2	80us	80us	2	10 us (400nJ)	20us	20 us (200nJ)	40us
T3	100us	100us	3	15us (600nJ)	40us	30 us (300nJ)	80us

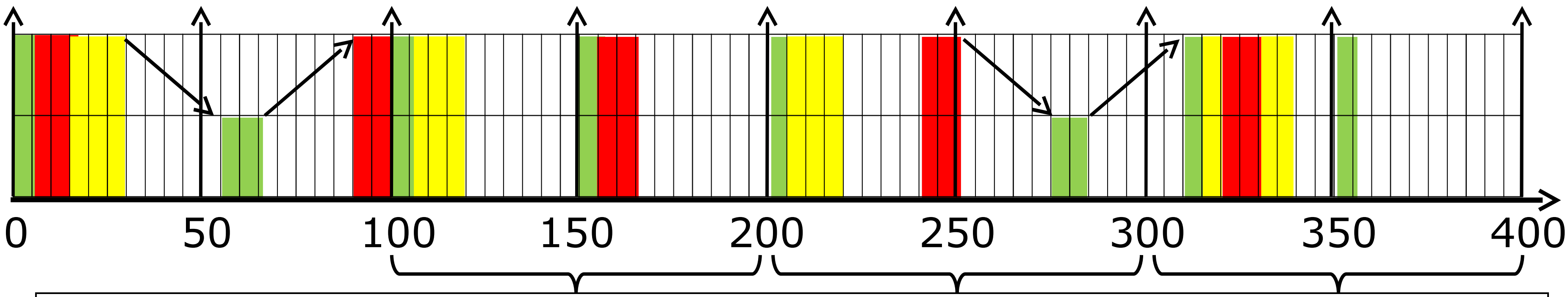
High speed (ACET1, WCET1)   Low speed (ACET2, WCET2)

- Assumption : CPU speed can be switched upon task switches
- Strategy : CPU speed is lowered only if any succeeding task does not violate its deadline



Real-Time Voltage Hopping (2/2)

Conventional DVS consumes 6.46mJ (6.0mJ)



T1, T2, and T3 run twice, once and once in every 100us → WCET is 80us

Our MPP consumes 4.62mJ (23% reduction)