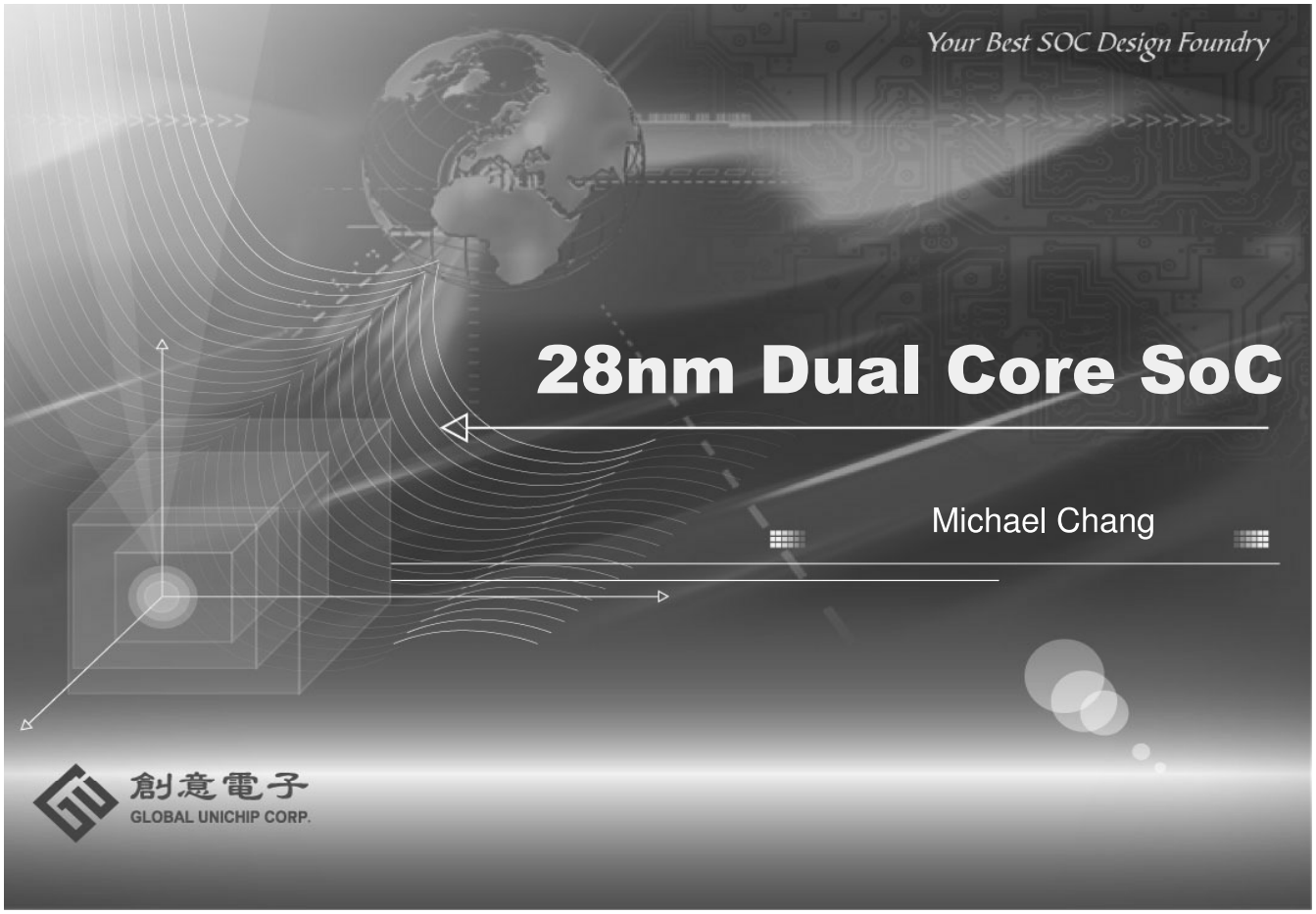

Agenda

- SoC Specification
- CPU core Hardening
- Memory Interface Design
- Co-Simulation

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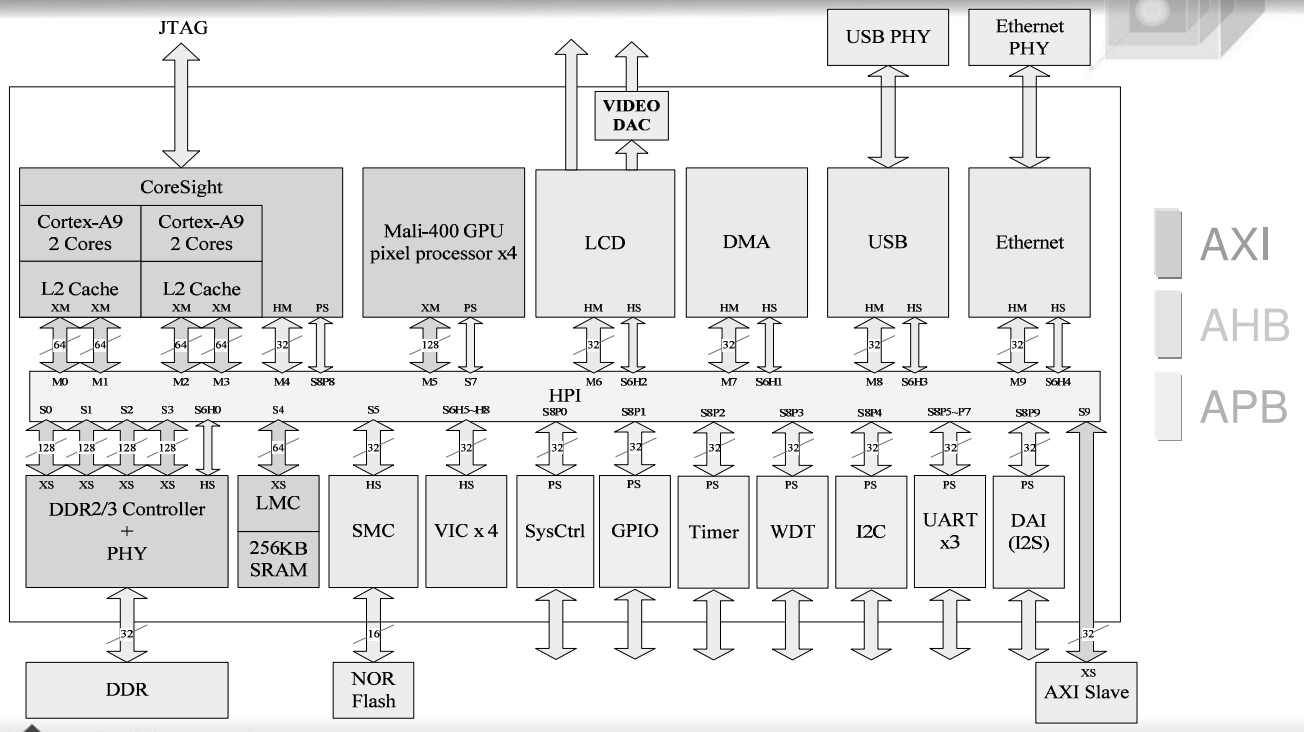
SoC Block Diagram



Specification- CPU

- **CortexA9 MP core**
  - 2 GHz Dual Core
  - 32KB/32KB I/D Cache
  - CoreSight
- **L2 Cache controller Features**
  - Prime cell PL310 with 256KB SRAM
  - Configurations:
    - Cache way size: 32KB
    - Number of cache ways: 8 ways

Specification- GPU

- **Mali400 Features**
  - 4 pixel processors
    (up to 1000MP/s)
  - Power management Unit
  - 32 KB L2 cache
  - 128 bits Data Bus width
  - Compatible with
    - OpenGL-ES2.0
    - OpenGL-ES1.1
    - OpenVG 1.1

Specification- DDR2/DDR3

- **Memory Interface**
  - Support DDR2 and DDR3 SDRAM
  - DDR2 operation speed is up to 1066Mbps
  - DDR3 operation speed is up to 2133Mbps
  - Memory data width: 32 bit

Display Interface

- **Display Frame Buffer**
  - Support image format, YCbCr 422
  - Support image format, RGB 1/2/4/8/16/24 bpp (bit per pixel)
  - Built-in YUV to RGB color space converter
  - Support single panel mono/color STN display with 4/8-bit interface
  - Support color TFT display with 12/18/24-bit interface
  - Resolution programmable up to 1920 x 1080
  - 256 entry, 24 bit user-defined palette table
  - Dither algorithm to enhance color resolution
  - Programmable polarity for panel control signals

Peripherals

- **USB OTG Features**
  - Compliant with the On-The-Go Supplement to the USB2.0 specification Revision 1.0a
- **UART Features**
  - Function compatible to the standard 16550 UART interface
- **Digital Audio Interface (DAI) Features**
  - Support multiple digital audio interfaces formats
    - Support I2S, MSB extended, Left-justified, Right-justified data format
    - Software programmable word length, support 1 to 24 valid bits/word
    - Software programmable word ignored bits, support 0~31 bits
    - Support 1~24 bits/word packet mode
  - Support for Direct Memory Access (DMA)
- **Ethernet 10/100Mbps MAC**
  - Compliant with IEEE 802.3 standard
  - Full/Half Duplex capability
  - Support IEEE 802.1Q VLAN mode

Other features

- **Build-in 256KB internal SRAM for programmer usage**
- **Support LCD touch panel**
- **Build-in Flash memory interface for system boot up**
- **Build-in GPIO, Timer, WDT and DMA basic peripherals**

Agenda

- SoC Specification
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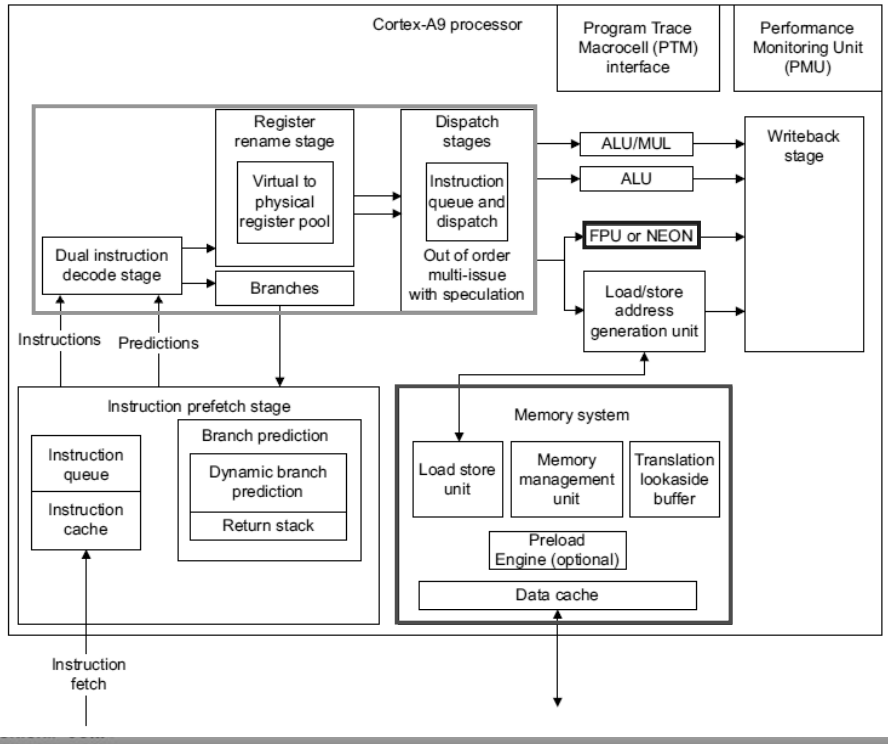
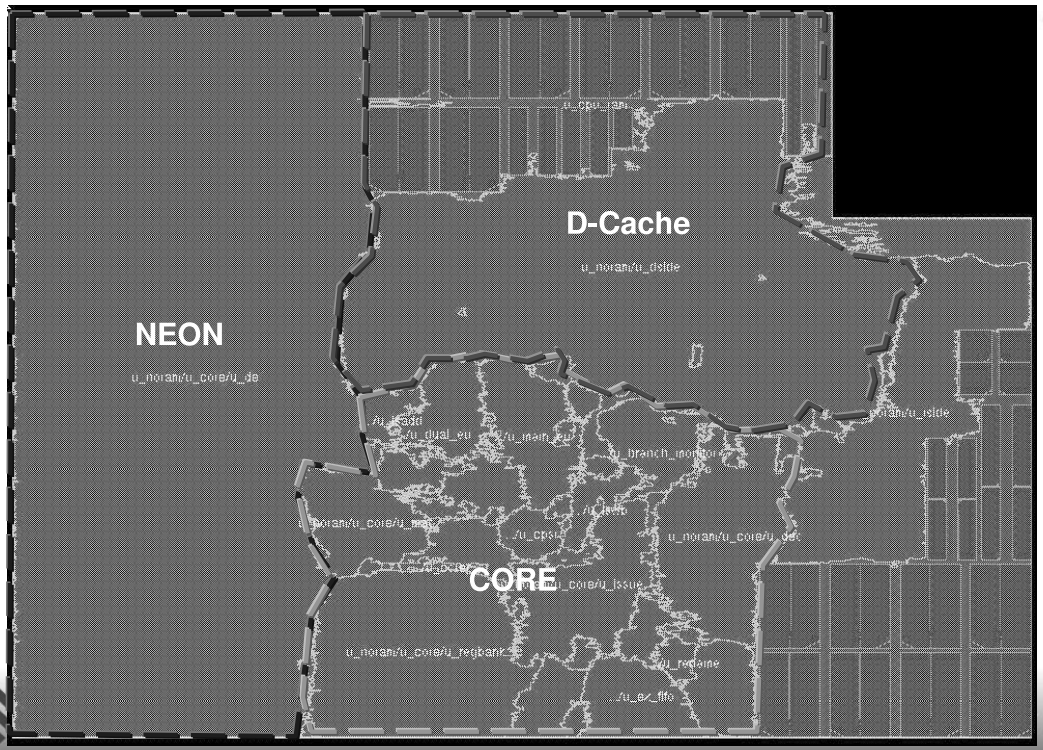
EDA tool

- **EDA tools used for Hardening**
  - Frontend
    - Synopsys DCG
    - Create close correlation with ICC to further enhance timing
  - Backend
    - Synopsys ICC
    - Rubix for CTS and post-CTS optimization
  - Sign-off
    - Synopsys PT

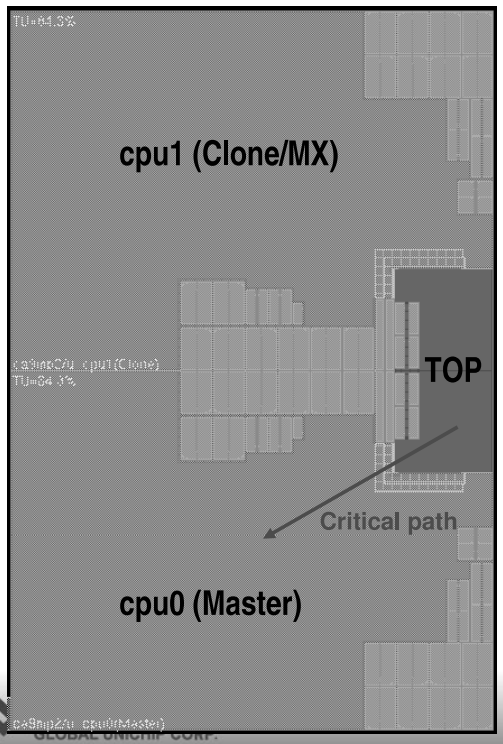
Block diagram of falcon_cpu



falcon_cpu



Top level critical paths analysis



- **Critical path analysis**
  - CPU level boundary not well optimized. (Timing budgeting)
  - CPU clock latency prediction is not accurate.
  - Optimization limitation (can't optimize the cells within CPU level during Top optimization)

Improve Top level timing

- **Improve Top level timing**
  - Optimize timing budgeting between SCU and Falcon
  - Predict precise clock tree latency in Falcon
  - Place SCU related FF in the Falcon boundary
  - SCU should be faster than Falcon
  - The critical path should be in Falcon
  - The CA9 MP timing should be limited by Falcon speed

Falcon level critical paths analysis

- **TOP 5K critical paths in falcon_cpu**
  1. dside module
  2. core/NEON module
  3. core other modules
  4. cpu_ram
     - Timing estimated at cworst WCL corner

- **Critical path analysis**
  - Critical path is R2R path, not memory related paths
  - The most critical paths are located at dside module

Improve Falcon and boundary timing

- **Improve Falcon timing**
  - Create correlation between DC and ICC
  - Analyze the critical-path groups seen in ICC
  - Fine tune constraint to further enhance critical paths in DC
  - Generate qualified netlist with better timing and correlation with encounter

- **Improve boundary timing**
  - To make high-speed I/O ports ease for chip integration and will not degrade the CA9 speed
  - Do CTS for high-fanout and full-speed input ports
  - Carefully place related FF for full-speed I/O ports
  - Carefully arrange the port location for high speed I/O ports

Agenda

- SoC Specification
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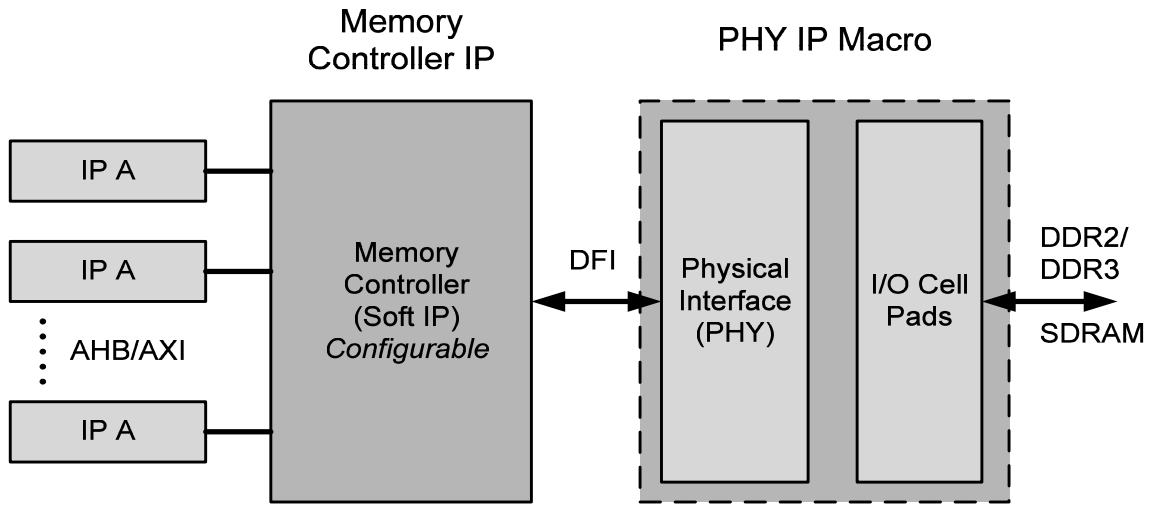
Memory Interface Design

- **Block diagram in system**



High Speed PHY Macro

Timing Budget

- System designer need to break timing budget into individual parts in DDRPHY

tREF clock	1250			
	unit: ps	jitter/skew	setup time (ps)	hold time (ps)
Transmitter Components	DFF	skew	5	5
	BUFFER	skew	2	2
	MUX	skew	2	2
	local clock tree	skew	5	5
	local clock tree	jitter	5	5
	dll	jitter	50	50
	DQ IO duty	skew	5	5
	DQ IO C2C	jitter	20	20
	SSO push out	jitter	50	20
Total transmitter uncertainty			144	114
Inter-connection	PCB cross talk		10	10
	ISI		5	5
	Package and substrate	skew	8	8
	PCB	skew	10	10
Receiver components (DRAM)	tDS/tDH (1600mpbs) base AC150		10	45
	tDS/tDH (1600mpbs) delta		75	50
	tDS/tDH (1600mpbs) total		85	95
	Total Worst Case Jitter + Skews		406	356
	Data UI		625	
	Margin Under Absolute WC		-93.5	-43.5
	Margin Under typical case		121.0017	126.7633
	Margin Under guard banded		13.75084	41.63165

High Speed PHY Macro

PHY Macro Components

- IO (so called SSTL-15)
- PLL/DLL(source synchronous DQS/DQ)
- Logic (Ser/De-Ser, DFT…)
- PVT (calibration)

High Speed PHY Macro

- **To accommodate low cost and provide high performance DDR IP, per-bit de-skewing technology need to be used to eliminate the following skew and limit the total skew to 30ps**
  - Internal Clock Skew
  - Internal Circuit Routing Skew
  - Package Skew
  - PCB Skew

DDR3 Interface Functional Highlight(1)

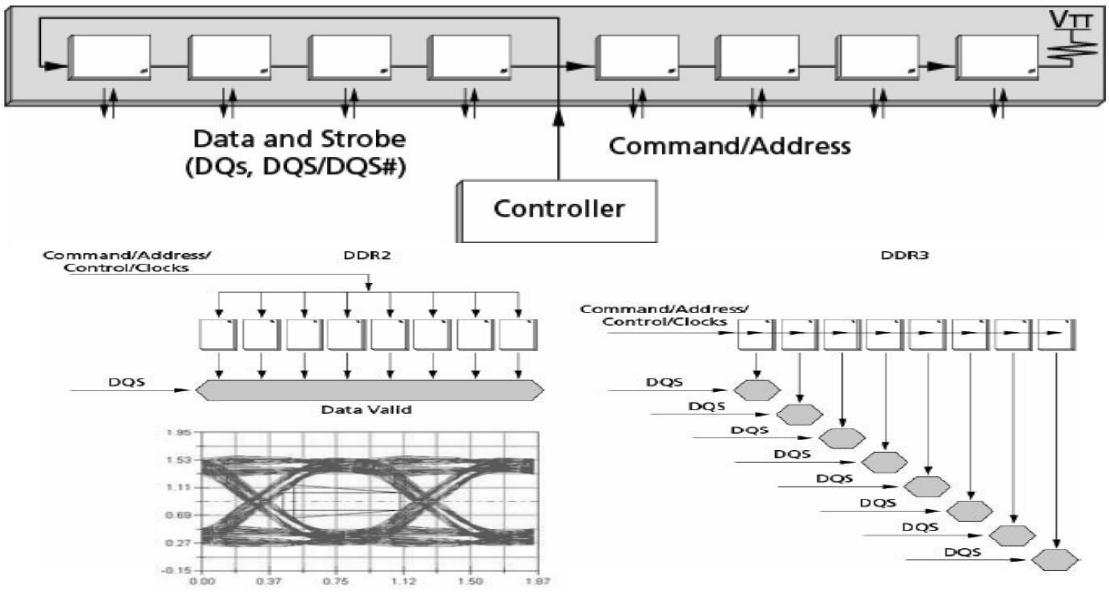
- **Self calibration**
  - Through a ZQ pin to calibrate the accurate ODT (on die terminator) and OCD (off chip driver)
- **In DDR2, most of DDR chip use trimming to adjust OCD value**

DDR3 Interface Functional Highlight(2)

- **Dynamic ODT (On Die Terminator)**
  - ODT advantage
    - Dynamically turn on and off parallel terminator
    - Save power
      - Extra components cause leakage
    - Save cost
      - No extra components
  - ODT can change value on the fly without idle time in DDR3
    - It is applied in 2 DIMM module system
      - For the non-active device during write, with low-impedance terminator value
      - For the active device during write, with high-impedance terminator value

DDR3 Interface Functional Highlight(3)

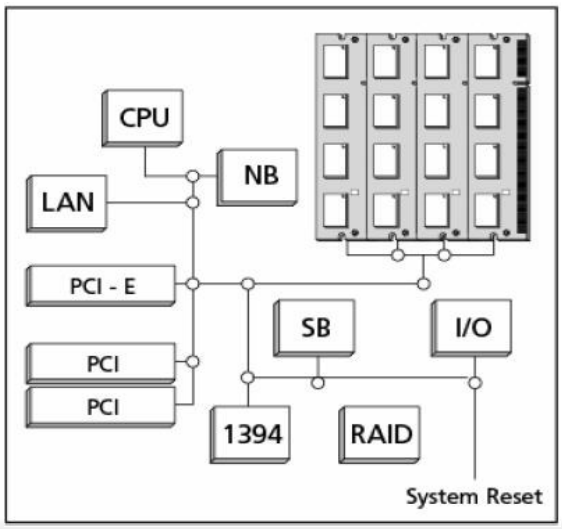
- **Write/ Read leveling**



Source: Micron

DDR3 Interface Functional Highlight(4)

- **Master Reset**
  - Improve system stability
  - Reduce controller burden to ensure no illegal command



Source: Micron

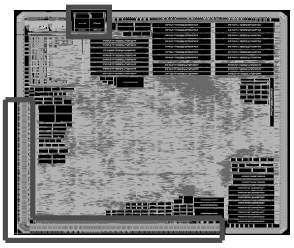
Agenda

- SoC Specification
- CPU core Hardening
- Memory Interface Design
- **Co-Simulation**

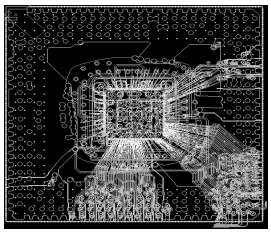
PI/SI

- **Power integrity and Signal integrity analysis are must be items for DDR system design**
- **A DDRPHY claims it could run up to 1.6Gbps does not mean anything**
- **Package and PCB design impact the timing budget seriously**

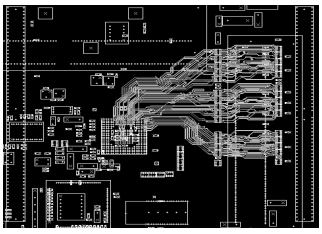
Chip model

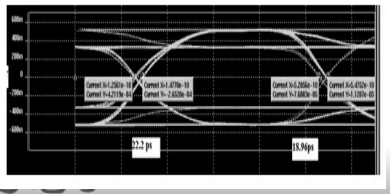


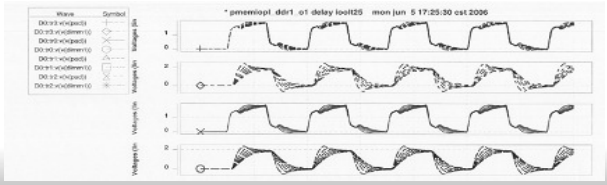
Package model



Board model





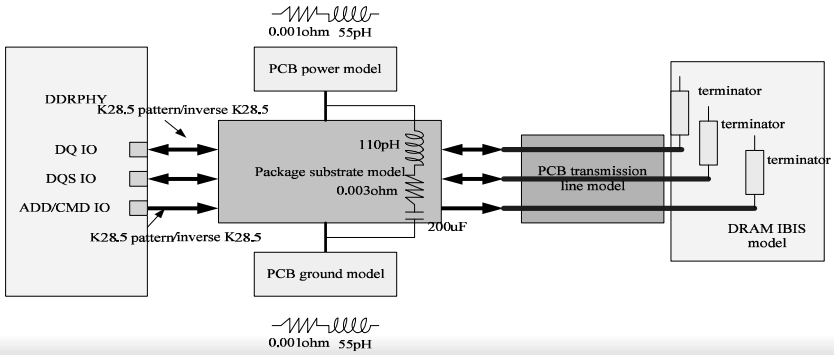


Power Integrity Analysis

- **PI (power integrity)**
  - Decoupling capacitor adding could lower the impedance in PI simulation
    - Decoupling capacitor need to be put as close to circuit as possible
    - On package decap
      - Capacitance size larger but with substrate inductance from die
    - On die decap
      - Capacitance size smaller but with very small inductance
  - How to optimize the usage of two kinds of decap
    - With flexible decap added on DDRPHY IP could optimize the package design flow in adding decap

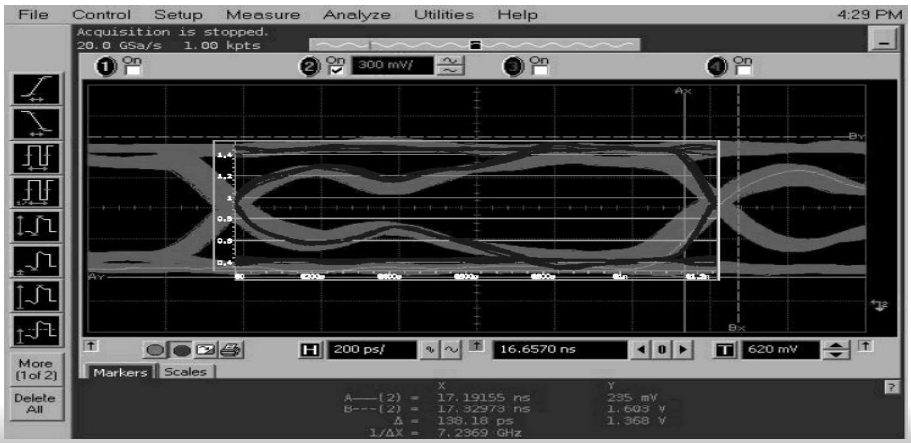
Signal Integrity Analysis

- **Eye Diagram**
  - The final sign-off of the DDRPHY system will be eye-diagram, which contains the following information
    - SSO
    - Cross-talk
    - ISI
    - IO duty
    - reflection



Signal Integrity Analysis

- **Iteration**
  - Model correctness will decide the accuracy of simulation result
    - PCB
    - Package
    - IO
  - Iteration on the correlation of simulation result and measurement takes a long cycle and timing consuming



Achieve 2133Mbps

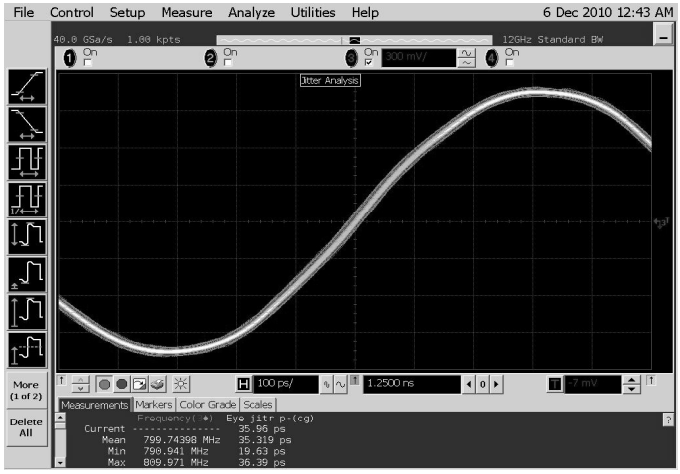
- **DDR3 maximum speed is 2133Mbps**
  - UI = 468.8ps compared with UI =625ps when operating in 1600mbps. Difference = 156.2ps
- **There is no design margin in such high speed operation**
- **How to "squeeze" the source synchronous system for the extra shrinking 156ps from 1600Mbps data eye , that is a big challenge**

Achieve 2133Mbps

- **DDR3 2133Mbps**
  - From the data eye simulation of 1600Mbps, the setup time + hold time = 418ps, which means the following items take UI(625ps) -418ps-25ps (dqs skew + jitter) = 182ps
    - SSO
    - Cross-talk
    - ISI
    - IO duty
    - reflection
  - DDRPHY designer need to squeeze 100ps from 182ps and another 50ps from the other skew and jitter inside the PHY

Achieve 2133Mbps

- **DDR3 2133Mbps**
  - Every components in the system need to be designed very carefully
    - PCB
    - Package
    - IO
    - Impedance matching
    - Clock skew
    - PLL/DLL jitter



Thank you !

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