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THE NETWORK-ON-CHIP COMPANY

Interchip Link Technology

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MpSoC Conference, Beaune, France

July 6, 2011

Interchip Link Background

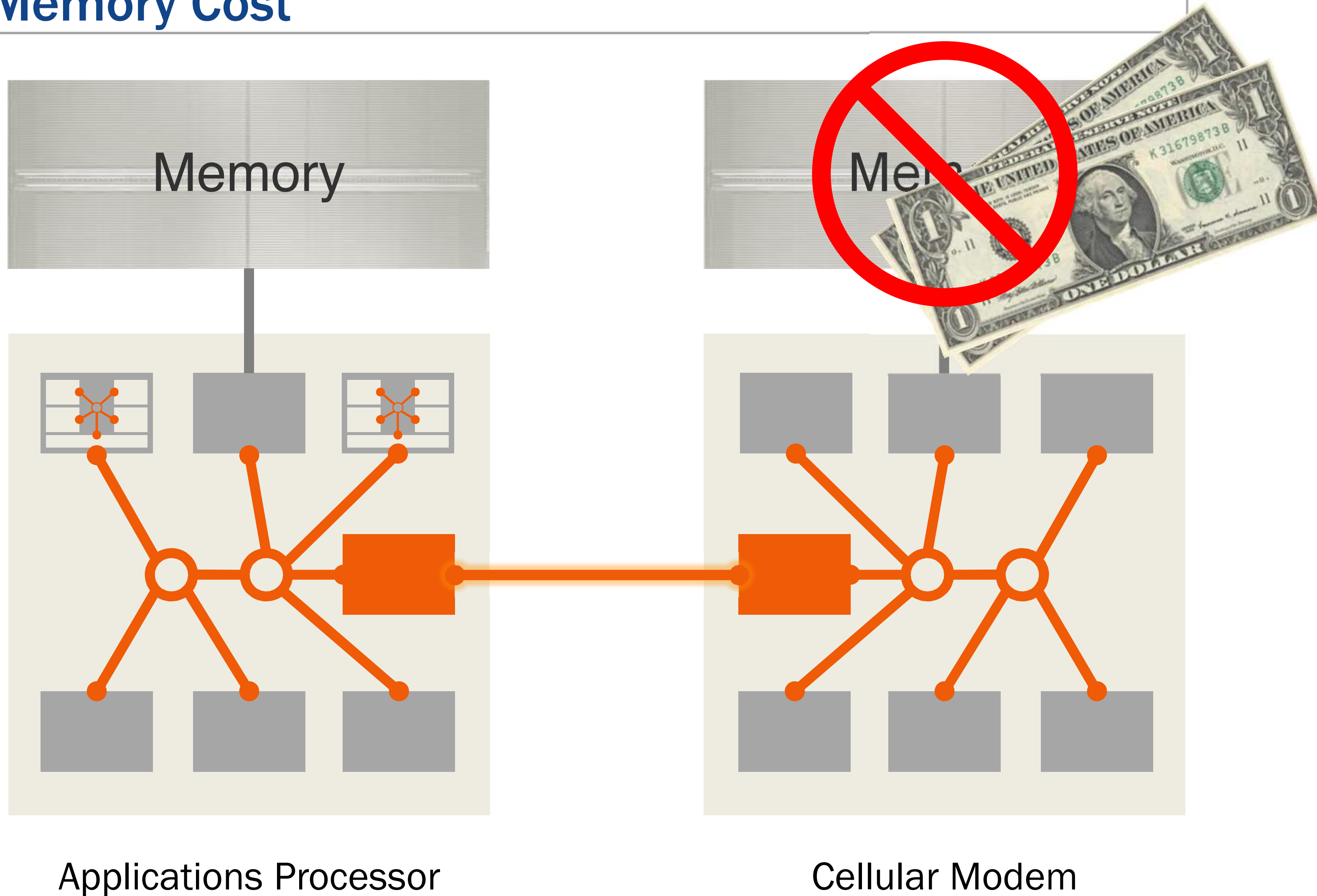
- Some functions belong on the same chip but others do not
  - High end modems and application processors
  - Multiple modem co-processors
  - Video co-processors
  - Analog and digital dies
  - Multiple FPGAs
  - Processors and FPGAs etc.

- How to effectively integrate communications between multiple dies
- **Answer: With Interchip link technology**

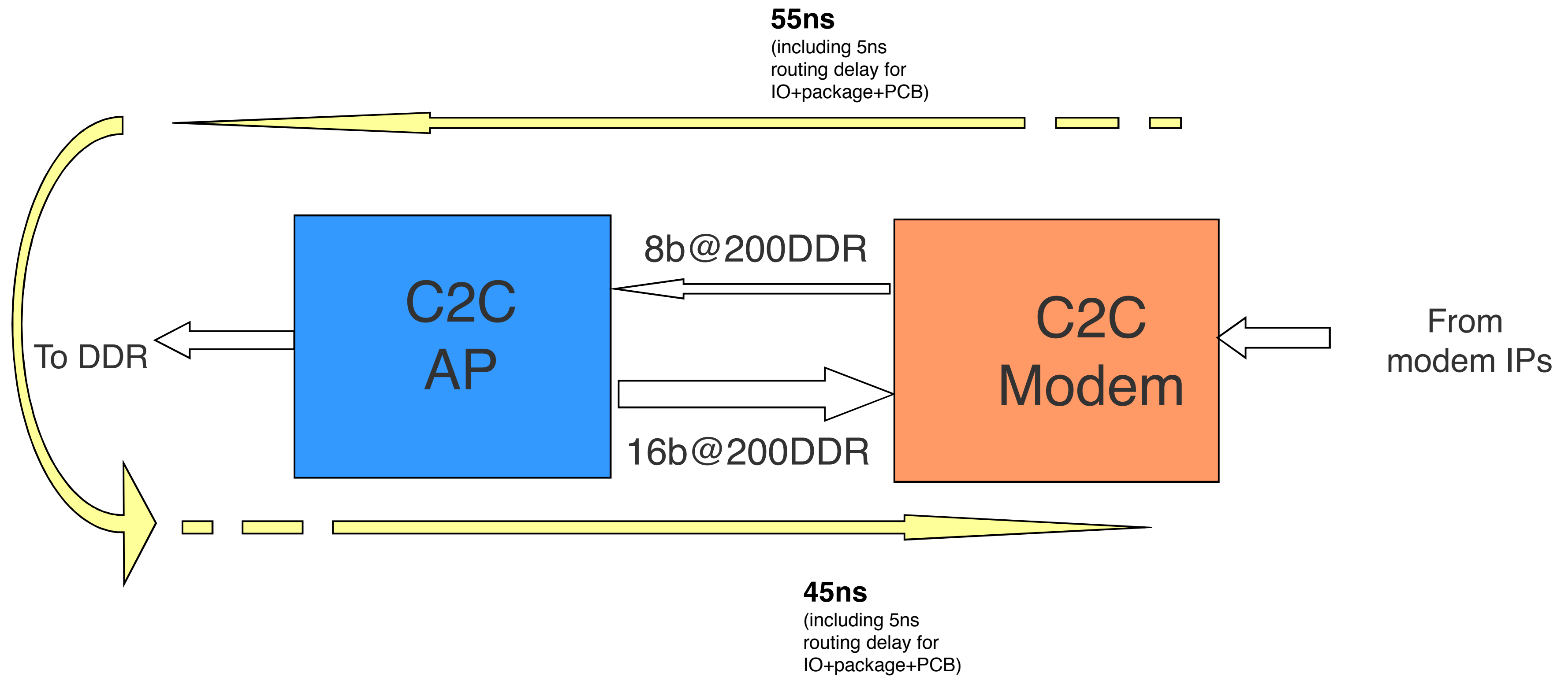
C2C comparison to other Interfaces

	C2C	PCIe	HIS	Unipro
Main Function	DRAM sharing between high performance processor SOC's for Mobile Platforms	Plug/Play system level peripheral networking	Application processor to cellular (modem) communications	Board level chips networking for mobile platforms
Tech Specification	Point to point bidirectional address mapped communication between SOC interconnects. Allows DRAM and SOC peripheral sharing between 2 devices	Full set of networking components (hosts, etc). Plug and play discovery, qos mechanisms	Point to point serialized communication	Multipoint based communication between several devices
Latency for a 32B burst	~100ns	>250ns	Slow in the ~us range	>150ns
PHY	Configurable pin count. DDR2 200MHZ (400 effective rate) pads. NO PHY NEEDED	PCIe serdes 2.5Gbs configurable number of lanes	4 LVCmos pins each direction. 200Mbps max	MIPI D PHY, 80MBps. Current 1Gbs and M PHY would enable 2.9 Gbs.
Size	100k gates excluding pads	>200kgates for transaction level end point. Also need additional area for PHY	TBD	Unknown except large variations depending on performance and flexibility operating point (number of connections)
Benefit compared to others	Optimized for low latency DRAM sharing. (cache refill performance) Uses standard DDR pads and no need for complex serdes technology and constraints. No set up necessary by embedded SW	S/W driver and OS support	Simple but low throughput and high latency	

Arteris FlexLLI™ Interchip Link Connects Dies & Saves on Memory Cost



C2C latency : total round trip 100ns



Traffic latency example for cache line refill

- no AP traffic : around 200ns (40cycles @200MHz).
- high AP traffic : around 300ns (60cycles @ 200MHz).

LPDDR1 @166MHz: (CPI 1.87 /278 MIPS)

-C2C, No AP traffic: -5.7%

-C2C, Heavy AP traffic: -10.8%

LPDDR1 @200MHz: (CPI 1.82 /286 MIPS)

-C2C, No AP traffic: -8.4%

-C2C, Heavy AP traffic: -13.3%

Two Interchip link IP Implementations

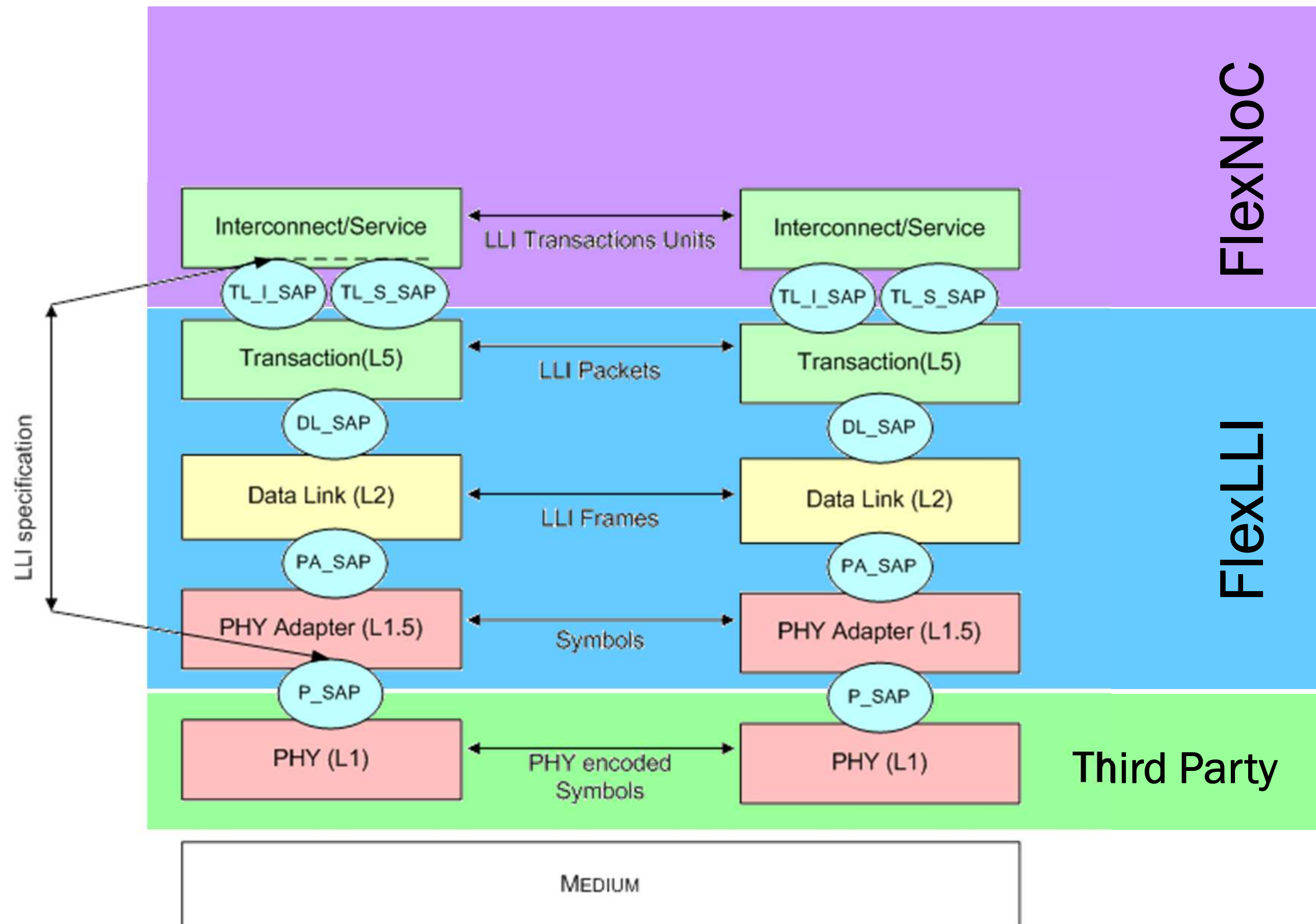
C2C™

- Available now
- No PHY required, DDR pads
- Roundtrip latency = 100ns
- 8 or 16 Tx pads / 8 or 16 Rx pads or 32 pins
- 100K gates
- Users: 8 baseband modem & 4 application processor vendors - with others considering

MIPI LLI → Arteris FlexLLI™

- Early LLI shipped 4Q10, FlexLLI available upon LLI spec. release
- LLI is a digital controller, MIPI M-PHY required
- Round trip latency ~ 80ns
- 2 pins per lane up to 6 lanes or 12 pins
- < 100K gates plus M-Phy
- Users: Early LLI on two application processor platforms

MIPI LLI Layer Structure



Conclusion

- Real Inter-chip eco-system emerging
- Lowering cost of inter-die communications by ~$2/phone
- Lowering board space by saving space of memory chip
- Two efficient interchip link approaches available
  1. Through DDR pads
  2. Through an M-Phy
  3. Future; through silicon – Wide I/O
- Viable alternative to on silicon integration for some applications