RWTH AACHEN UNIVERSITY

MPSoC'13

Two new Use Cases for Virtual Platforms

Rainer Leupers
Software for Systems on Silicon (SSS)
RWTH Aachen University

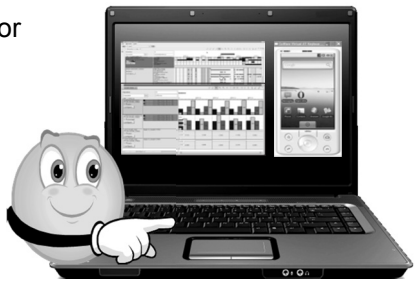
ICE

Institute for Communication Technologies and Embedded Systems

Why Virtual Platforms?

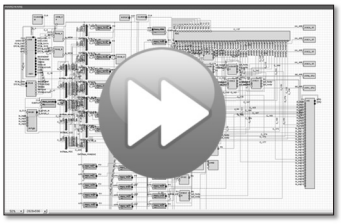
- **Benefits compared to HW:**
  - Earlier available than silicon prototypes
  - Easier to deploy than FPGA prototypes/lab equipment
  - Full control and visibility

- **Major use cases today:**
  - Platform HW/SW co-optimization for cost/performance
  - Pre-silicon SW development and integration
  - Platform-specific SW optimization and timing verification

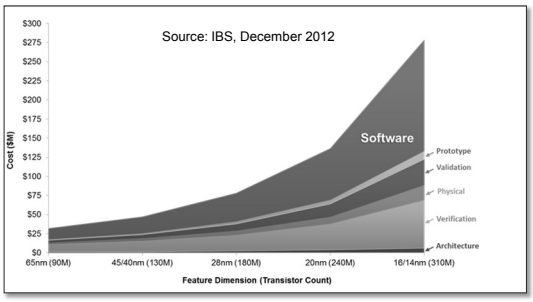


Forthcoming challenges in Virtual Platforms

- **Simulation speed**
  - *Transistor counts are increasing faster than simulation tool speed.* [Lisa Su, Freescale, DAC 2011]
  - Solutions: (careful) abstraction, maximum parallization, HW support, …



- **Improve VP ROI via more use cases**
  - Rising SW complexity → advanced MPSoC debug technology
  - „Dark silicon“ issues → early power estimation
  - VP based HW synthesis
  - „Google Earth“ like VP´s

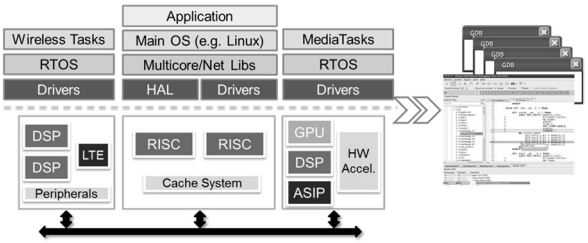



Use case 1: Embedded SW debugging for MPSoC´s

Institute for Communication Technologies and Embedded Systems

Challenge 1: scalability

- **How to design a SW debugger for SoC´s with 100s of heterogeneous cores and complex SW stacks?**
- **Classical single-processor oriented debug approach does not scale**
- **→ Higher debug abstraction levels needed**

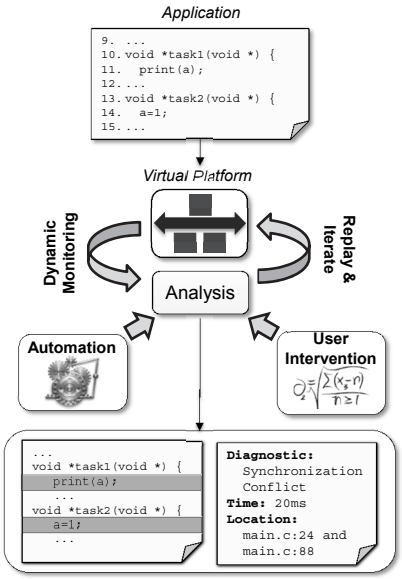


Debugging is underrepresented in MPSoC tools research:

Google search hits (May 2013):
- „multicore programming“: ~116,000
- „multicore DSE“: ~ 51,000
- „multicore debugging“: ~ 6,500

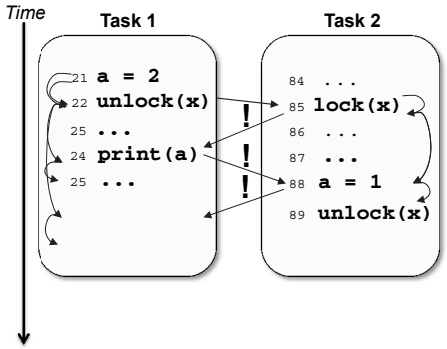
Scalability approach: high-level event monitoring

- **Debug engineer is interested in high-level communication and synchronization events**
- **Abstract from individual code lines**
- **Concept: Event monitor observes low-level events/state changes within VP and assembles (user specified) high-level events of interest**
- **→ Input for manual or automatic bug detection**



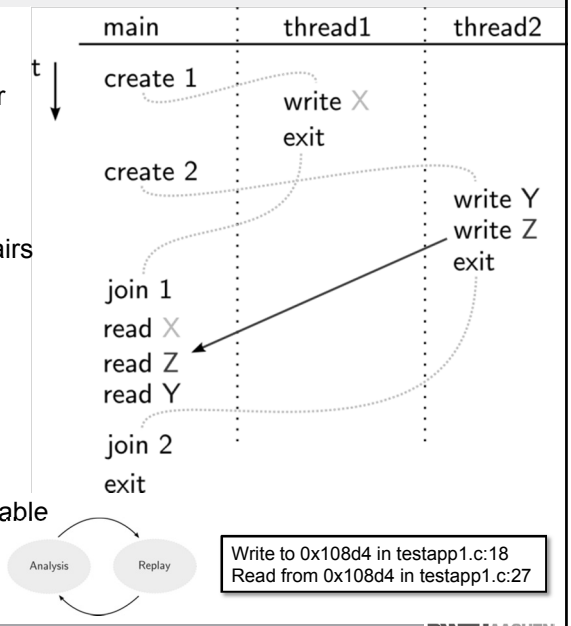
Challenge 2: concurrent SW bugs

- **Multicore SW shows: races, deadlocks, nondeterminism, …**
  - All in addition to „usual“ sequential SW bugs
  - Particularly hard to debug and reproduce (e.g. due to scheduling variances)



Concurrency bug approach: controlled event replay

- **Free replay**
  - Don‘t enforce event order
- **Strict replay**
  - Enforce total event order
- **Constrained replay**
  - Enforce order of event pairs
  - Concurrent replay
- **Iteration**
  - Replay using various constraints
  - Test effect on program
- **Output**
  - Nondeterminism with notable effect
  - Resolve to code lines

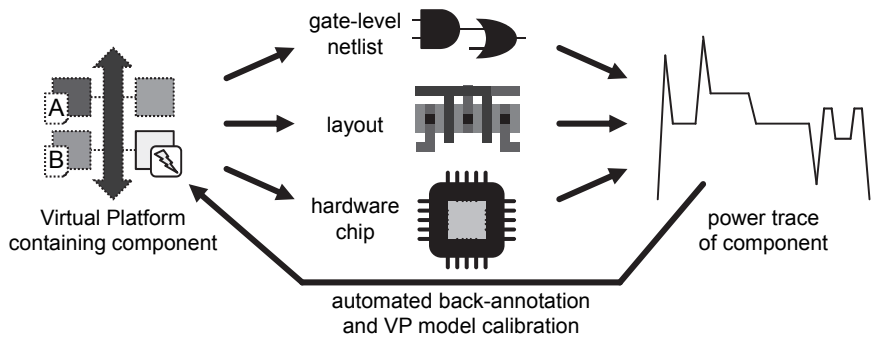


Use case 2: ESL power estimation

Institute for Communication Technologies and Embedded Systems

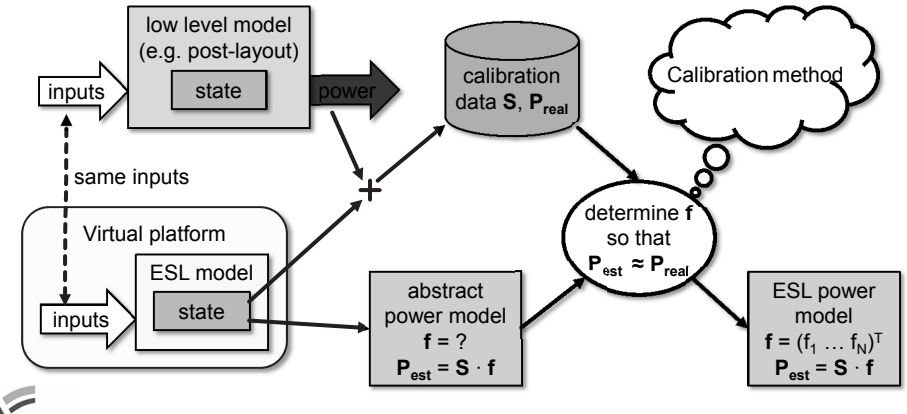
VP based power estimation approach

- **Enhance Virtual Platforms with power estimation features**
- **Fast and accurate power estimation provides added value to VP**



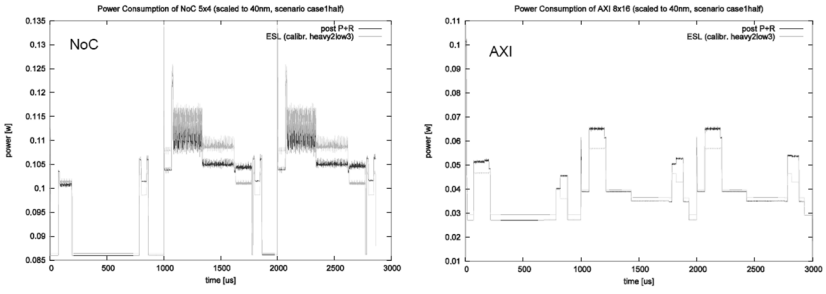
Power model calibration approach

- **Run low level model and VP model with same inputs**
- **Record VP component state and low-level power as calibration data**
- **Assume linear power model**
  - Determine power state factors **f** with best fit



Case study: AMBA AXI and custom NoC power analysis

- **VP based power estimation methodology verified for AMBA AXI and complex custom NoC at VLSI layout level (post P&R)**
- **Average error 5% - 21%**
- **600x - 1400x faster than low-level power simulation**
- **Can predict different „power phases“ correctly**
- **See [Schürmans@DAC2013] for details**



RWTH AACHEN UNIVERSITY

Thank you!