
Simulation of Many-core NoCs with QEMU and SystemC

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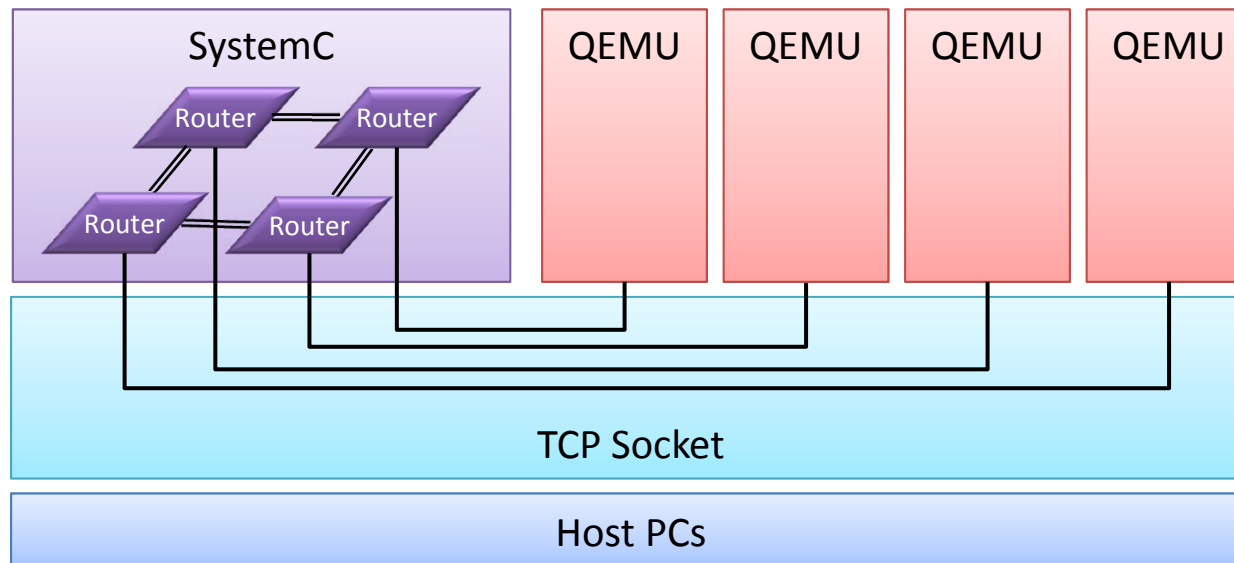
MPSoC 2013

Naxim

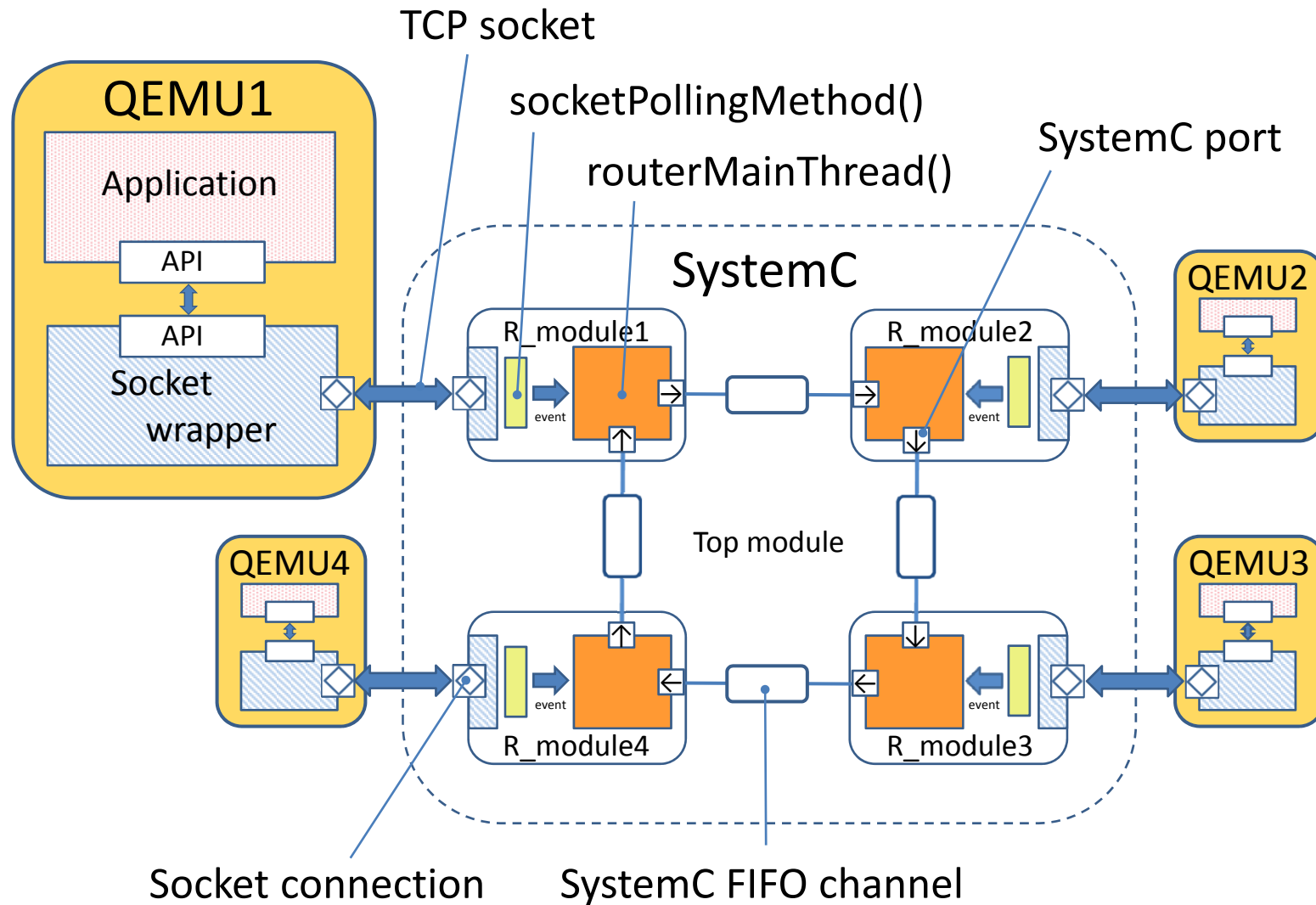
- ◆ Fast and retargetable NoC simulator
 - ◆ Software development
 - ◆ NoC architectural design space exploration
- ◆ Based on QEMU and SystemC
 - ◆ QEMU
 - ◆ Very popular open-source processor simulator
 - ◆ Very fast thanks to dynamic binary translation
 - ◆ Variety of processor cores supported
 - ◆ SystemC
 - ◆ Standard language for hardware design and simulation
- ◆ Key features
 - ◆ High retargetability
 - ◆ High simulation speed

Naxim Overview

- ◆ QEMU simulates software on a core
- ◆ Routers modeled in SystemC
- ◆ QEMU and SystemC simulator connected by TCP sockets
- ◆ QEMUs and SystemC simulator run in parallel as different processes on a multicore host or multiple hosts
- ◆ Message-passing communication (No shared memory)



Naxim Organization



Timing Issues

◆ QEMU part

- ◆ Use QEMU as is
 - ◆ Fast and retargetable, but inaccurate
- ◆ Use modified QEMU
 - ◆ Cache simulation implemented in ARM model

◆ Network part

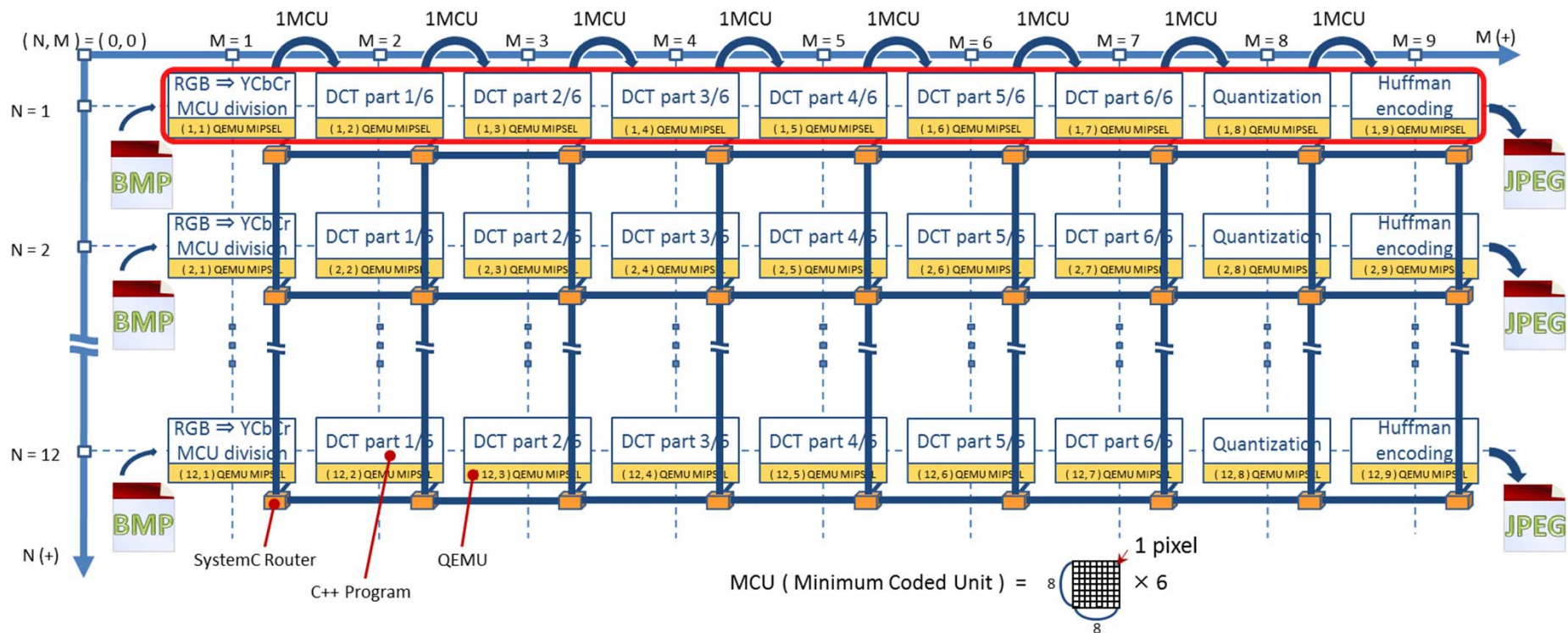
- ◆ Functional simulation
 - ◆ Transfer a whole packet from router to router in a *delta* cycle
- ◆ Cycle-accurate simulation

◆ Synchronization between QEMUs and SystemC

- ◆ SystemC has a master timer
- ◆ QEMU and SystemC synchronize when the QEMU sends/receives packets

Preliminary Experiments

- ◆ 2D-mesh NoCs (9 to 108 cores)
- ◆ Multiple JPEG encoders
 - ◆ 9-stage pipeline

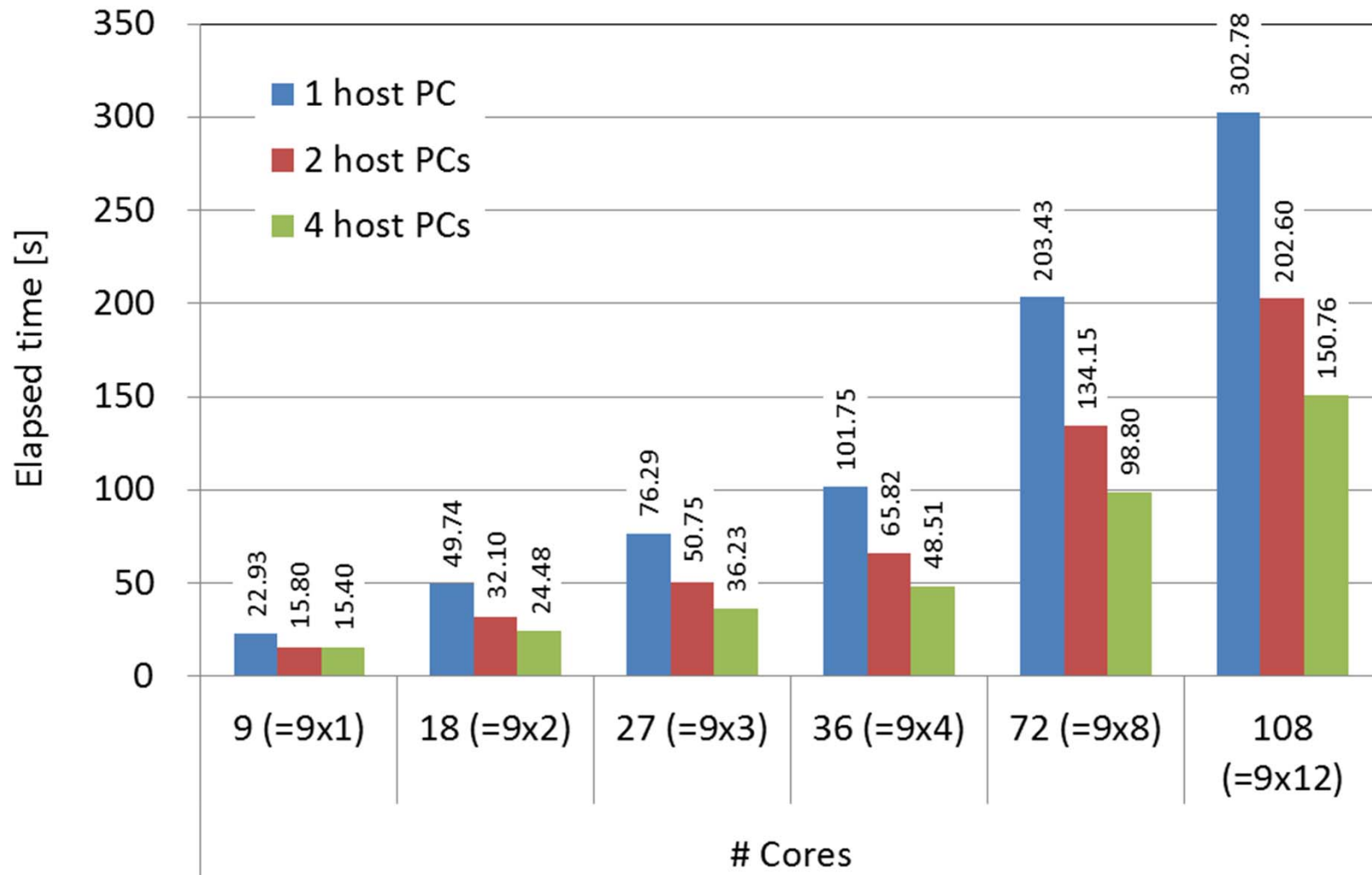


Scalability

Host: Intel Core2 Duo (2.53GHz)

Target: i386

Application: 1 to 12 JPEG encoders (1024x768 pix.)



Comparison with TLMu

◆ TLMu

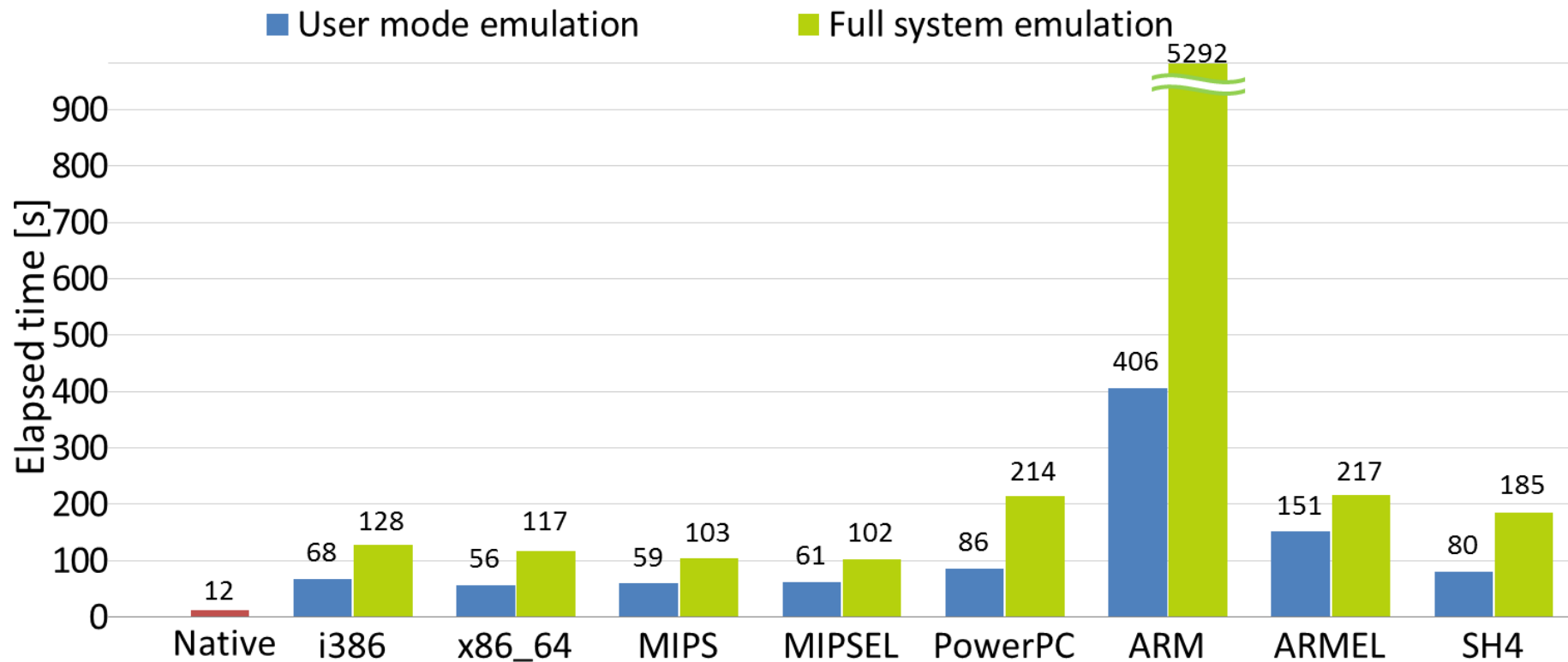
- ◆ Open-source SystemC wrapper for QEMU
- ◆ Single process execution

Elapsed simulation time	
Naxim	24 sec
TLMu	23,466 sec

Host: Intel Core i7 (3.46GHz, 6 cores, 12 threads)
Target: 9 ARM cores
Application: JPEG encoder (1024x768 pix.)

Retargetability

Host: Intel Core i7 (3.46GHz, 6 cores, 12 threads)
Target: 9 cores
Application: Single JPEG encoder (3648x2736 pix.)



Concluding Remarks

◆ Naxim

- ◆ Fast, retargetable NoC simulator based on QEMU and SystemC
- ◆ Successfully simulates >1000 core NoC

◆ Ongoing work

- ◆ Improve timing accuracy
- ◆ Support shared memory
- ◆ Adaptive load balancing over multiple hosts

◆ Contributors

- ◆ Keita Nakajima, Yusuke Fukutsuka, Yosuke Kurimoto, Shuto Kurebayashi, Takuji Hieda, Ittetsu Taniguchi