FINAL PROGRAM

SUNDAY JULY 6: WELCOME

18:00 Registration

19:00 Welcome reception

MONDAY JULY 7

8:00 Registration continued

KEYNOTE

8:30 Alexis Mather, ARM, UK, *"The secrets to tomorrow's high performance, low power media subsystems"*

9:30 Break

SESSION 1: MINI-KEYNOTES
"Communication & Energy Efficient MPSoC"

10:00 Keiji Kimura, Waseda University, Japan, *"A Latency Reduction Technique for Network Intrusion Detection System on Multicores"*

10:12 Kees Goossens, Eindhoven University of Technology, Netherlands, *"Better than worst-case design for real-time streaming applications"*

10:24 Marcello Coppola, STMicroelectronics, France, *"Low power multicore architecture using FDSOI technology"*

10:36 Shinobu Fujita, Toshiba, Japan, *"Advancement of Normally-off Processors (Ultra-low-power Processors) based on ultra-high-speed STT-MRAM"*

10:48 Ran Ginosar, Technion Institute of Technology, Israel, *"Plural: Shared Memory Many Core with Hardware Scheduling"*

11:00 Hiroshi Nakamura, The University of Tokyo, Japan, *"Normally-Off Computing for Smart City Applications"*

11:12 Marc Pollina, M3S, France, *"MIMOSA : Multi-sensor navigation platform"*

11:24 Panel discussions with the lecturers

12:00 Lunch

SESSION 2: IN-DEPTH TECHNICAL PRESENTATIONS
"Large scale computing & parallelism"

13:30 K. Charles Janac, Arteris Inc., USA, *"Advances in Safety and Resilience in SoC Interconnect"*

14:00 John Goodacre, ARM, UK, *"EUROSERVER: Riding the perfect storm"*

14:30 Jim Tung, MathWorks, USA, *" Extending Model-Based Design for HW/SW Design and Verification in MPSoCs"*

15:00 Break

15:30 Jason Cong, UCLA, USA, *"Automating Beyond High-Level Synthesis"*

16:00 Jochen Haerdtlein, Bosch, Germany, *"The Challenge of Mastering Parallelism in Real-time Systems"*

16:30 Hironori Kasahara, Waseda University, Japan, *"Multi-platform Automatic Parallelization and Power Reduction by OSCAR Compiler"*

17:00 Panel discussions with the lecturers

TUESDAY JULY 8

KEYNOTE

8:30 Akihiko Shinya, NTT Nanophotonics Center, Japan, *"Integrated Nanophotonics Technology Toward fJ/bit Optical Communication in a Chip"*

9:30 Break

SESSION 3: MINI-KEYNOTES
"Runtime Management in MPSoC"

10:00 Koichiro Yamashita, Fujitsu Laboratories LTD, Japan, *"Evaluation of Architecture Search Simulator for Wide-range Grid Wireless Sensor Network"*

10:12 Pierre G. Paulin, Synopsys, Canada, *"Parallel Processing Challenges in Embedded Vision Subsystems"*

10:24 Frederic Rousseau, TIMA, France, *"Lightweight task migration in multi-tiled architecture - Communication consistency"*

10:36 Nakajima Masaitsu, Panasonic, Japan, *"A Multithreaded Multi-core SoC for 4K2K Smart Screen Applications"*

10:48 Emil Matus, Technical University Dresden, Germany, *"Tomahawk-2 MPSoC and Model-Driven Software Development"*

11:00 Yoshinori Takeuchi, Osaka University, Japan, *"A Hierarchical Shared Bus Architecture Design Space Exploration Method"*

11:12 Gerhard P. Fettweis, TU Dresden, Germany, *"The TOMAHAWK-2: A Runtime Adaptive MPSoC"*

11:24 Panel discussions with the lecturers

12:00 Lunch

SESSION 4: IN-DEPTH TECHNICAL PRESENTATIONS
"Reconfigurable Computing"

13:30 James C. Hoe, Carnegie Mellon University, USA, *"Making Reusable Hardware Design IPs Usable: a NoC perspective"*

14:00 Iakovos Mavroidis, Forth, Greece, *"NUMA-like architecture for Microservers"*

14:30 Marilyn Wolf, Georgia Tech., USA, *"Accuracy-Aware Computing: Opportunities and Pitfalls"*

15:00 Break

15:30 Kees Vissers, Xilinx, USA, *"Novel 10Gbps memcached implementations designed with High Level Synthesis in FPGAs"*

16:00 Arnaud Grasset, Thales Research & Tech., France, *"Reliable and Predictable MPSoCs for Critical Embedded Systems"*

16:30 Sorin Cotofana, Delft University of Technology, Netherlands, *"Ageing Assessment, Prediction, and Lifetime Reliability Aware Resource Management"*

17:00 Panel discussions with the lecturers

WEDNESDAY JULY 9

KEYNOTE

8:30 Giorgio Cesana, ST, France, *"The FD-SOI Technology for Very High-speed and Energy Efficient SoCs"*

9:30 Break

SESSION 5: MINI-KEYNOTES
"MPSoC HW and SW Architectures"

10:00 Koji Inoue, Kyushu University, Japan, *"CPU-Memory Power Shifting on High Performance Computing"*

10:12 Gabriela Nicolescu, Ecole Polytechnique de Montréal, Canada, *"KyberSecurity, a platform for endpoints protection in cloud"*

10:24 Kees van Berkel, Ericsson, Eindhoven University of Technology, Netherlands, *"Multi-core for 4G cellular modems"*

10:36 Akira Asato, Fujitsu, Japan, *"Design methodology for SoCs in large supercomputer systems"*

10:48 Jos van Eijndhoven, Vector Fabrics, Netherlands, *"Programmability of shared-memory multi-core architectures"*

11:00 Jiang Xu, Hong Kong University of Science and Technology, Hong Kong, *"Sensor Network on Chip: A HW-SW Collaborated Method for Resilient MPSoC"*

11:12 Masaki Gondo, eSOL, Japan, *"A new way to describe hardware for software tools – SHIM"*

11:24 Panel discussions with the lecturers

12:00 Lunch

SESSION 6: IN-DEPTH TECHNICAL PRESENTATIONS
"Application Specific MPSoC Architectures"

13:30 Rishiyur Nikhil, BlueSpec, USA, *"Bluespec BSV, the choice for CPU and SoC designers"*

14:00 Chris Rowen, Cadence, USA, *"Making High Performance Vision Processing Real"*

14:30 Tsuneo Nakata, Fujitsu Laboratories of Europe, UK

15:00 Panel discussions with the lecturers

15:30 Speakers' Meeting

19:30 Social event

THURSDAY JULY 10

KEYNOTE

8:30 Jean Pierre Tual, Gemalto, France, *"An overview of some security and privacy design challenges in M2M, Internet of Things or Wearable computing applications"*

9:30 Break

SESSION 7: MINI-KEYNOTES
"Design Methodologies"

10:00 Yuichi Nakamura, NEC Corp., Japan, *"A scalable connection method beyond processor cores"*

10:12 Giovanni Beltrame, École Polytechnique de Montréal, Canada, *"Efficient Device Lifetime Estimation via Design Space Pruning"*

10:24 Edith Beigne, CEA-Leti, France, *"Wide Voltage Range Operation Using FDSOI Technology and Maximum Frequency Tracking Techniques"*

10:36 Takashi Miyamori, Toshiba, Japan, *"Novel Video and Image Processing beyond Commoditization"*

10:48 Gerd Ascheid, RWTH Aachen University, Germany, *"Efficiency, Flexibility and Ease of Programming - A comparison of two opposite architectural approaches"*

11:00 Sungjoo Yoo, POSTECH, Korea, *"Low Power Hybrid Memory Cube with Link On/Off Management"*

11:12 Rui Hou, Chinese Academy of Sciences, China, *"Understanding the Behavior of In-Memory Computing Workloads"*

11:24 Panel discussions with the lecturers

12:00 Lunch

SESSION 8: IN-DEPTH TECHNICAL PRESENTATIONS
"Secured MPSoC"

13:30 Yankin Tanurhan, Synopsys, USA, *"In the Days of IoT: Dealing with Software Parallelization for Heterogeneous Multicore Architectures"*

14:00 Babak Falsafi, EPFL, Switzerland, *"Meet the Walkers: Accelerating Index Traversals for In-Memory Databases"*

14:30 Yoshifumi Sakamoto, IBM Japan, Japan, *"Performance evaluation of a multi-core system using Systems development method utilizing Reverse modeling and Model-based Simulation"*

15:00 Break

SESSION 9: MINI-KEYNOTES
"Energy Efficient MPSoC Architectures"

15:30 Fumio Arakawa, Nagoya University, Japan, *"Nanoprocessor Cluster: Conversion from ILP to uTLP"*

15:42 Norbert Wehn, University of Kaiserslautern, Germany, *"A Runtime Reconfigurable Architecture for Monte Carlo Option Pricing in the Heston Model"*

15:54 Tsuyoshi Isshiki, Tokyo Institute of Technology, Japan, "*Low Power Multicore SoC Architecture for UWB MAC Processing*"

16:06 Kiyoung Choi, Seoul National University, Korea, *"Low Energy STT-RAM Cache with Dead Write Prediction"*

16:18 Tohru Ishihara, Kyoto University, Japan, *"Near-Threshold Computing on Heterogeneous Multicore Architectures"*

16:30 Andreas Herkersdorf , TU Munich, Germany, *"Conquering MPSoC Design and Architecture Complexity with Bio-Inspired Self-Organization"*

16:42 Youn-Long Lin, National Tsing Hua University, Taiwan, *"Distributed Flow-Table Cache for OpenFlow Switch"*

17:00 Panel discussions with the lecturers

FRIDAY JULY 11

KEYNOTE

8:30 Sylvain Martel, École Polytechnique de Montréal, Canada, *"Coordinating simultaneously tens of millions of intelligent autonomous robots, each being smaller than a red blood cell, for cancer therapy and beyond"*

9:30 Break

SESSION 10: MINI-KEYNOTES

10:00 Frédéric Pétrot, TIMA Lab, Grenoble University, France. *"Automatic Generation of Efficient Dynamic Binary Translators"*

10:12 Pieter van der Wolf, Synopsys, Netherlands

10:24 Masaaki Kondo, The University of Tokyo, Japan, *"Evaluating Power-Efficiency for an Embedded Microprocessor with Fine-Grained Power-Gating"*

10:36 Yuan Xie, Penn State/AMD Research, USA, *"Reliability-Aware Cross-Point Resistive Memory Design"*

10:48 Xiaoyao Liang, Shanghai Jiao Tong University, China, *"Compiler Assisted Dynamic Register File in GPGPU"*

11:00 Raphaël David, CEA LIST, France, *"In Sensor Processing: Opportunities for Massively Parallel Computing"*

11:12 Panel discussions with the lecturers

12:00 Lunch