The FD-SOI technology for very high-speed and energy efficient SoCs

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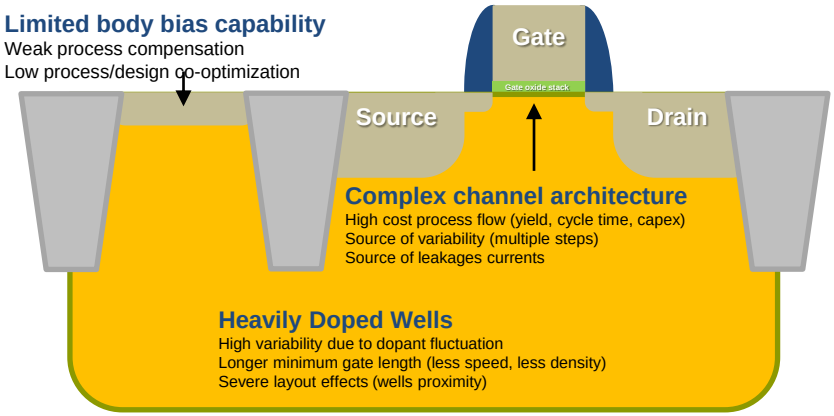
STMicroelectronics

FD-SOI

life.augmented

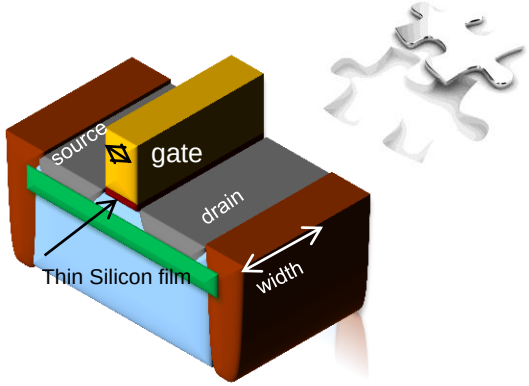
FD-SOI Technology

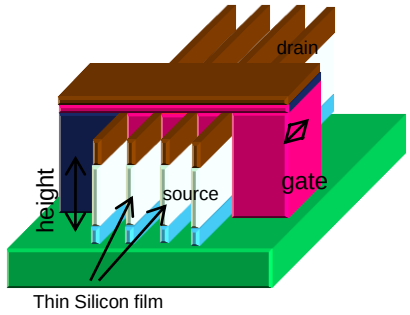
Bulk Transistor Reaching Limits at 20nm



Depleted devices deliver improved electrostatic control and device scalability

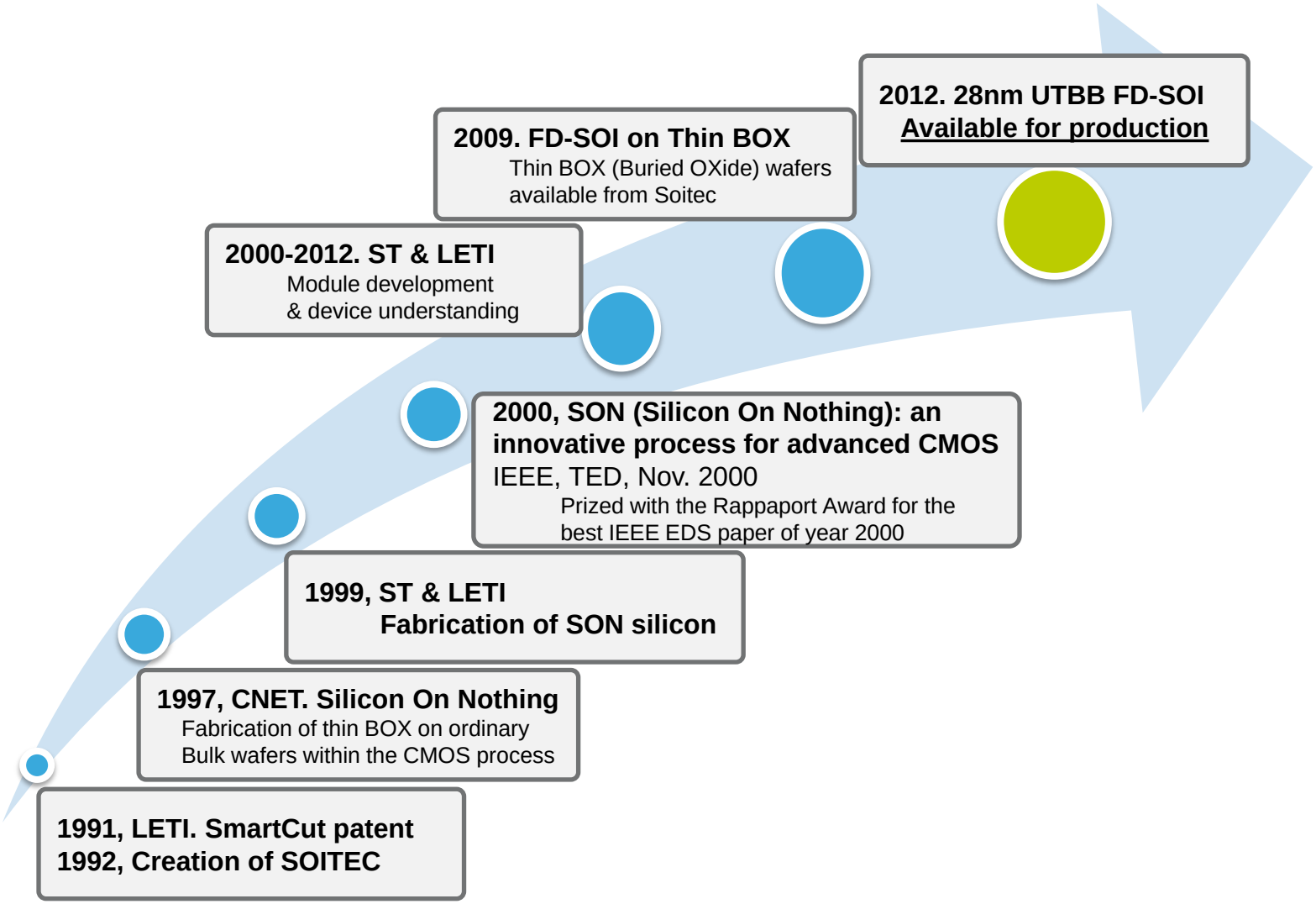
FD-SOI = 2D



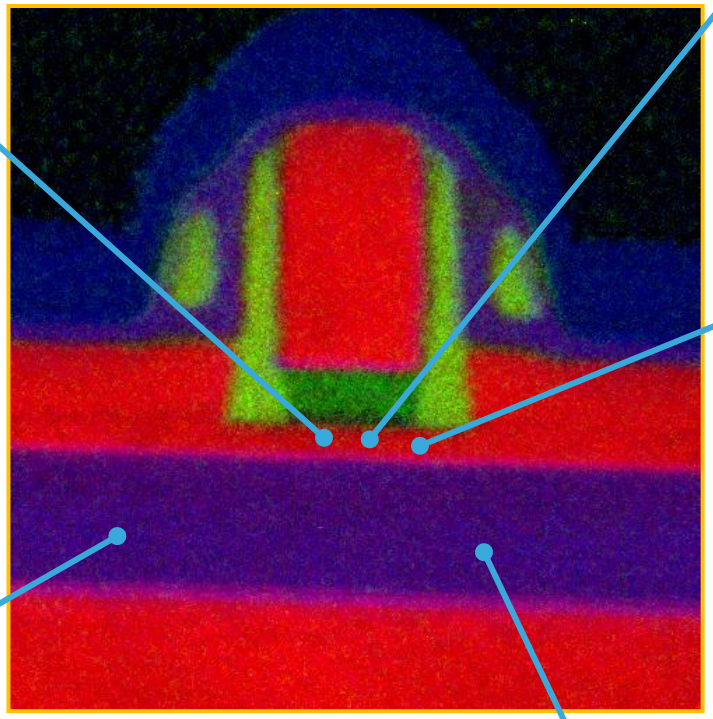


FinFET = 3D

UTBB FD-SOI, A Long R&D Success Story

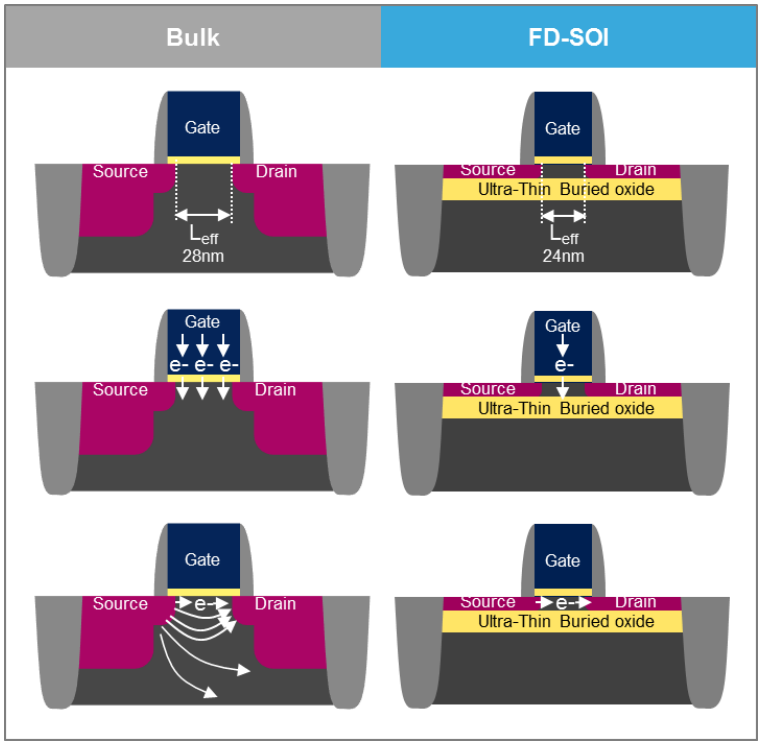


28FDSOI Transistor Summary



Efficient FD-SOI Transistors

- FD-SOI enables better transistor electrostatics
  - Enabling faster operation at low voltage, leading to better energy efficiency
  - Improving transistor behavior, especially at low supply, enabling ultra-low-voltage operation
  - Reducing transistor variability sources
- FD-SOI has a shorter channel length
  - 28nm FD-SOI is in reality a **24nm** technology!
- FD-SOI has lower leakage current
  - Lower channel leakage current
    - Carriers efficiently confined from source to drain
  - Thicker gate dielectrics, leading to lower gate leakage
  - Enabling ultra low power SRAM memories
  - Leakage current is less sensitive to temperature with FD-SOI



FD-SOI
The best technology choice

Superior and flexible technology

- FD-SOI transistors are faster, cooler, simpler
- Outstanding power efficiency across all use cases
- Efficiency at all levels: CPU, logic, Memories, Analog
- Manufacturing infrastructure and process reuse
- Improved reliability

Enhanced design options

- Very large operating range for the same design
- Back-biasing as a flexible and powerful optimization
- Ultra-wide range DVFS
- Enhanced efficiency of multi-core processing
- Easier design than FinFET

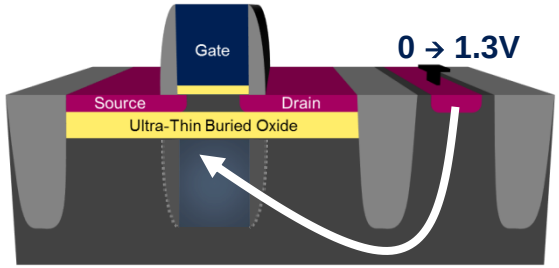
Gives your SOC competitive advantages

- Costs: chip-level and/or system-level (e.g. cost of cooling)
- Thermal power dissipation (TDP)
- Extended battery life
- Computing Power / Speed / Reactivity
- Reliability
- Time-to-Market

Forward Body Biasing (FBB)

A very reasonable effort for extremely worthwhile benefits

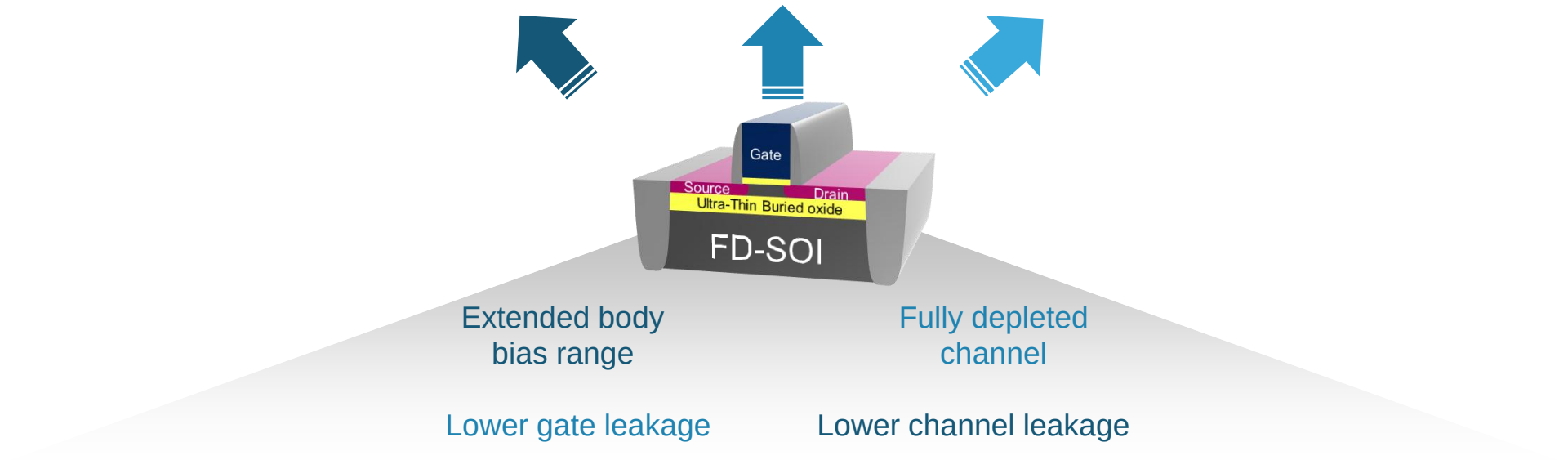
- An **extremely powerful** and flexible concept in FD-SOI to :
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts



- Comparatively **easy to implement** – if you've ever done DVFS you'll have no difficulty with Body Biasing

FD-SOI: Efficiency at all levels

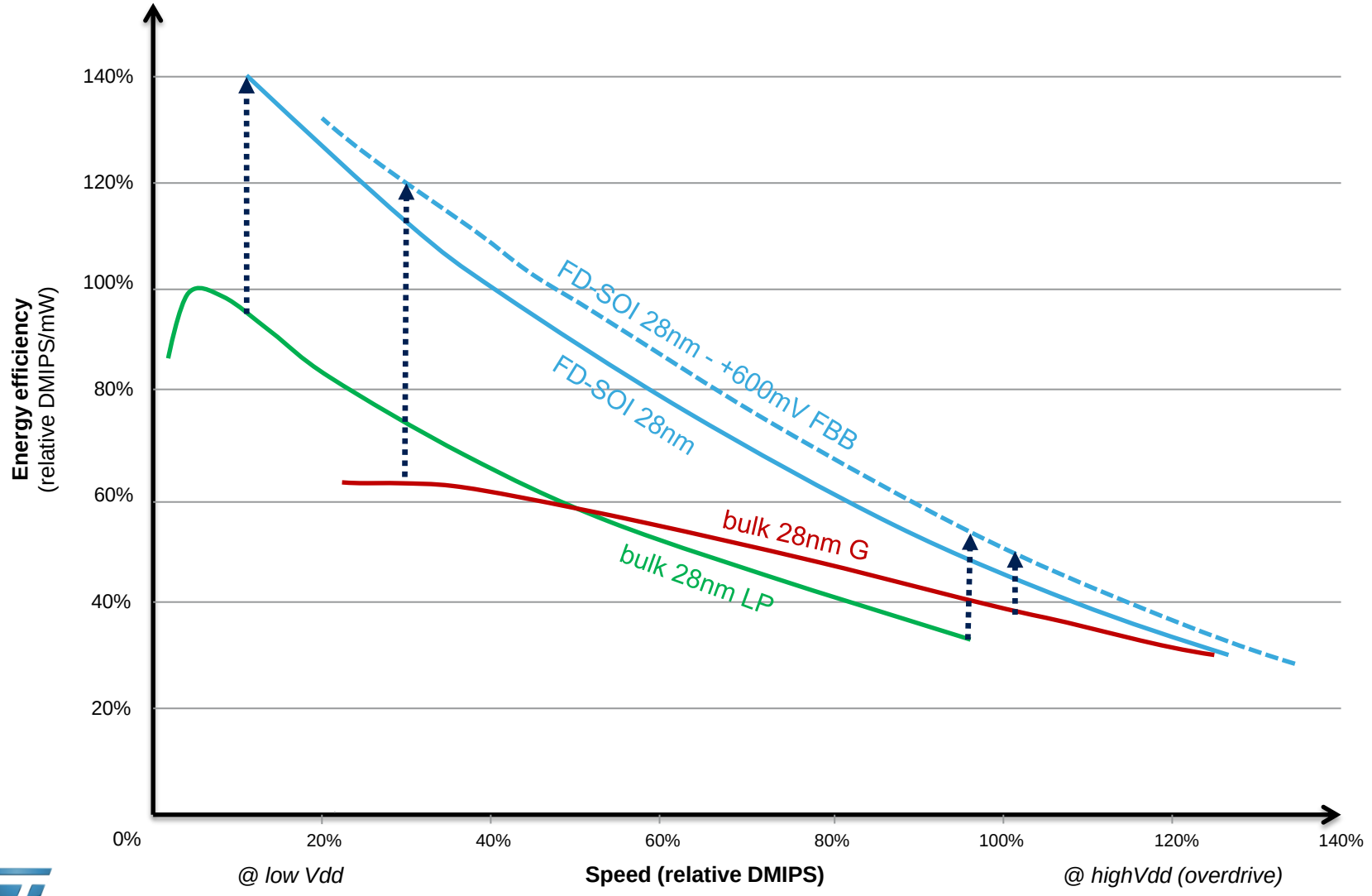
CPU, GPU and logic	Memories	Analog & High-speed
FBB dynamic modulation to get the best total power Best dynamic power /leakage tradeoff	Memory bit cells in FD-SOI have much less leakage compared to Bulk	FD-SOI analog performance far beyond Bulk one Better figure of merit than FinFET for high-speed IPs



Better transistor electrostatics

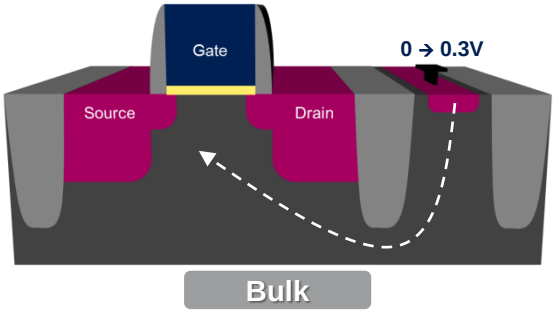
FD-SOI Energy Efficiency

28nm FD-SOI Best in class efficiency

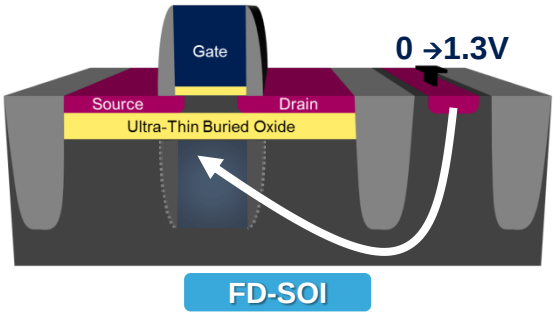


FD-SOI: The FBB advantage

- What is Body Biasing?
  - A voltage is applied to the substrate (or body).
  - When voltage is positive, it is called **Forward Body Biasing**, or **FBB**



- Why FBB is much more efficient in FD-SOI?
  - The Insulator layer (UTTB) prevents the parasitic effects that normally appear during the body biasing
  - This allows much wider range of biasing compared to Bulk
  - FBB can be modulated dynamically during the transistor operation and the transitions are transparent to the SW



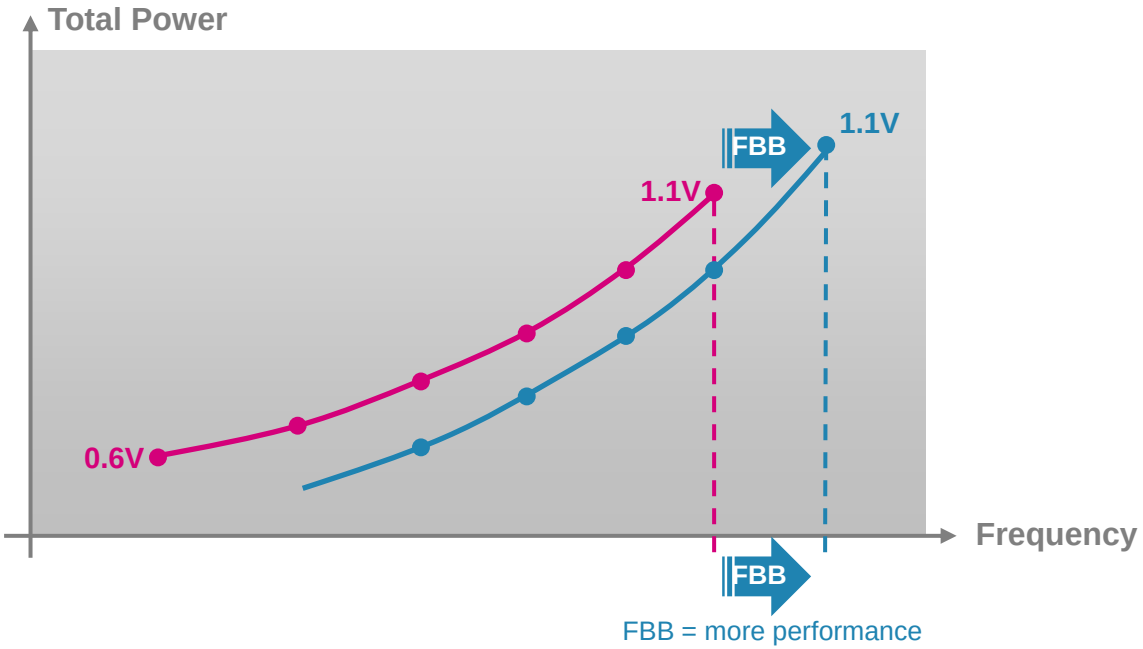
- FBB benefits
  - **Performance boost**
  - **Reduce power consumption** at a given performance requirement
  - **Process compensation** reducing the margins to be taken at design
  - **Easy to implement**: seamless inclusion in the EDA flow

FBB for performance boost

- FBB provides performance boost when voltage can’t be increased
  - Limited impact on dynamic power, no impact on voltage drops

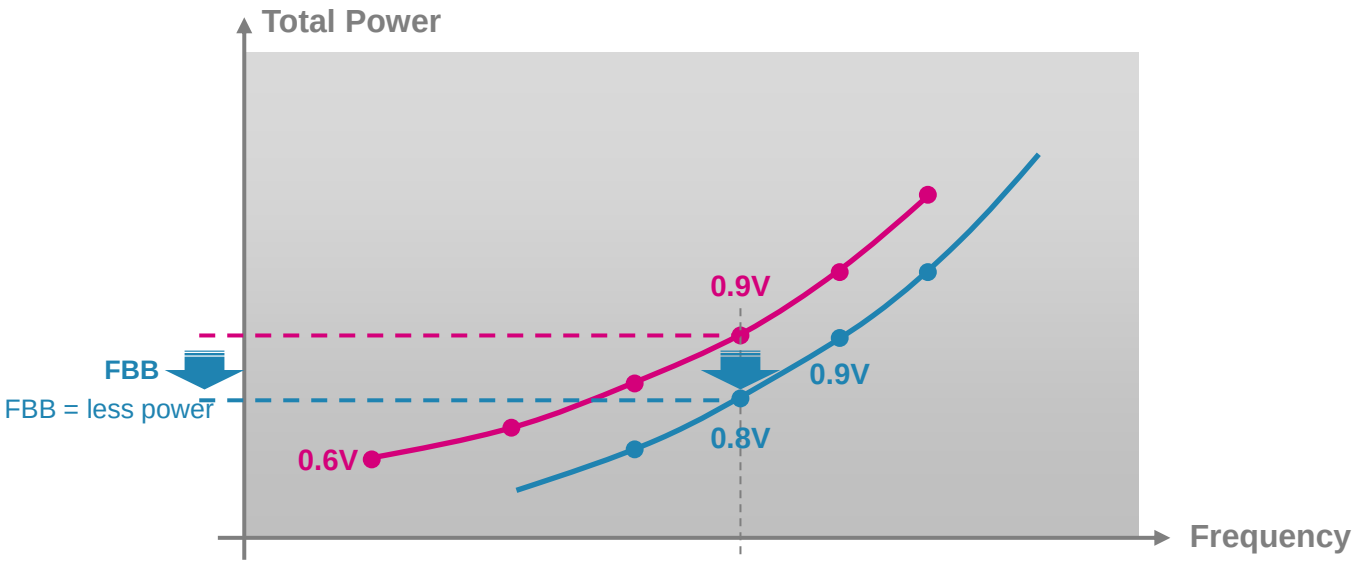
  → More efficient performance increase than turning the voltage
  - Impact on leakage at high temperature

  → Back into 28G range but leakage can be turned off anytime by removing FBB



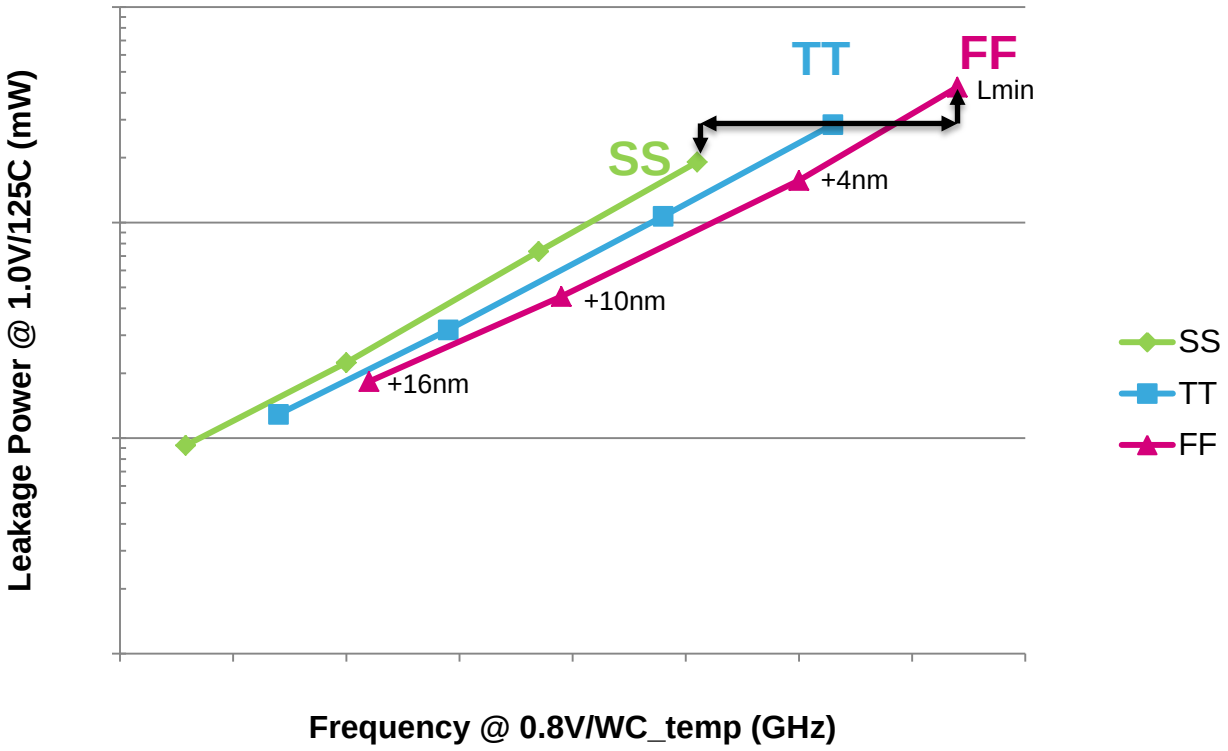
FBB improves power efficiency

- FBB improve the power efficiency at a given frequency
  - Limited impact on leakage, slightly higher than without FBB
  - Drastically decrease dynamic power



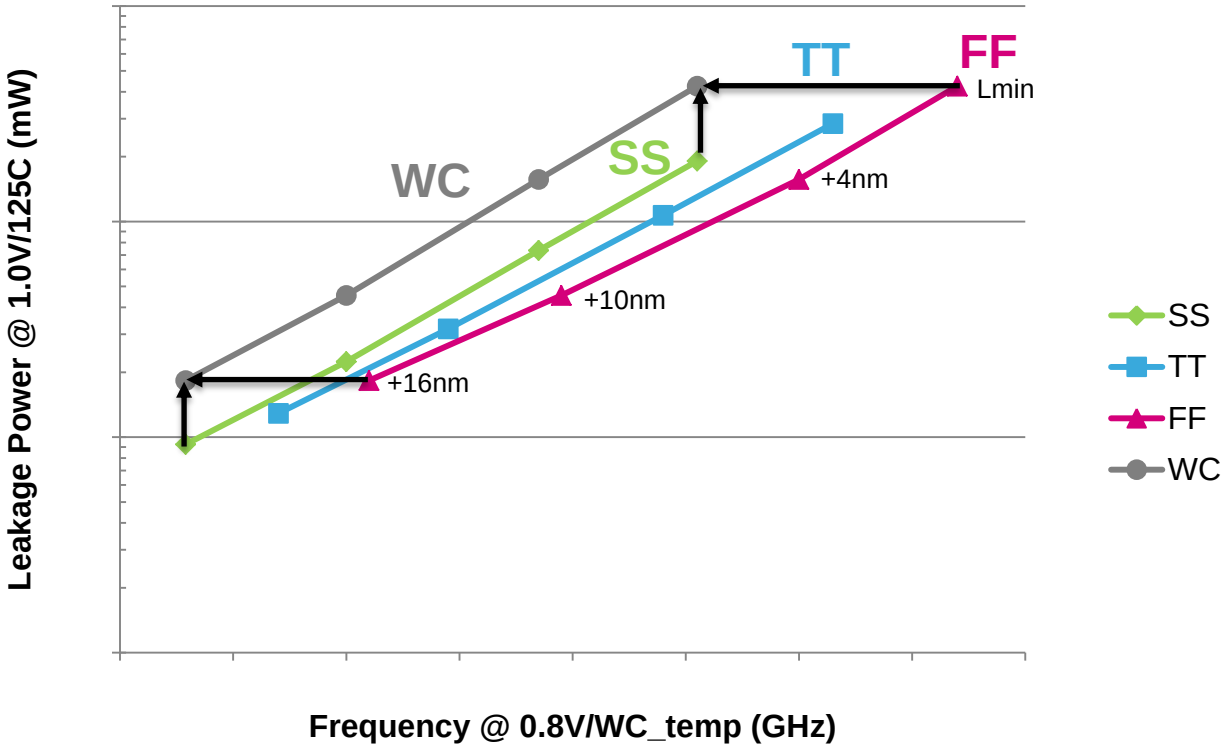
FD-SOI Process Compensation by Forward Body Bias

Performance Corner Spread w/o Body Bias



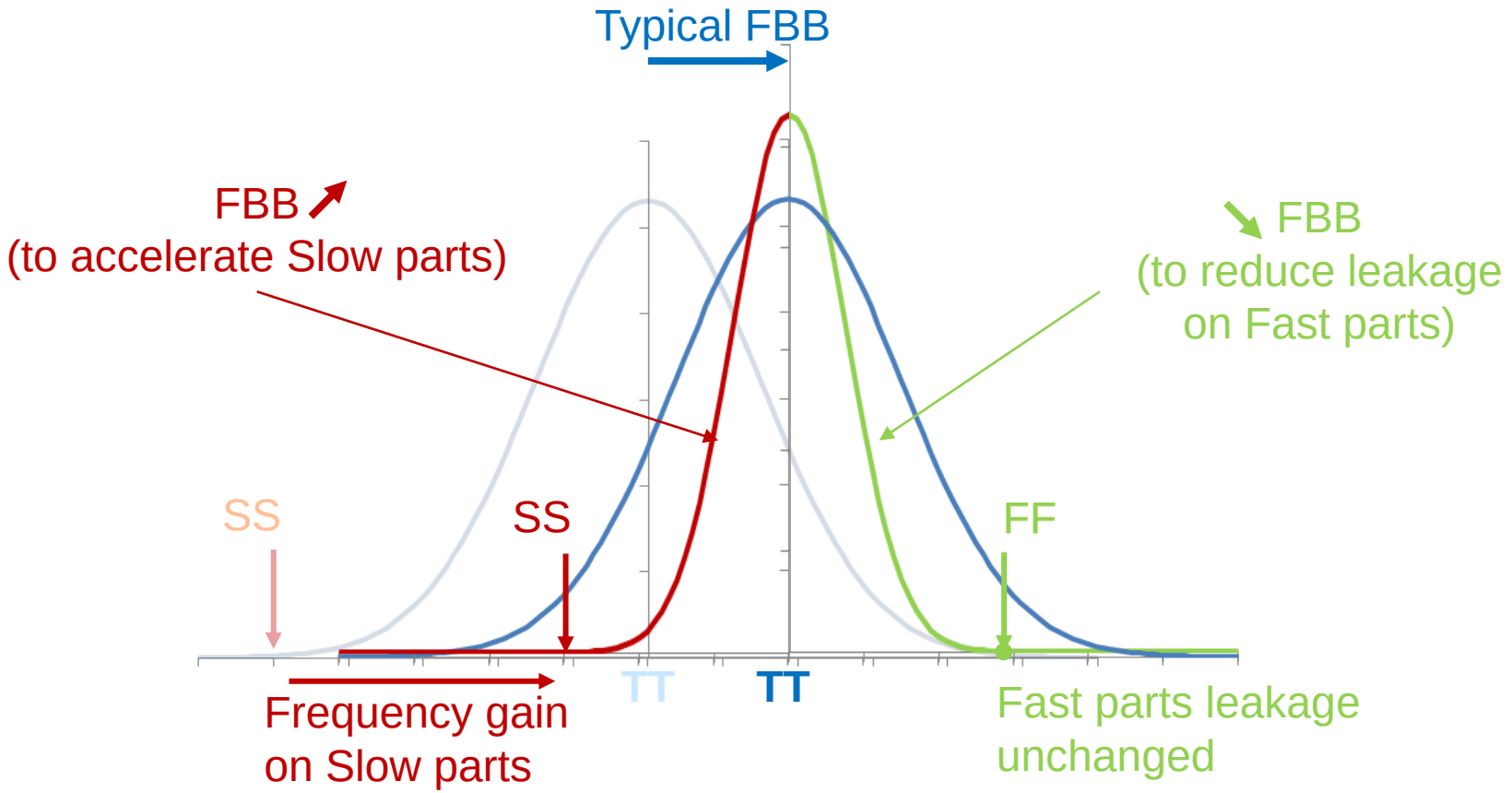
- Frequency and leakage corner spreads depend on PVT and channel length

Worst Case Performances w/o Body Bias



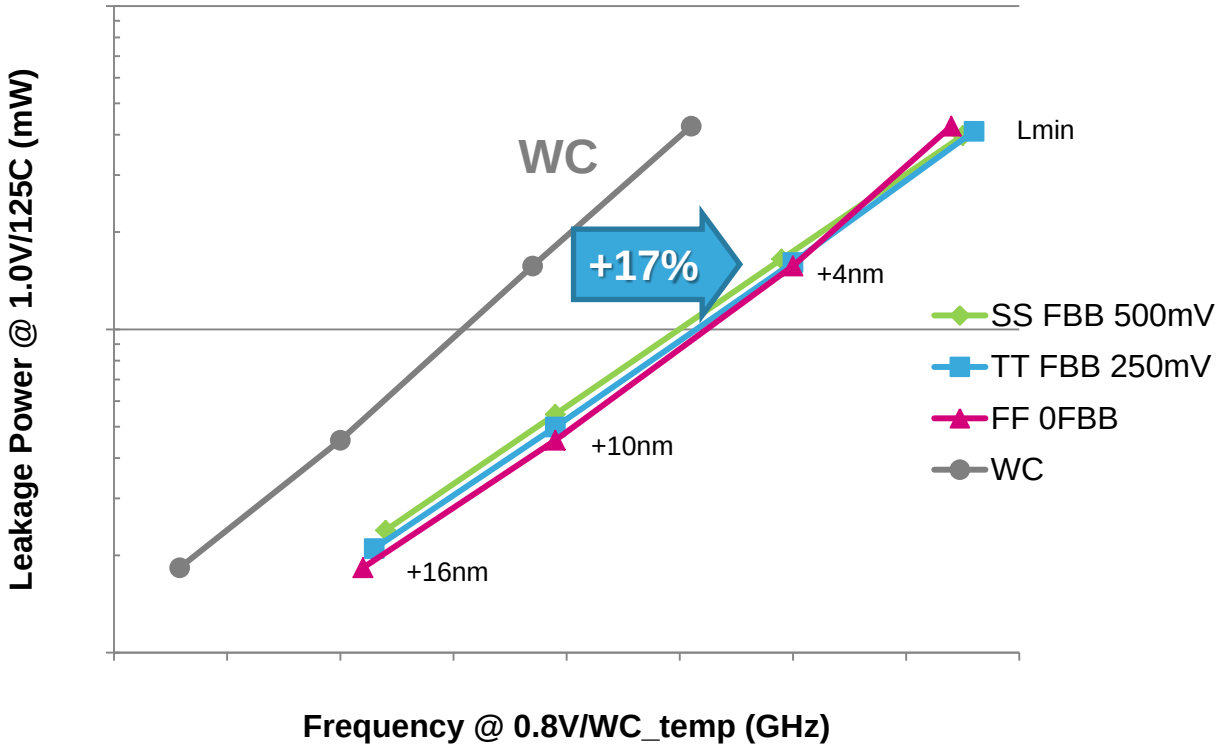
- For each gate length, the worst case performance trend (WC) is built using the slowest case (SS) and the leakiest case (FF)
- This is what used for ASIC sign-off

FBB-based Process Compensation: Principle



- SLVT doesn't allow RBB → FBB must be applied on typical to allow "pseudo-RBB" for Fast parts (leakage containment)
- Higher FBB is applied to accelerate Slow parts

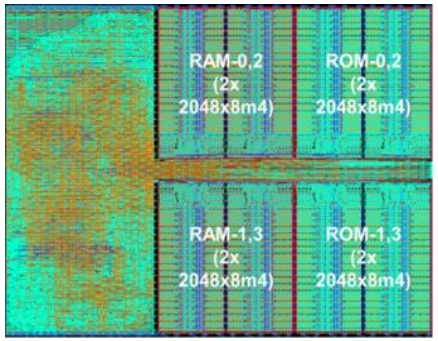
Process Compensation Through FBB



- Process Compensation through FBB allows
  - Masking SS-FF process spread
  - Recovering +17% speed in 28nm FD-SOI, at no dynamic power expense (as it would happen if using AVS)

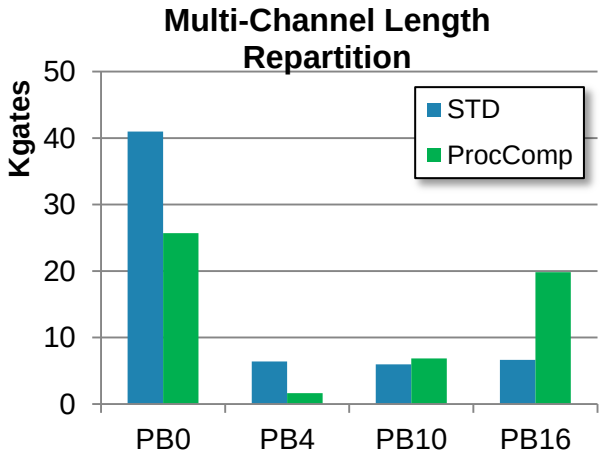
Process Compensation Benefits
The case of a Cortex M4

- ARM Cortex-M4
  - 50kgates, 5k FF
  - Target frequency: 700MHz @ WC/0.8V
- Two implementations comparison
  - Standard methodology, full process spread sign-off
  - Process compensation by FBB
    - SS corner is compensated by 600mV FBB



ARM Cortex-M4 FDSOI28

	Standard	Proc. Comp.	Diff/ %
Area (µm²)	81'407	61'035	-25%
Total Power @ Vmax, 125C, RCmax	REF	0.55x	-45%
Leakage (mA) @ Vmax, 125C	REF	0.49x	-51%



FD-SOI Technology for Fast CPU/GPU

Demonstrated Reduced Design Effort
for Full 28nm SoC Porting

- Same design flow as for 32/28nm LP
  - Same tools used
  - Same design cycle time
- True concurrent engineering
  - FDSOI product received before bulk version
- Direct mapping of IPs + ECO
  - Script based
  - Faster than rerunning synthesis
  - Floorplan reuse

CPU
Dual Cortex A9

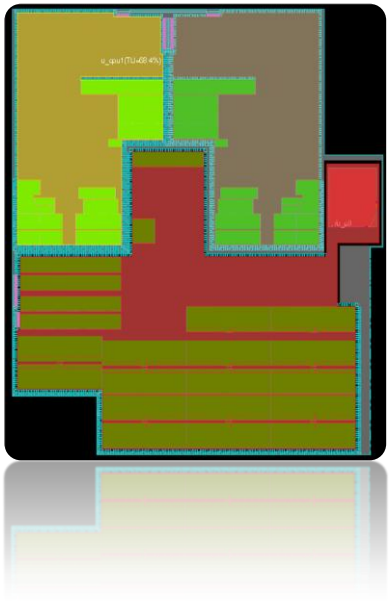
+40% in speed

> 3X at low V

GPU
SGX544 MP1

+20% at nom V

Power reduction



HD camera
IP

+30% in speed

LPDDR2
533Mhz

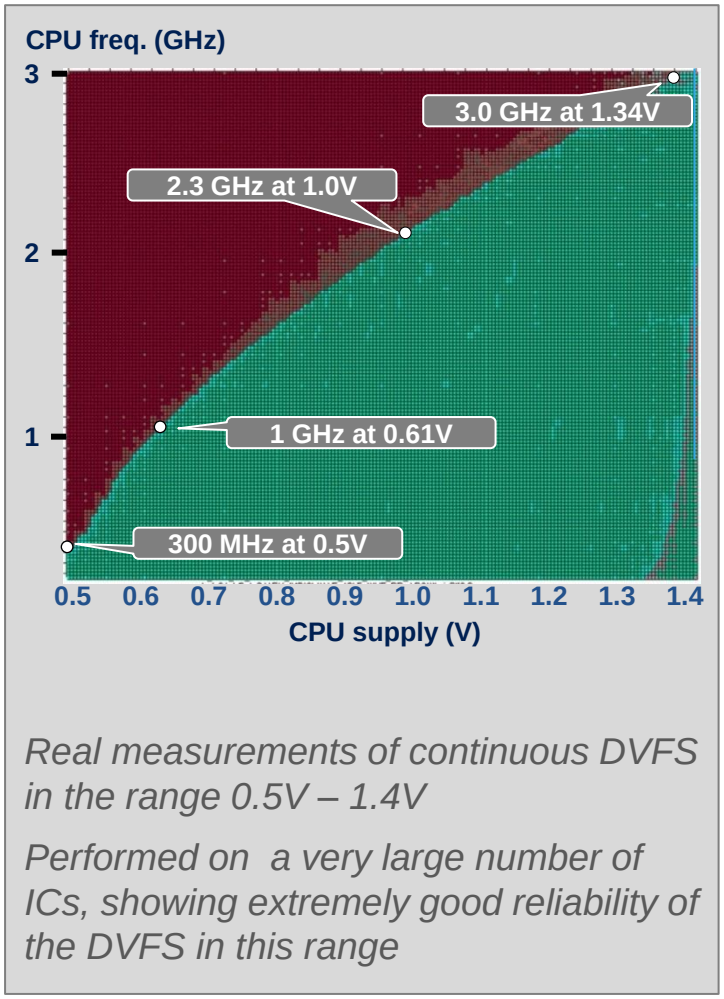
-15% in power

PLLs
Up to 4.6GHz

-15% in power

FD-SOI allowing Ultra-Wide DVFS

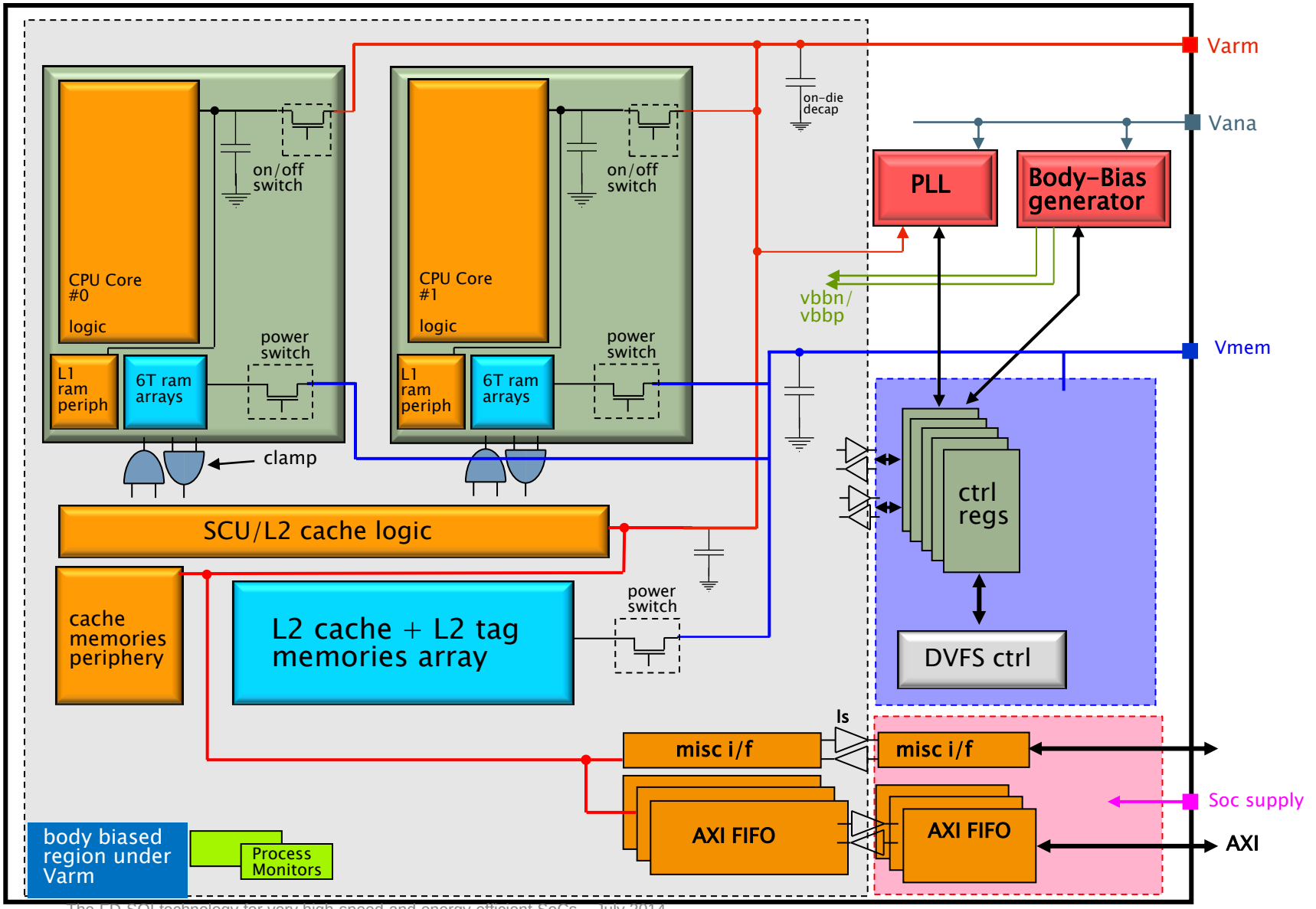
- FD-SOI allows the widest Vdd range for voltage scaling
- Still guaranteeing top notch speeds at very low operating voltage
  - >5x when compared to 28LP technology
  - >35% when compared to 28G technologies
- DVFS energy efficiency optimization is further extended thanks to body bias
  - Allowing to balance and optimize the static and dynamic power consumption components



Real measurements of continuous DVFS in the range 0.5V – 1.4V

Performed on a very large number of ICs, showing extremely good reliability of the DVFS in this range

Dual Cortex A9 subsystem architecture



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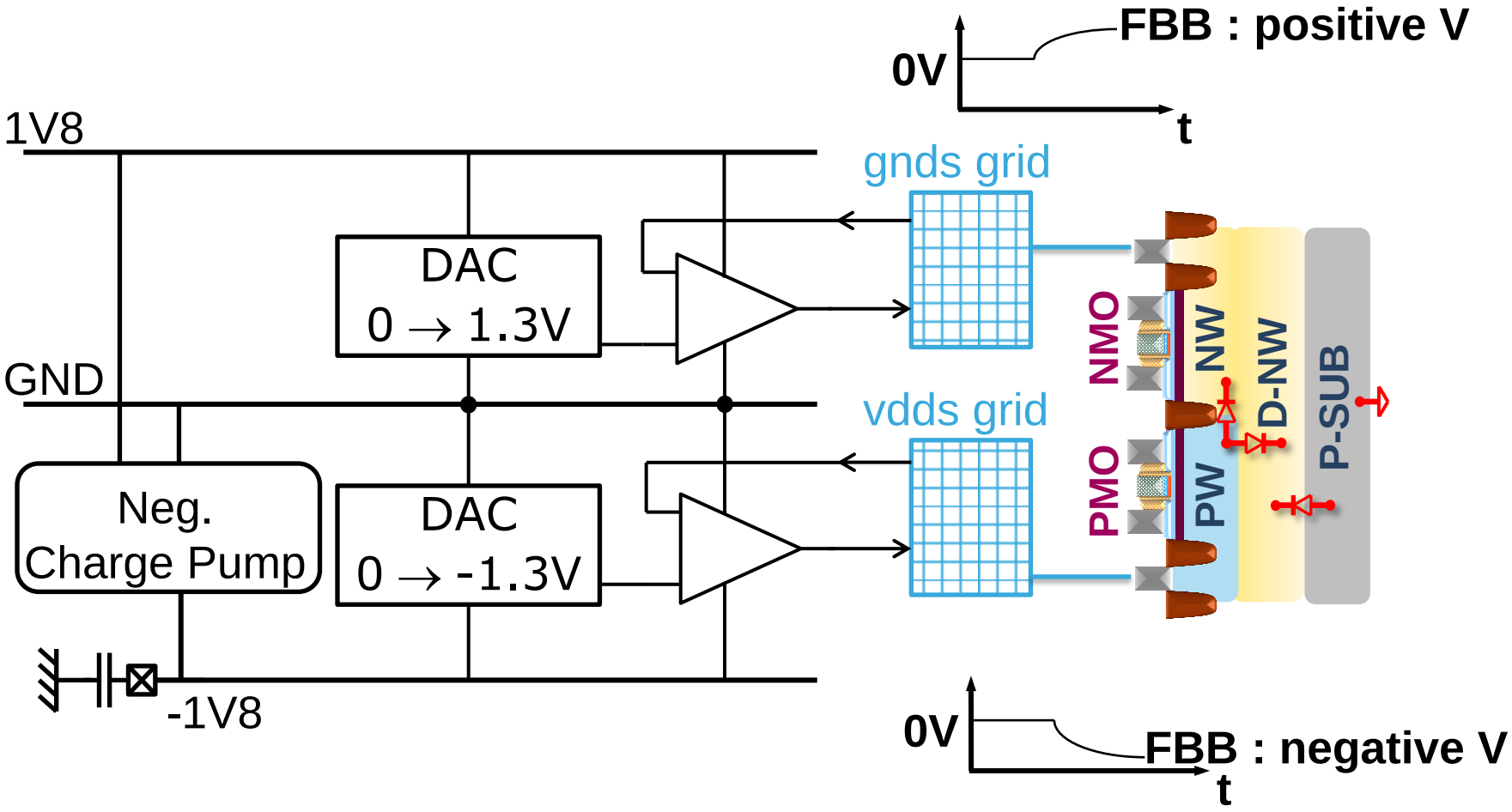
Body-Bias voltage generation

- How to generate programmable body voltages ?



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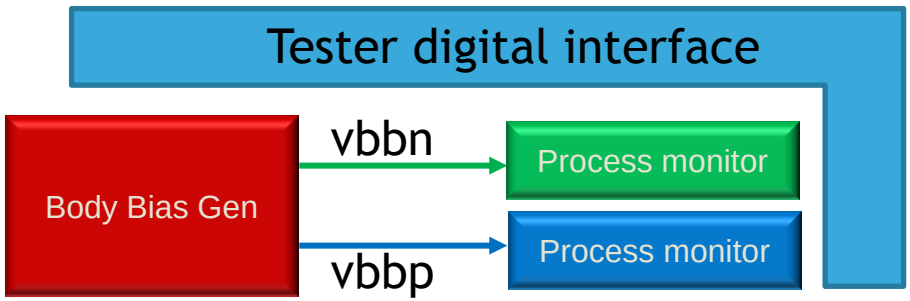
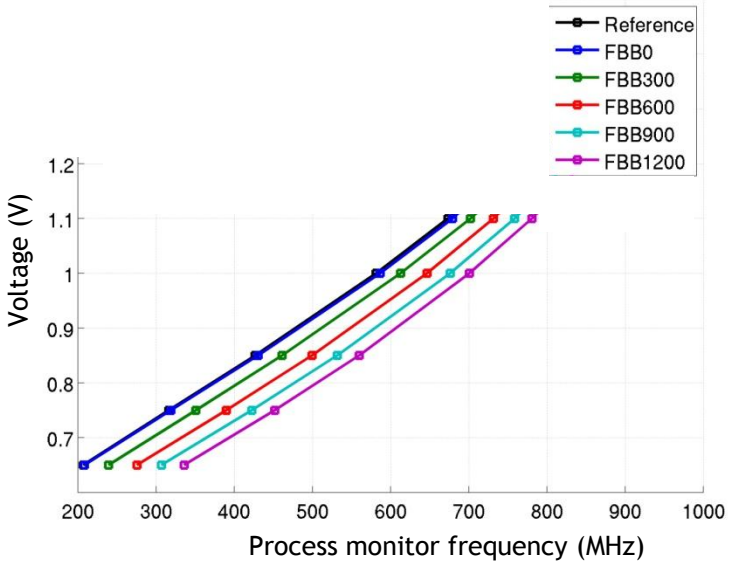
Fully digital testing of the BBgen

- The BBgen is generating 2 independent voltages
  - For the Nmos [0 to 1.3V] & Pmos [-1.3V to 0V] bodies
  - With a resolution of 100 mV
  - The embedded process monitors allow a full digital test of the BBGen in production test
    - No need for body nodes external access
    - Full access via a digital interface





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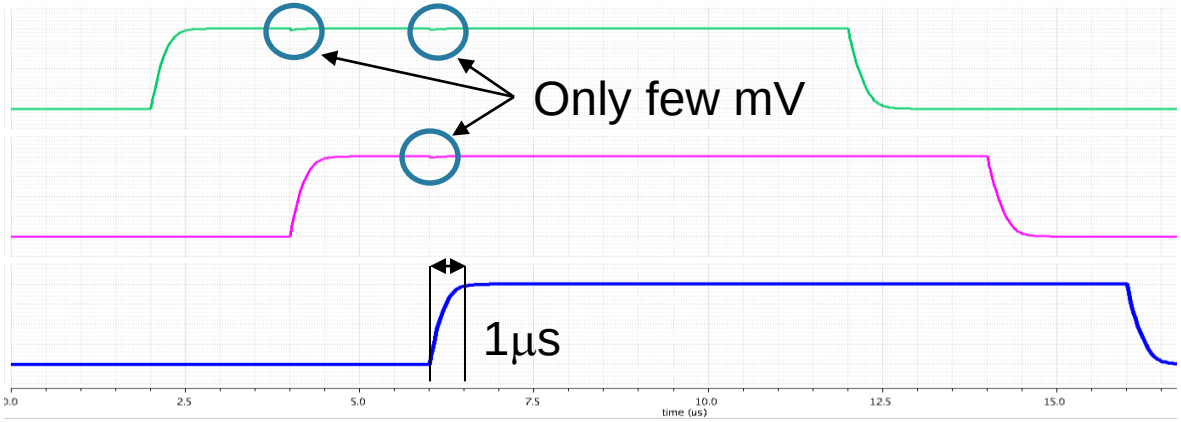
Fast dynamic body-bias management

- Low Zout amplifiers allow ms settling time of the body nodes
  - E.g. 3 body domains connected to the same generator
  - Each body domain can be activated
    - In less than 1ms
    - Activating any body domain does not disturb the voltage of the others

BB Domain#0 voltage

BB Domain#1 voltage

BB Domain#2 voltage



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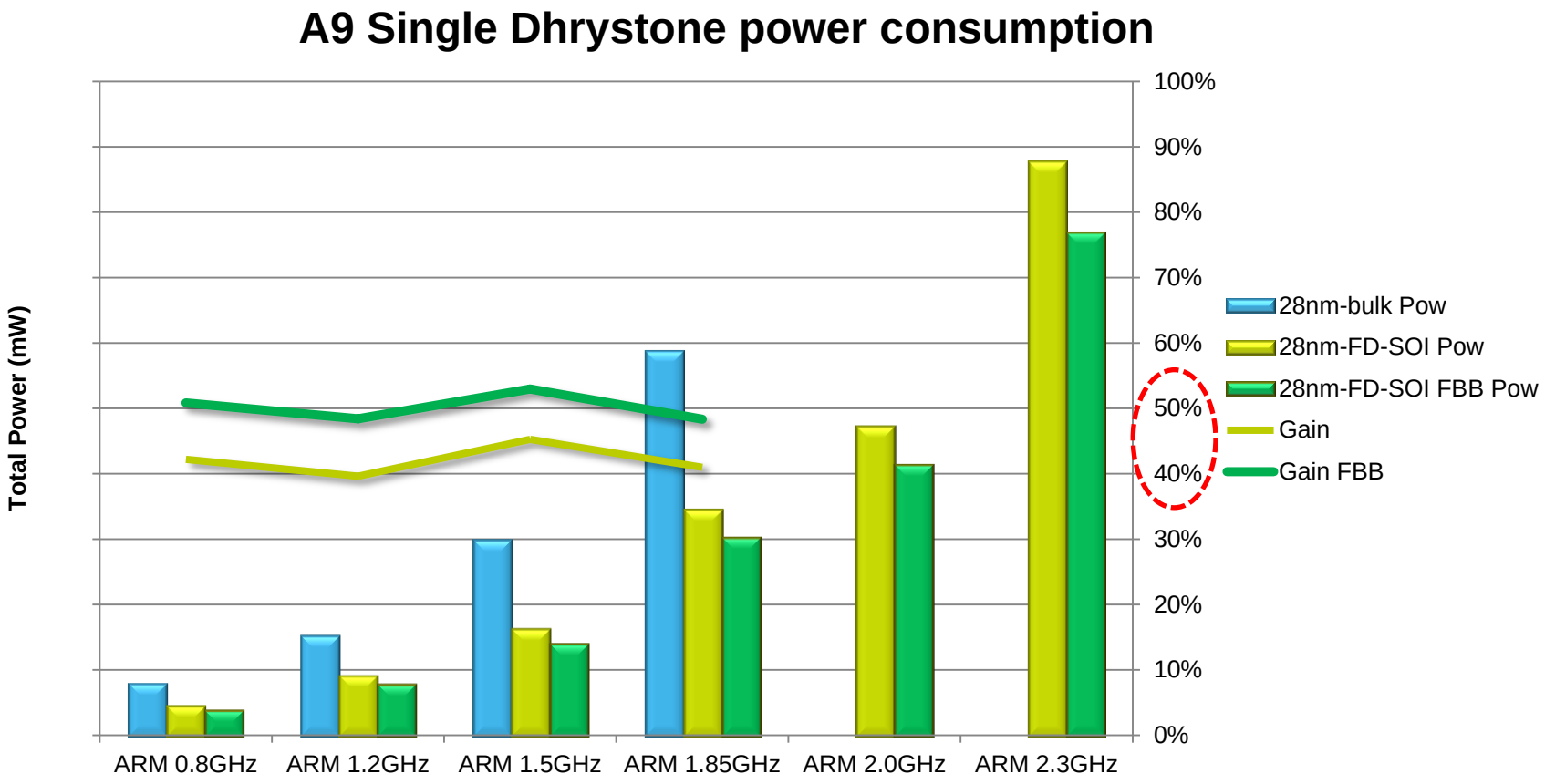
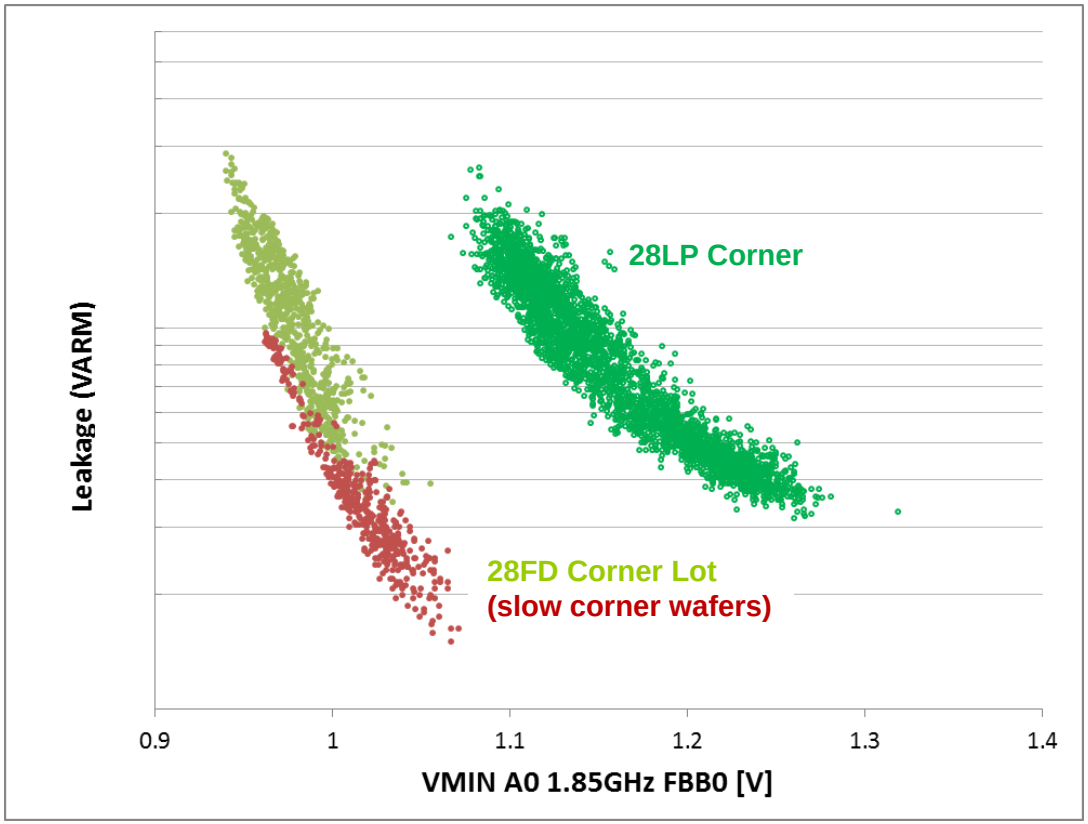
Cortex A9 Power vs. Performances



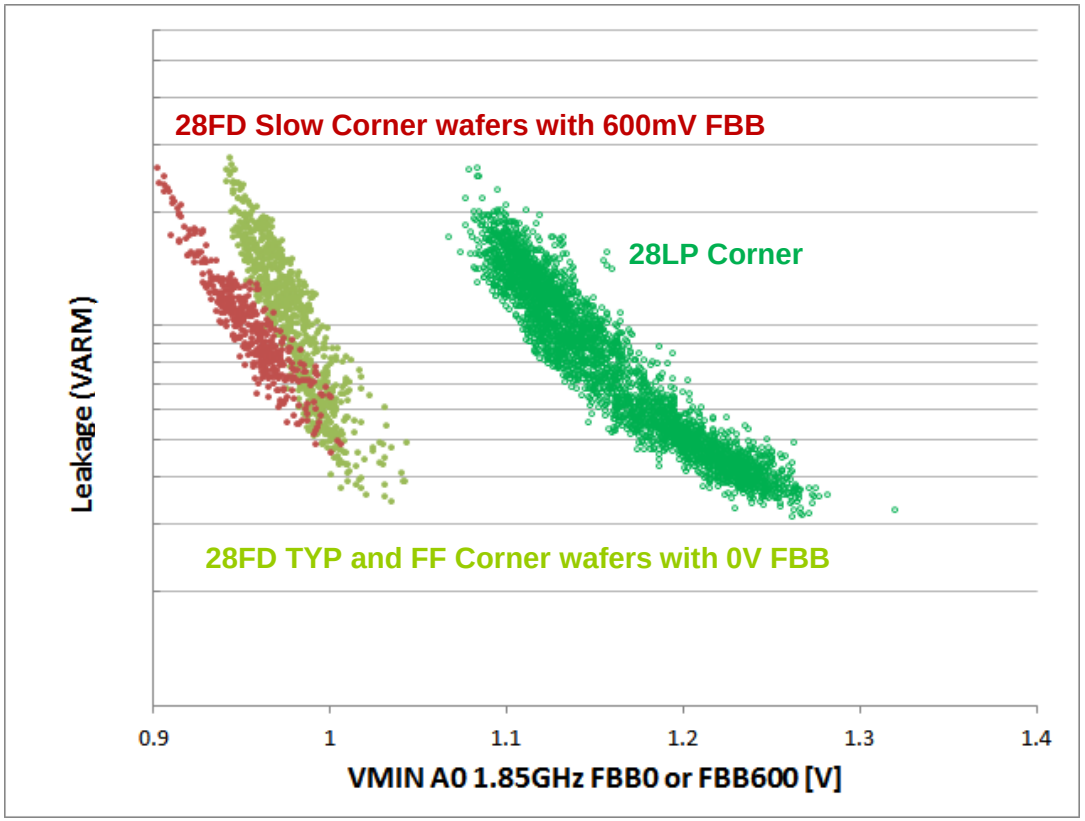
- LVT only block (multi-channel: Lmin to +16nm)
- Measurements done on board at room temperature

Cortex A9 Benchmark 28nm Silicon Results



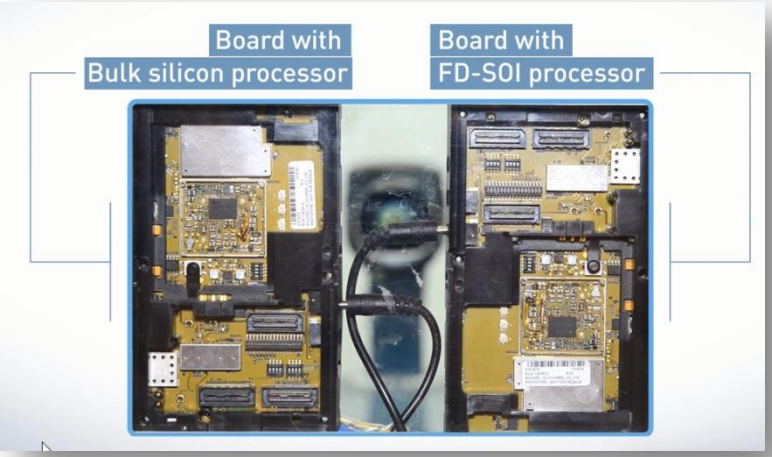
- VMIN for a given frequency (1.85GHz)
  - Vmin search is an EWS metric for Fmax
  - The metric allows a one-to-one benchmark between 28FD and 28LP performances

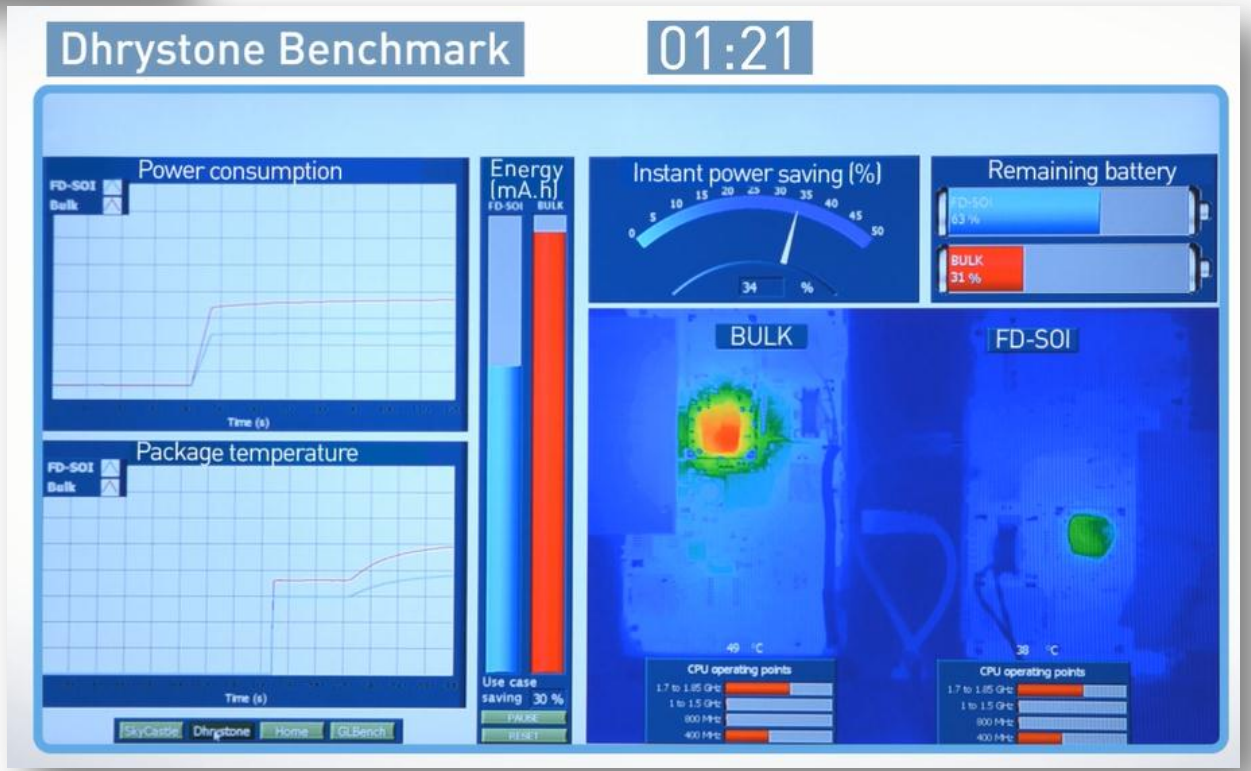
Cortex A9 Benchmark
Process Compensation through FBB



- Applying FBB 600mV enable reaching the target VMIN perfs
  - SLOW Population brought in TT-FF range

Cooler Demo

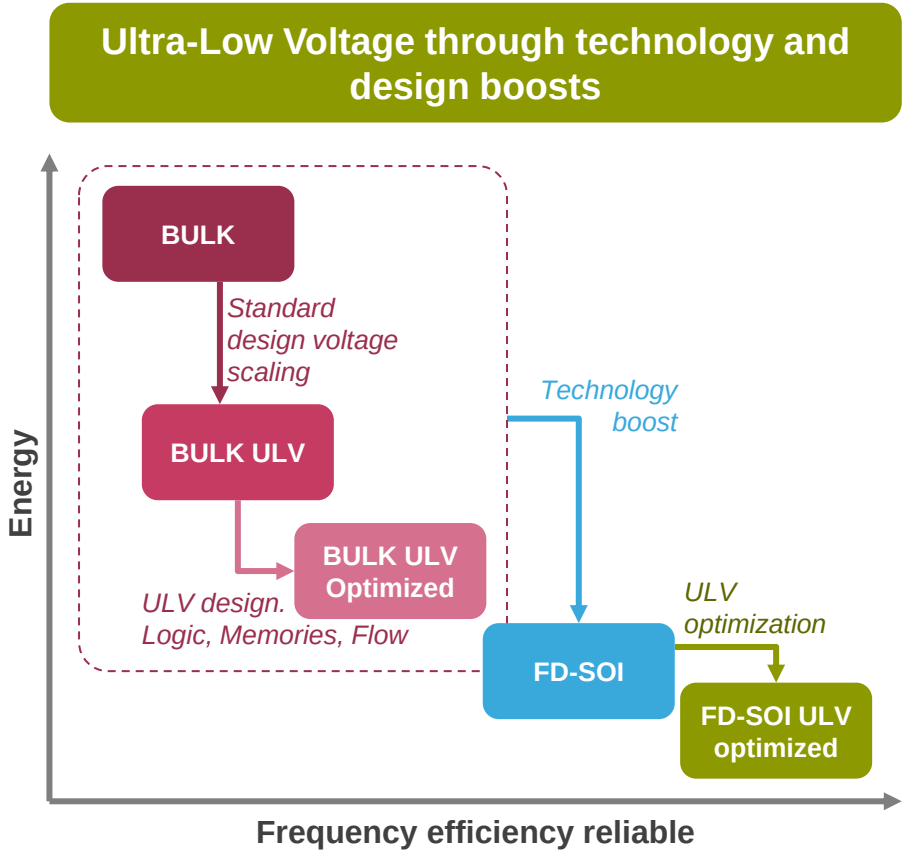

Board with
Bulk silicon processor
Board with
FD-SOI processor


Dhrystone Benchmark
01:21
Power consumption
FD-SOI
Bulk
Time (s)
Package temperature
FD-SOI
Bulk
Time (s)
SkyCastle
Dhrystone
Home
GLBench
Energy (mA.h)
FD-SOI
BULK
Use case saving 30 %
Instant power saving (%)
34 %
Remaining battery
FD-SOI
63 %
BULK
31 %
BULK
FD-SOI
49 °C
38 °C
CPU operating points
1.7 to 1.85 GHz
1 to 1.5 GHz
800 MHz
400 MHz
CPU operating points
1.7 to 1.85 GHz
1 to 1.5 GHz
800 MHz
400 MHz

FD-SOI Technology for Ultra Low Power / Voltage applications

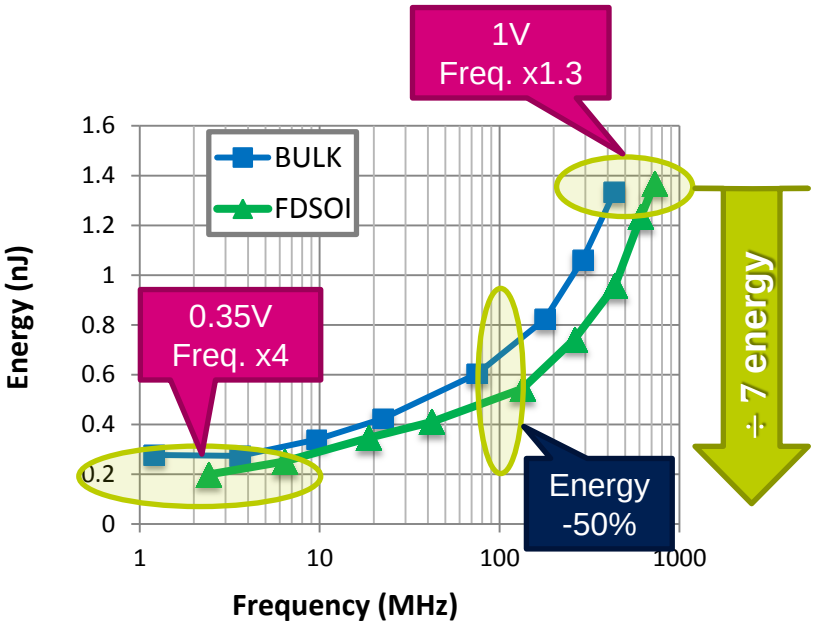
ULV Gains Confirmed in 28 FD-SOI

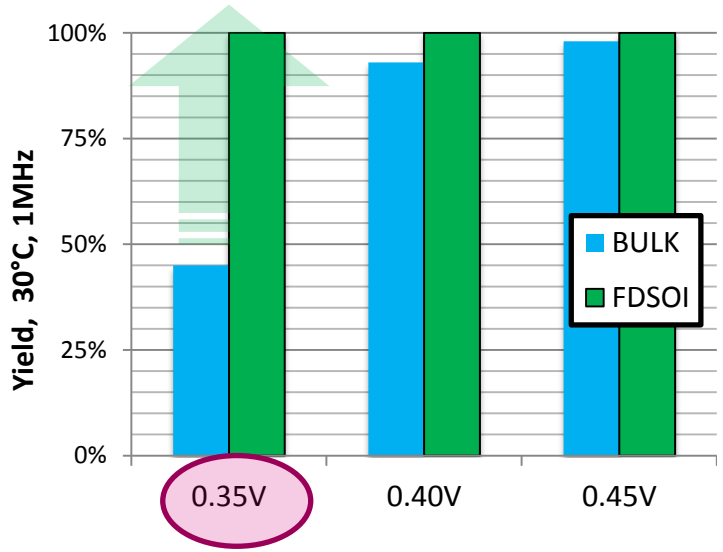
- Intrinsic FD-SOI advantage for ULV
  - Electrostatic control enhancement
  - → speed at low voltage
  - Undoped homogeneous channel
  - → Reduced variability
  - → Lower minimum usable supply voltage
- Specific design solutions to leverage FDSOI outstanding performance at ULV
  - Higher I_{ON} for clock tree
  - FBB for improved energy efficiency and delay



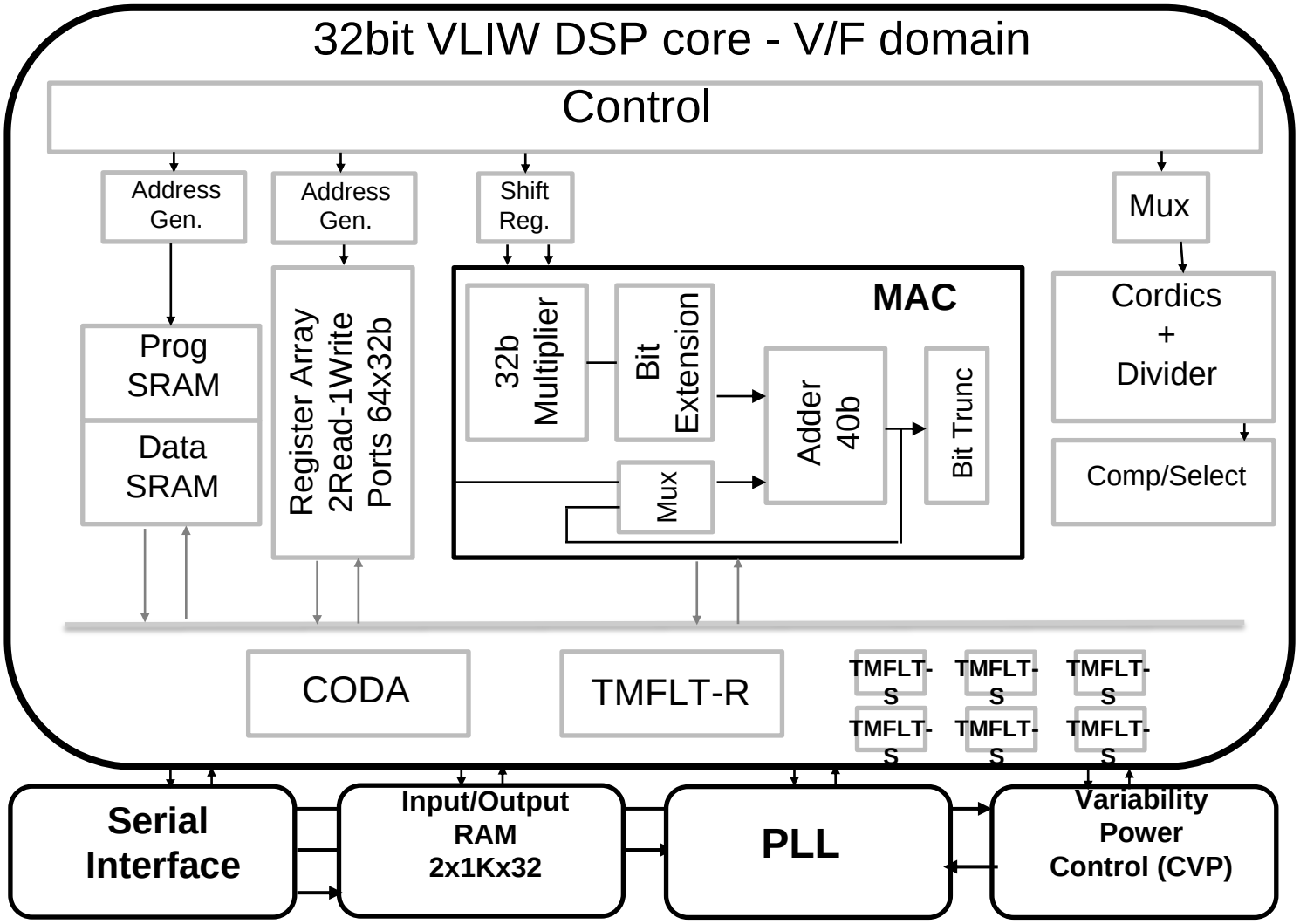
ULV Si Evidences at 28nm

- 2 BCH decoders: 28FD vs. 28LP
  - 252b frame error-decoder
  - Both adopting ULV specific design
- FD-SOI boost at ULV
  - Ultra-wide DVFS
    - From 1 to 700 MHz for 0.35-1.00V
  - Higher frequency at given energy
    - x1.3 to x4
  - Energy saver at given frequency
    - -25% to -50%
- Yielding at lower voltages
  - FD-SOI at 100% yield already at 0.35V
    - 100mV lower than 28LP



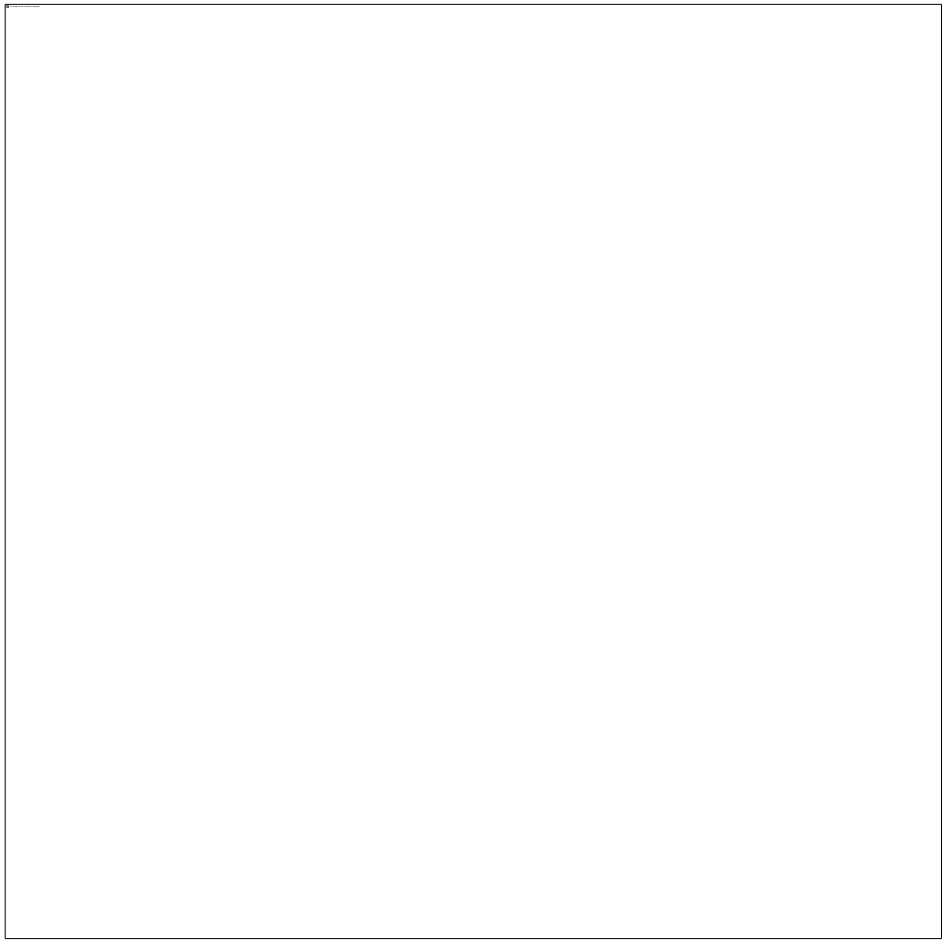


DSP architecture



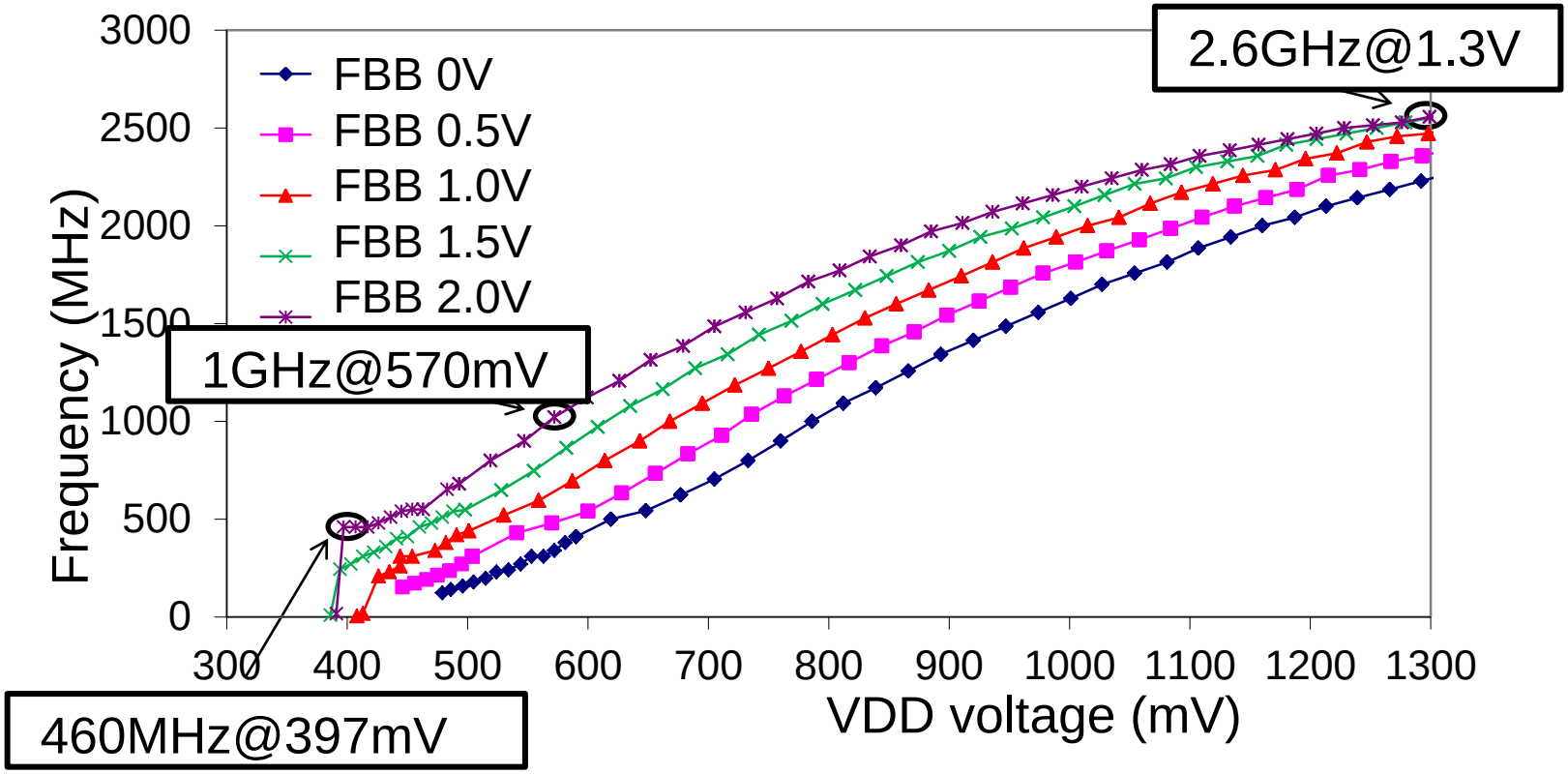
27.1 : A 460MHz@397mV – 2.6GHz@1.3V 32bit VLIW DSP Embedding FMAX Tracking

Chip Micrograph



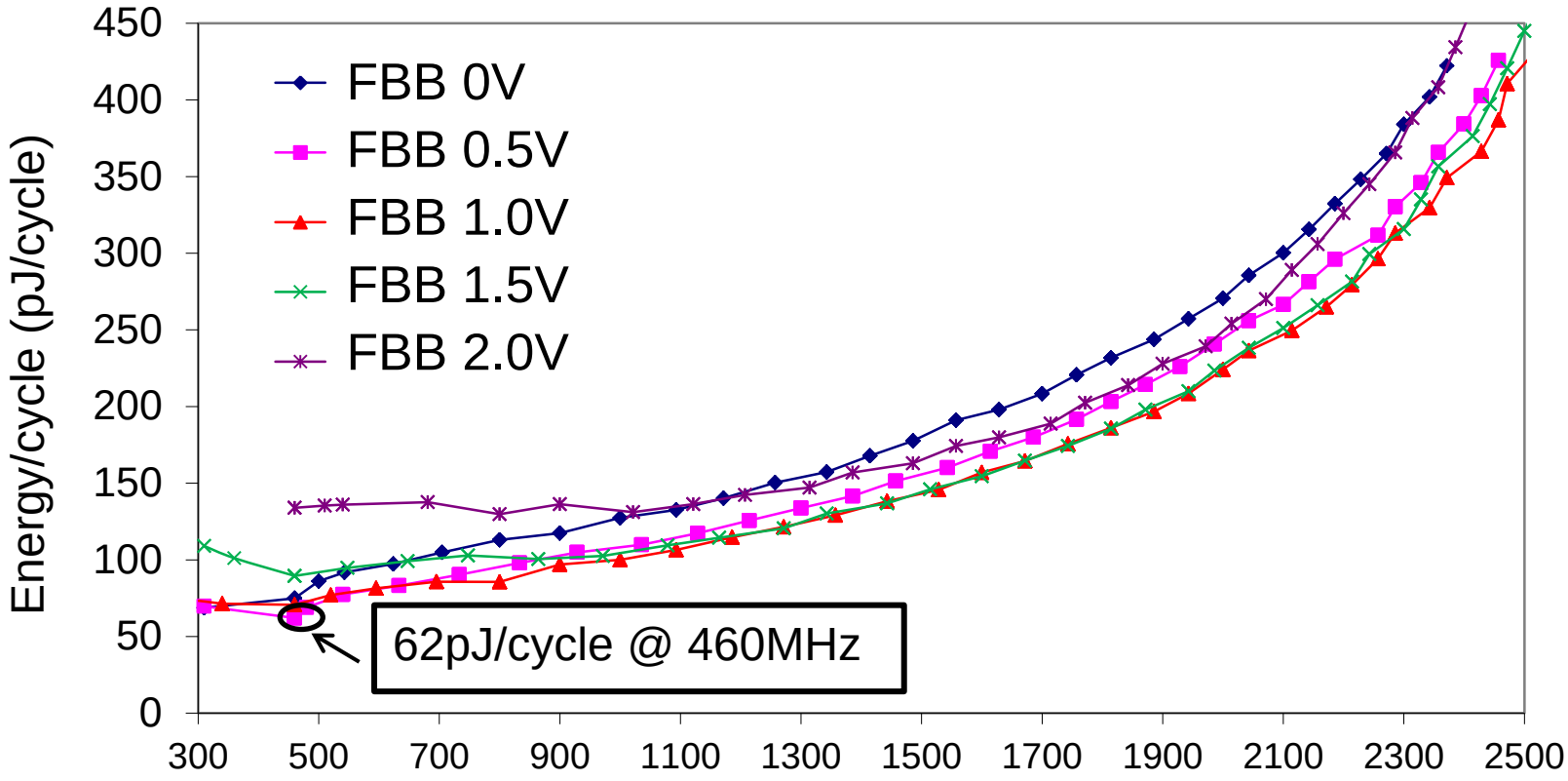
Technology	UTBB FDSOI 28 nm
Transistors	LVT Lmin=24nm
Core area	1 mm²
DSP benchmark	FFT 1024
VDD range	0.397V-1.3V
VBB range	0V/±2V

DSP speed performance measured results



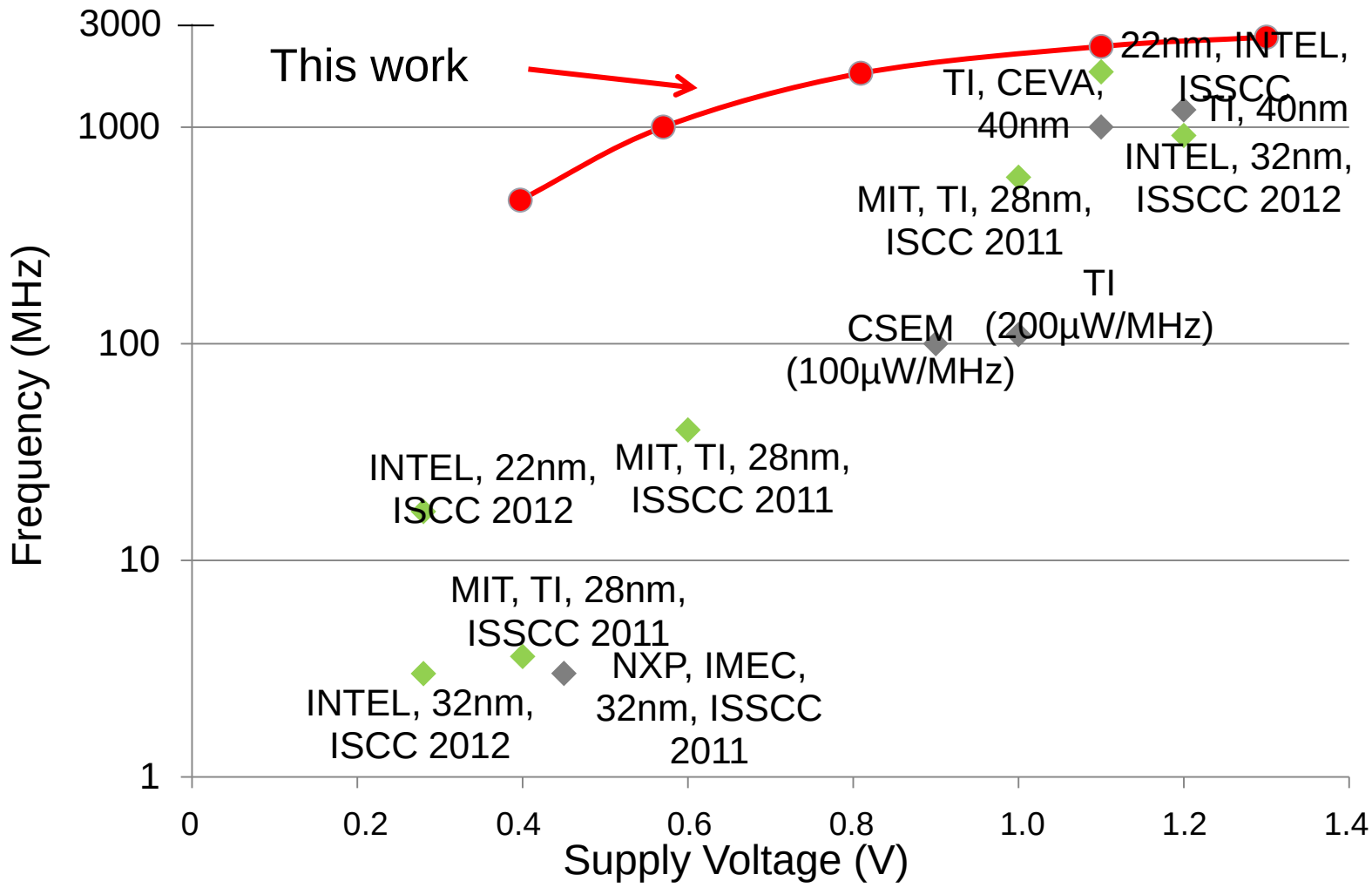
- FBB up to +2V and F_{MAX} tracking :
  - ↗ frequency up to 460MHz at minimum voltage

DSP energy performance measured results



- For a fixed voltage supply :
  - Lowest energy at 460MHz
  - Power consumption : 370mW at 1V

Comparison with State of the Art WVR



27.1 : A 460MHz@397mV – 2.6GHz@1.3V 32bit VLIW DSP Embedding FMAX Tracking

Thank You!