Near-Threshold Computing on Heterogeneous Multicore Architectures

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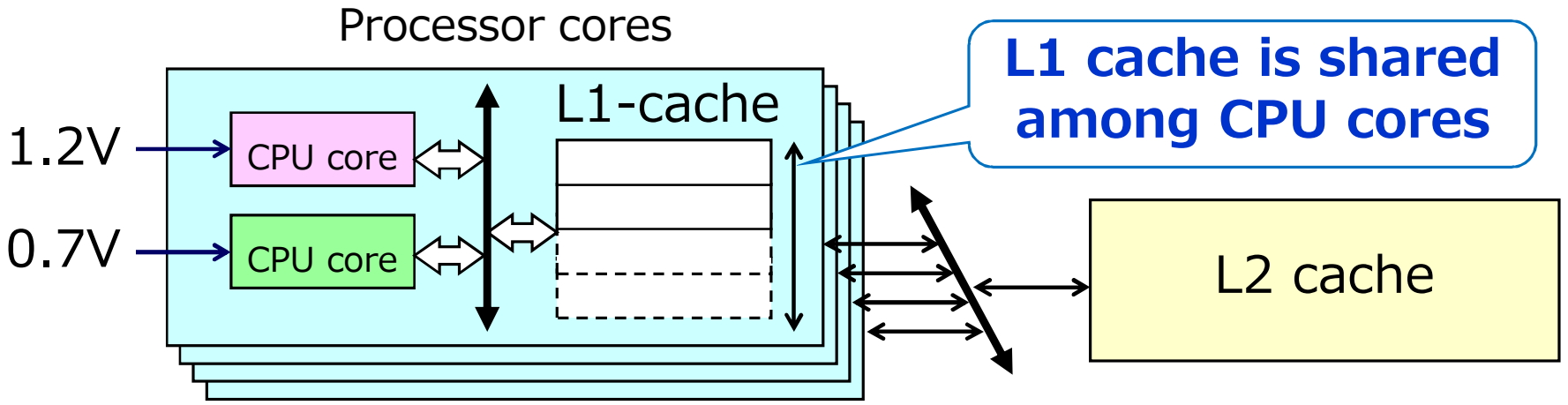
My Talk in MPSoC 2009

- A concept of Multi-Performance Processor (MPP) is presented
- Integrating multiple same-ISA CPU cores in a processor core
  - Only one CPU core is activated at a time
- Pros: Each CPU core is optimized for its frequency and V_{DD}
  Very low-overhead core migration is possible
- Cons: Large area overhead involved
  Multiple on-chip V_{DD}s are needed



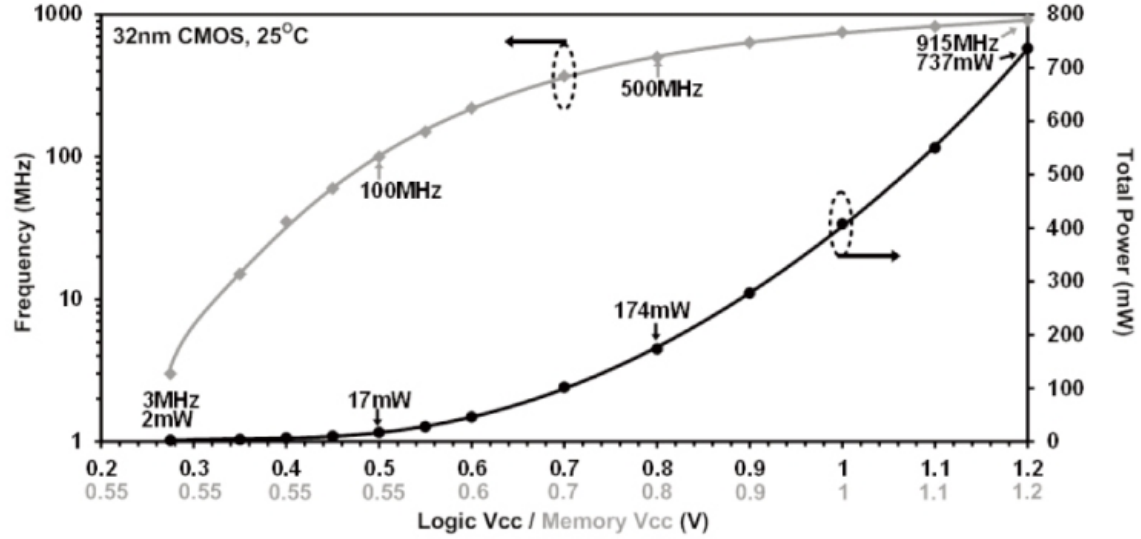
T. Ishihara, "Real-Time Dynamic Voltage Hopping on MPSoCs," MPSoC 2009, Savannah.

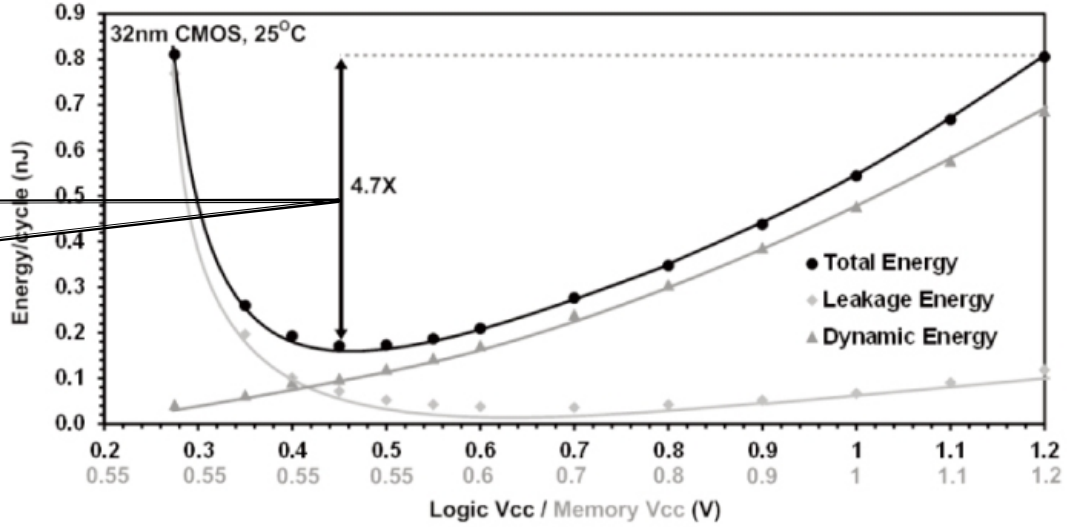
Motivation

- Highest energy efficiency is obtained at **near-threshold voltage** (NTV)

Reference: Research@Intel 2012, June 26, 2012

32nm test processor "Claremont"

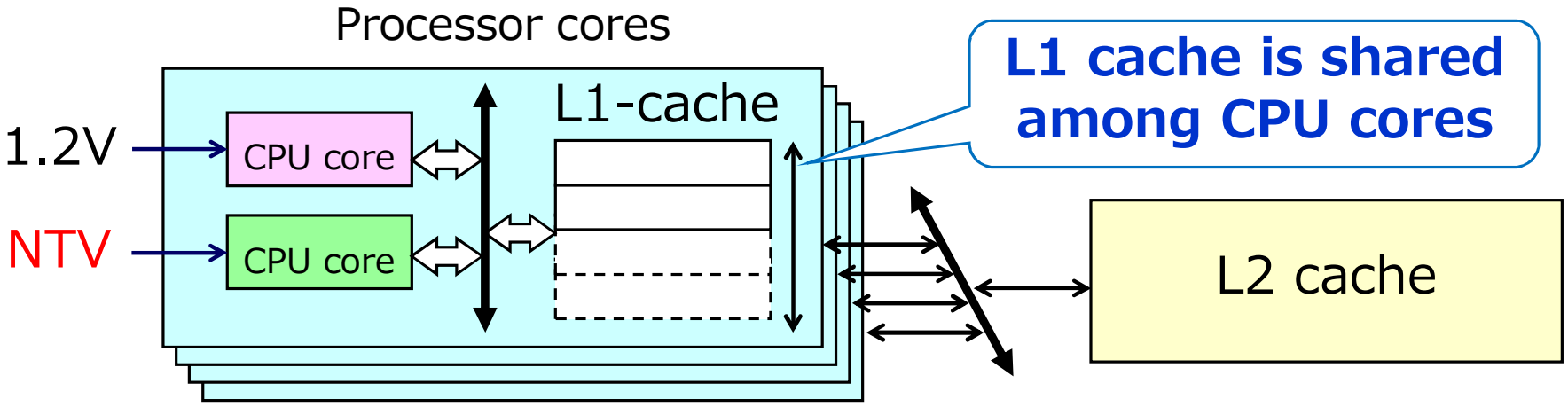




4.7x better energy efficiency at 0.45V

Approach

- A concept of Multi-Performance Processor (MPP) is presented
- Integrating multiple same-ISA CPU cores in a processor core
  - Only one CPU core is activated at a time
- High peak performance
- Low average power

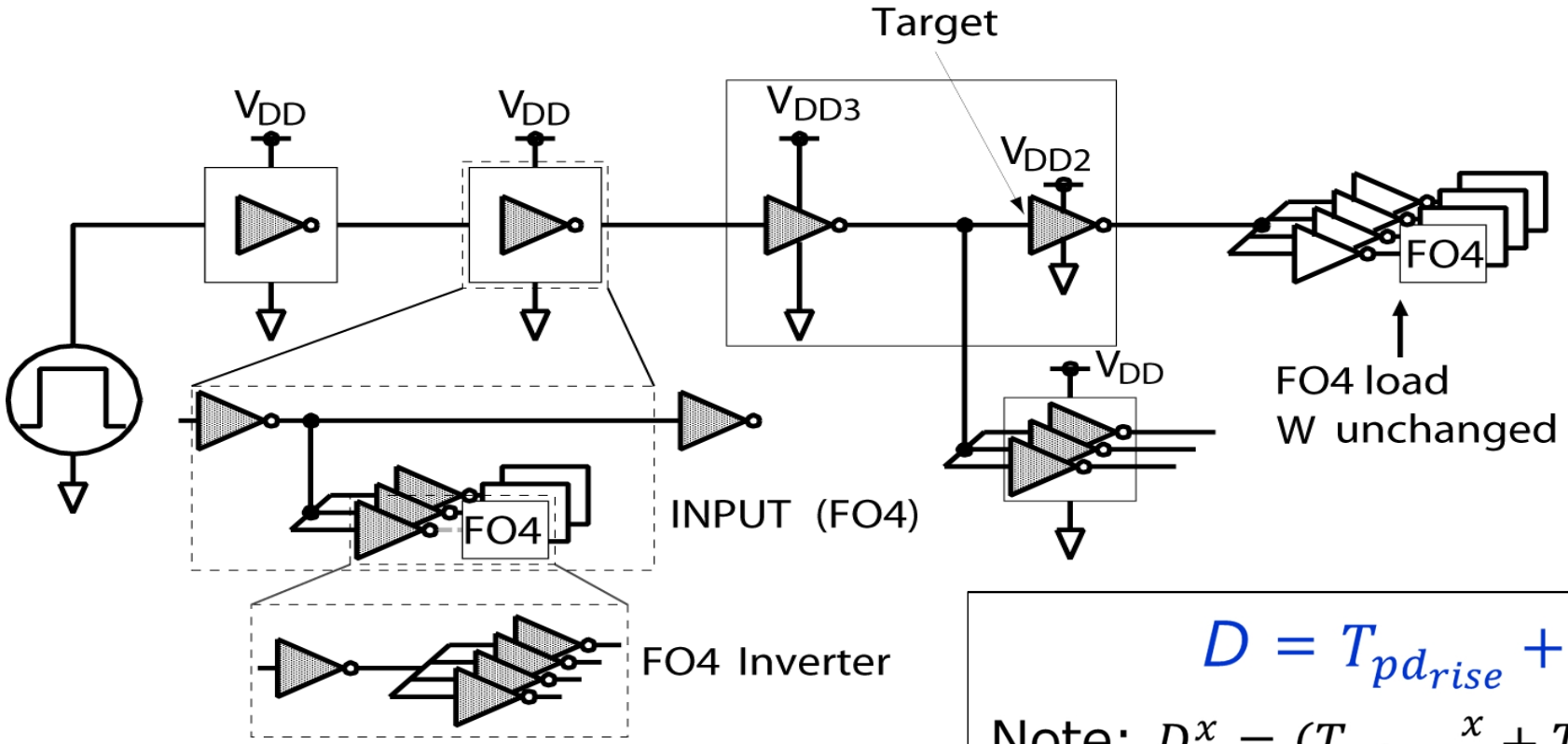


T. Ishihara, "Real-Time Dynamic Voltage Hopping on MPSoCs," MPSoC 2009, Savannah.

More Progressive Approach

- Optimize the gate width of target standard cells for NTV operation
  - Objective function: ED^x

E = Total energy consumed through V_{DD2} and V_{DD3}



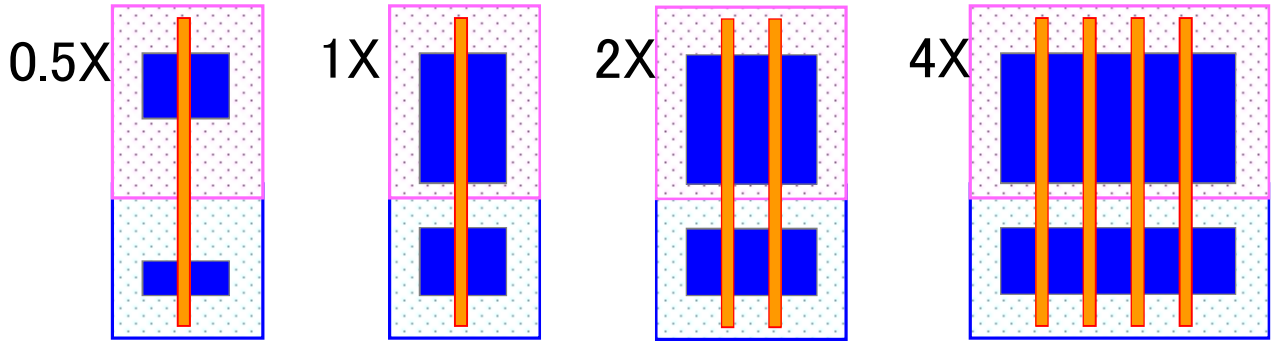
$$D = T_{pd_{rise}} + T_{pd_{fall}}$$

Note: $D^x = (T_{pd_{rise}}{}^x + T_{pd_{fall}}{}^x)$

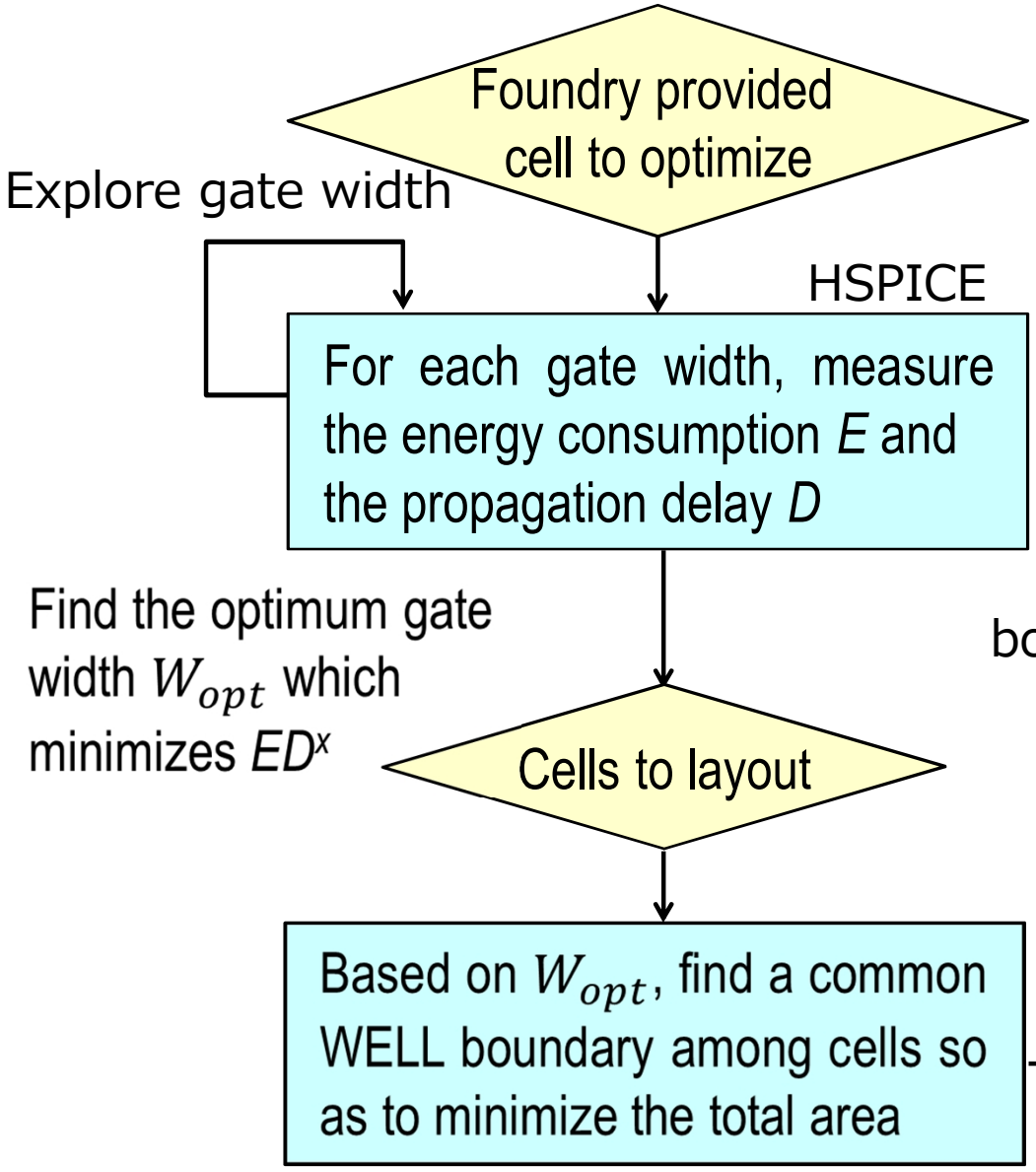
Target Standard Cells

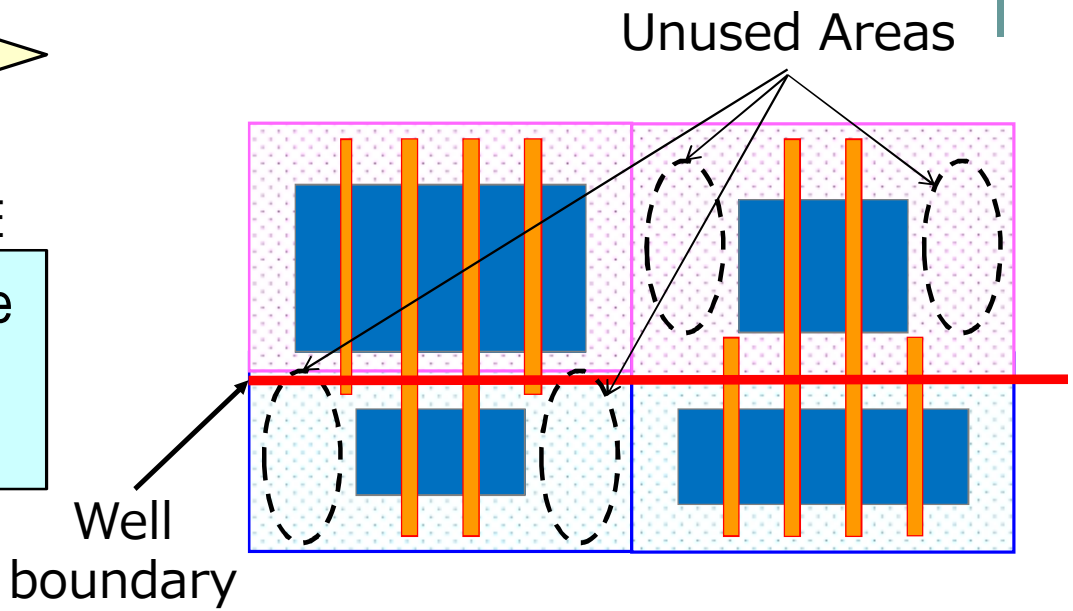
- Optimize the transistor size of foundry-provided standard cells (63 cells) for 0.6V operation
  - Commercial 65nm process technology is used
    - Nominal V_{DD} : 1.2V, V_{th} : around 0.5V
  - Logic Type: INV, BUF, NAND2, NOR2, AND2, OR2 AOI21, OAI21, AOI22, OAI22
  - Drive Strength: 0.5X, 1X, 1.5X, 2X, 3X, 4X, 6X, 8X, 10X, 12X, 16X

Layout examples)



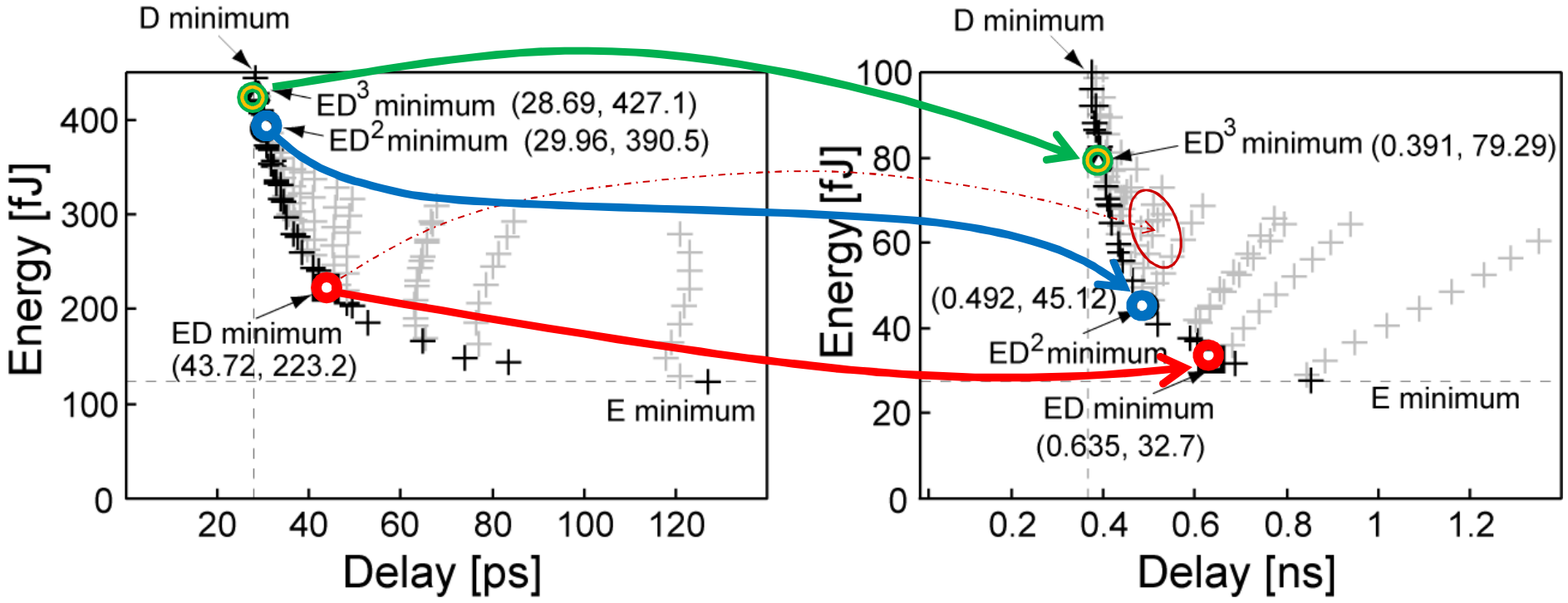
Optimization flow





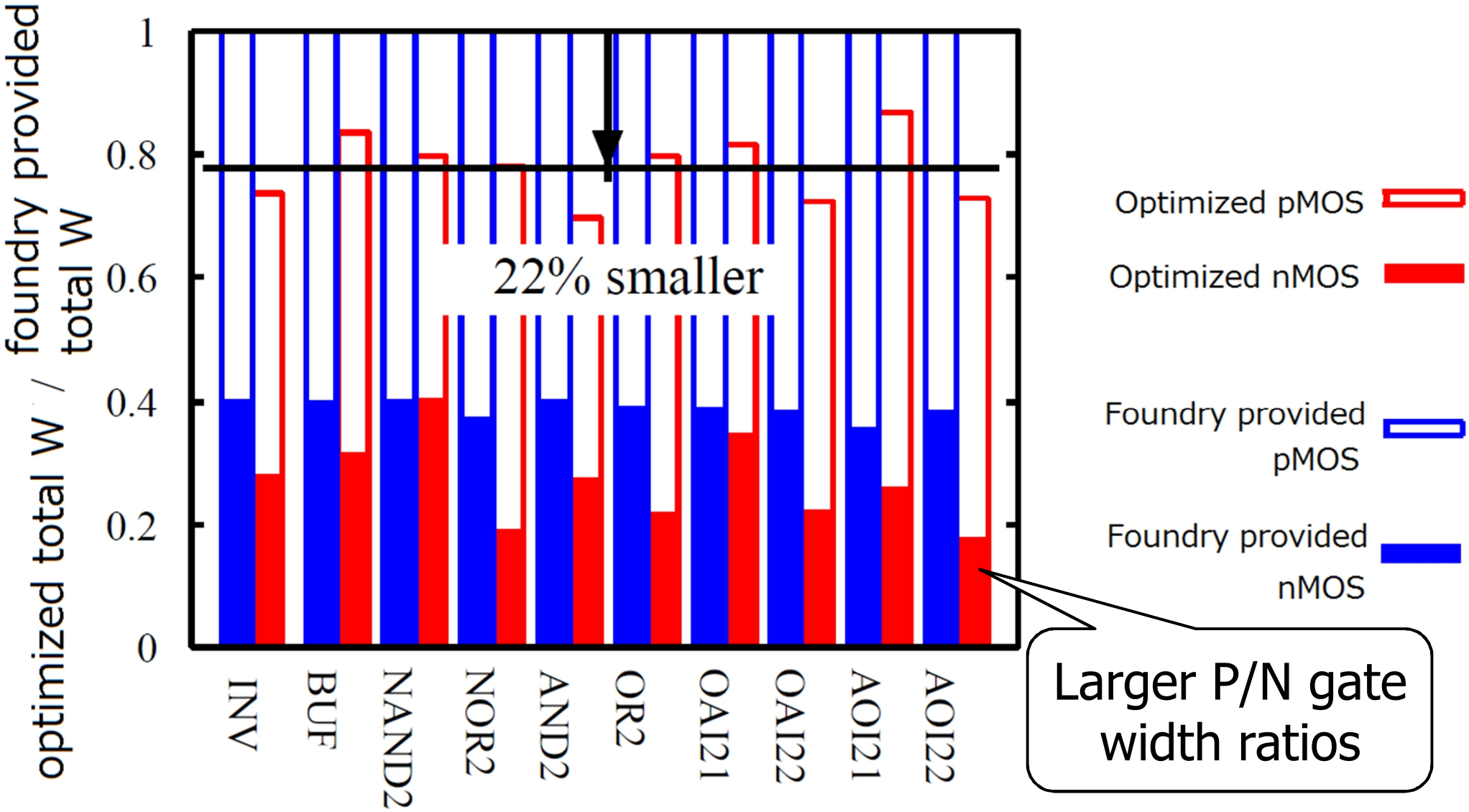
Pareto Optimal Curve

- A set of ED^x optimal points ⇒ Pareto optimal curve
- Foundry-provided cells are close to the Pareto optimal curve in nominal voltage operation
- Far from Pareto optimum in NTV operation



INV 16X

Results of P/N Width Optimization



Experimental Setup

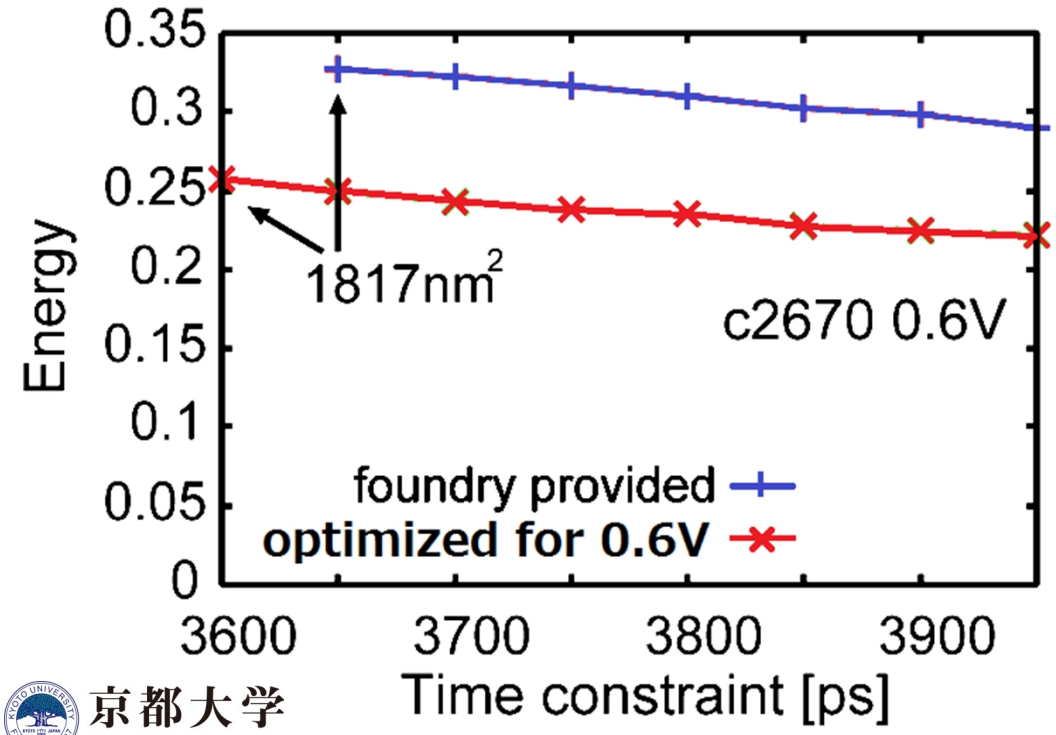
- Target: practically large scale circuits selected from ISCAS'85 benchmark suite
- Objective: evaluating the NTV library cells
  - Improvement of energy efficiency in individual cells does not always lead to an improvement of energy efficiency in large scale circuits
  - evaluating not only the energy consumption, but also area and performance of the circuits
  - 12-bit ALU, 32-bit adder / comparator etc.

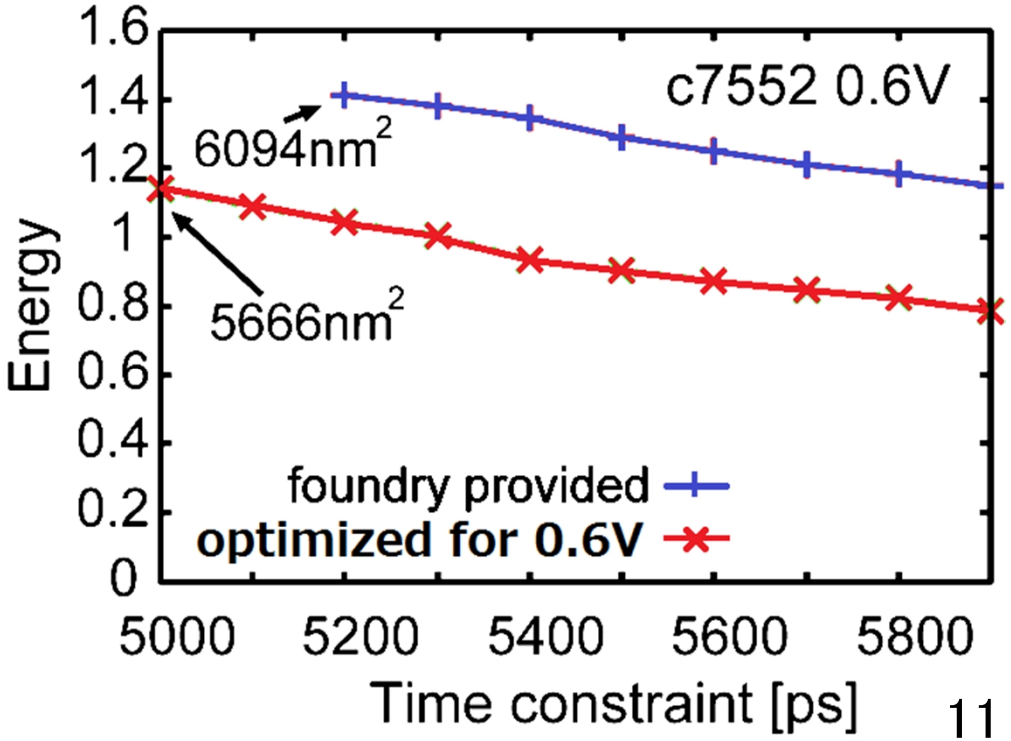
Synthesis Results of ISCAS'85 (1/2)

Energy consumed in NTV (0.6V) operation

Circuits synthesized with the cells optimized for NTV

- achieve 23% energy reduction for a given constraint
- satisfy more strict timing constraints



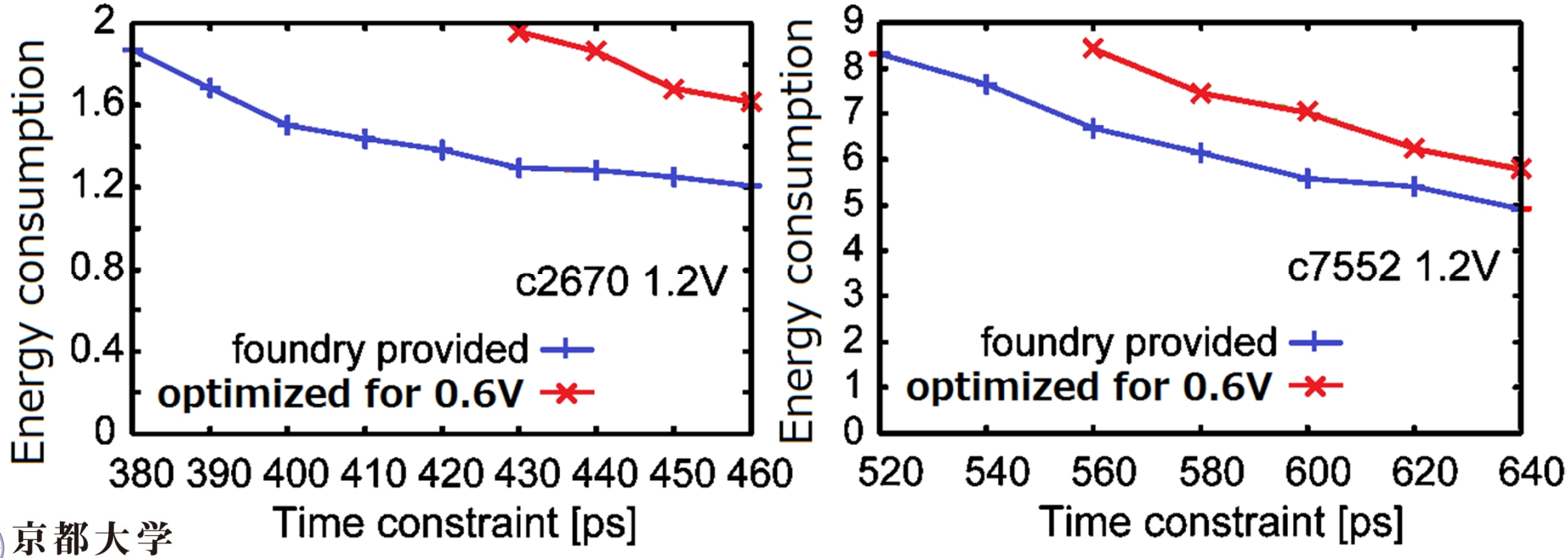


Synthesis Results of ISCAS'85 (2/2)

Energy consumed in nominal V_{DD} operation

Circuits synthesized with the foundry-provided cells

- always achieve lower energy consumption
- satisfy more strict timing constraints



Conclusion

- Optimization method for near-threshold voltage is presented.
- The cells optimized for NTV reduce the energy consumption of benchmark circuits operated with NTV by 23% on average.
- Delay and area of the circuits are reduced.
- Future work
  - Improve the optimization procedure
  - Apply the method to the MPP design