MPSoC2015

How to Develop 4K Realtime HEVC Encoder by FPGA

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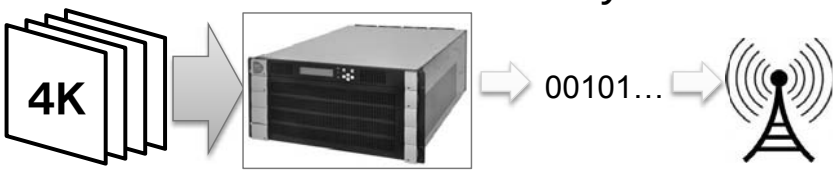
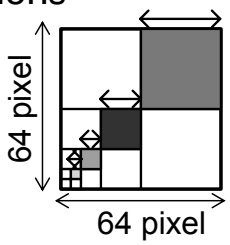
HEVC real-time encoder for 4K video broadcasting

- High Efficiency Video Coding (HEVC) is proposed
  - It achieves 2x compression ratio than current video codec H.264/AVC.
  - 4K/8K video transmission using HEVC is expected
- Hardware real-time encoder is necessary for broadcasting

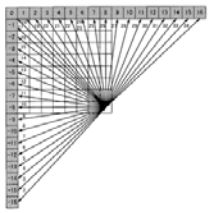


HEVC Encoder

- HEVC algorithm introduces variety of complicated coding options
  - E.g. various block sizes and predictions
  - Encoders should explore optimal one and use it.



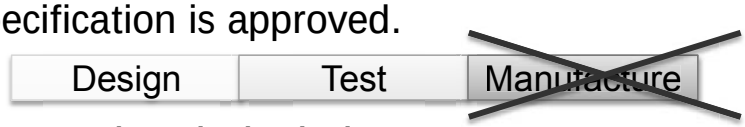
Various Block Sizes



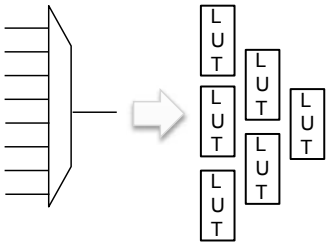
Various predictions

Adoption of FPGA: pros. and cons.

- ○ FPGA as a product can reduce Time-to-Market
  - No manufacturing time after design phase
  - Designers can verify the system using real input videos.
  - The only solution in order to release product just 1 year after HEVC specification is approved.



- × The clock frequency of FPGA is relatively low
  - At most 200MHz -> a few cycles per pixel block
  - Parallelism design is important.



- × It is difficult to implement huge multiplexers.
  - Increase of multiplexers
  - HEVC's various options often introduce huge multiplexers to select various inputs and outputs

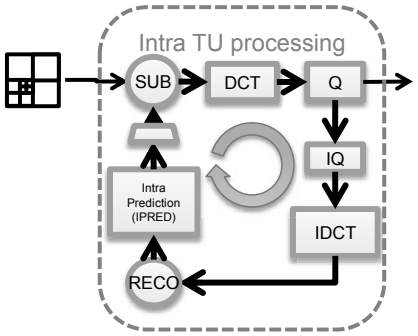
2 technologies to realize HEVC encoder on FPGA

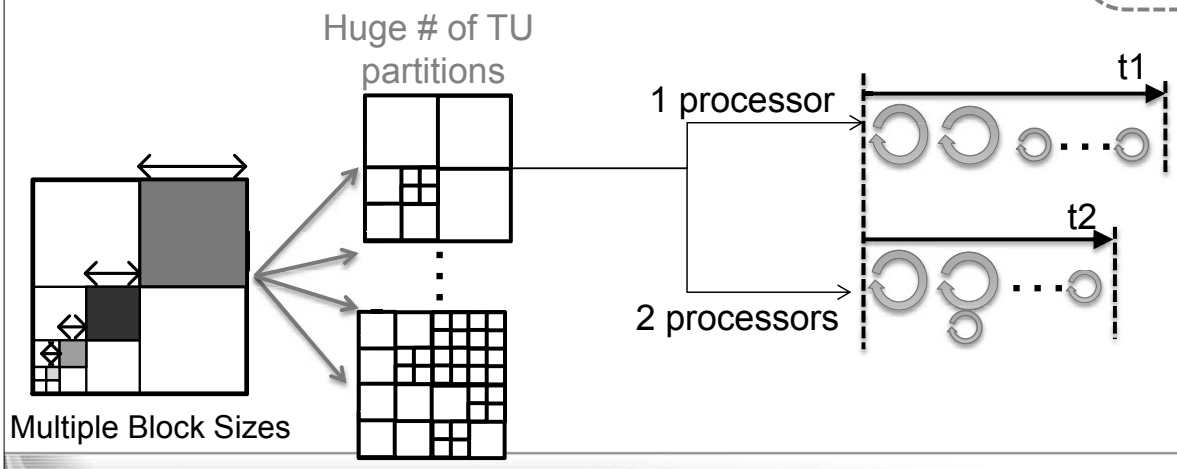
- A parallel scheduling system for transformation
  - Technology to overcome low frequency by parallelization
  - Introduces parallelizing scheduler and

- An intra prediction image generator method
  - Technology to reduce huge multiplexers

A parallel scheduling system for transformation

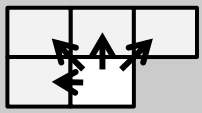
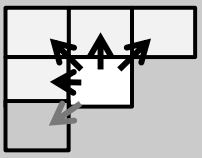
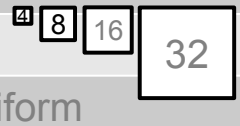
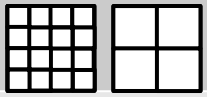
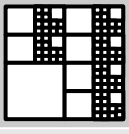
- Intra Transformation Unit (TU) processing is difficult to parallelize
  - It has dependency among neighbor blocks
  - There is various patterns on block partitioning -> appropriate parallel scheduling varies
- Problem for parallel execution design
  - How to schedule for all partitions?
  - How to explore appropriate parallelism?





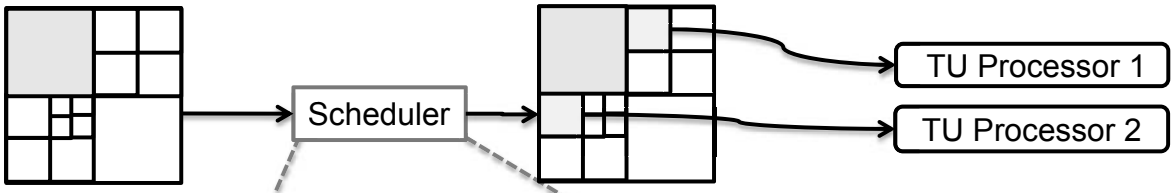
Difficulty comparison of H.264/AVC and H.265/HEVC

- Parallelism is behind complicated TU partitions and dependencies

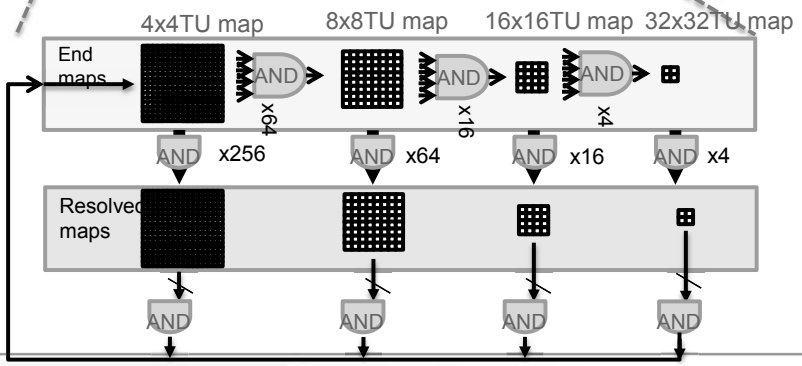
	H.264/AVC	H.265/HEVC
TU dependency	Low 	High 
TU size	2 sizes 	4 sizes 
TU partition patterns	Uniform partition of 16x16 (only 2 patterns) 	Non-uniform partition of 64x64 (> 1 million patterns) 
Parallelism	Obvious 	Depends on the TU partitions determined on-line.

How to schedule? => Parallel scheduler specialized for TUs

- The scheduler automatically output “next” blocks to process when registered “processed position of TUs”.

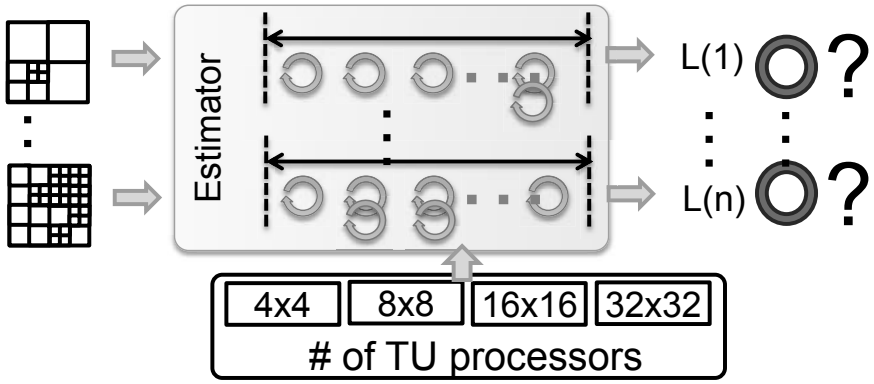


- The scheduler consists of only register maps and ANDs
  - Simple and a little area overhead

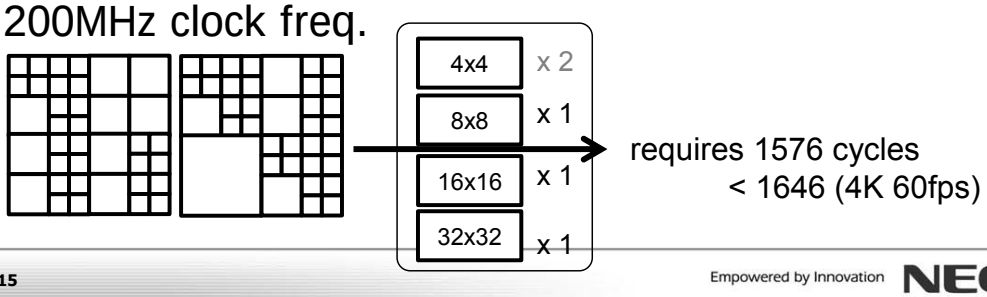


How to explore appropriate parallelism? => Performance estimation

- Given the processing time for each TU size (4x4, 8x8,16x16, 32x32), Estimator simply calculate performance considering parallelism of TUs by the proposed scheduler



- Example: Found two worst case partitions meet the constraint for 4K/60fps on 200MHz clock freq.

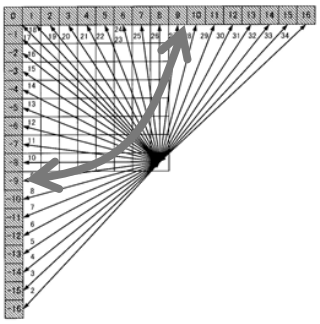


An intra prediction image generator method

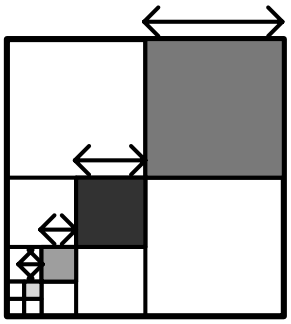
- In HEVC, # of intra prediction direction is 33 (from 9 in H.264/AVC)
  - For block sizes from 4x4 to 32x32

HEVC Intra Image Prediction

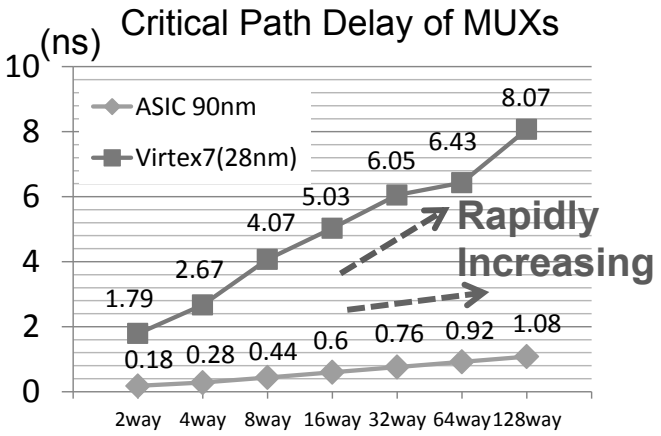
33 directions



Multiple Block Size



Defects of FPGA



Algrorithm : **High-Flexibility**

FPGA : **MUX bottleneck**

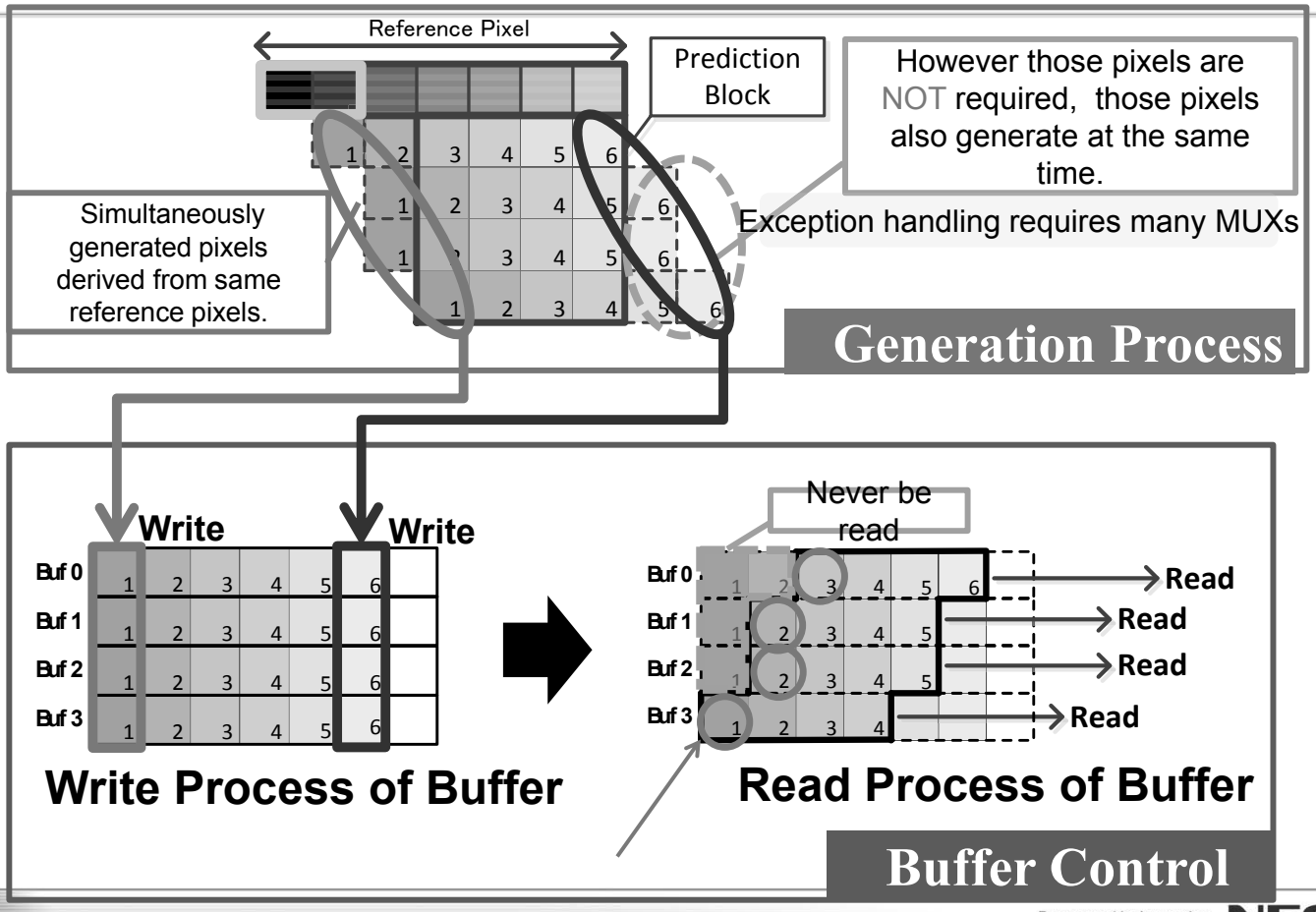
Key Concepts to eliminate MUXs

Simultaneous generation prediction pixels
by using minimum number of MUXs.

- As a result, generate order varies by the prediction direction.

Introduction of re-shaping buffer made of BRAM
for the sake of consistency of generation order.

System Architecture



Evaluation Results

✓ Resource Usage

	Raster scan architecture	**Proposed**	Ratio
Slice LUTs	3693	**1910**	-51%
Slice Registers	1211	**2508**	100%†
F7 MUX	329	**97**	-71%
F8 MUX	96	**48**	-50%
BRAM	0	**16**	N/A
DSP48	64	**64**	0%

✓ Maximum Frequency (MHz)

	Raster scan architecture	Proposed	Ratio
Maximum Frequency.	104.3	149.2	43%

Summary

- We proposed 2 technologies to provide 4K/60p real-time HEVC encoder with broadcasting quality.

- A parallel scheduling system for transformation
  - To overcome low frequency by utilizing parallelism hidden by complicated block dependencies
- An intra prediction image generator method
  - To avoid performance degradation by huge multiplexers introducing “re-shaping buffer”

Empowered by Innovation