Thermal Effects in Silicon-Photonic Interconnect Networks

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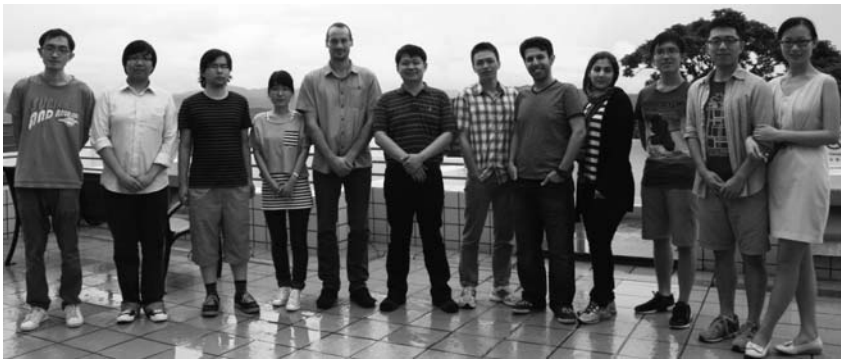

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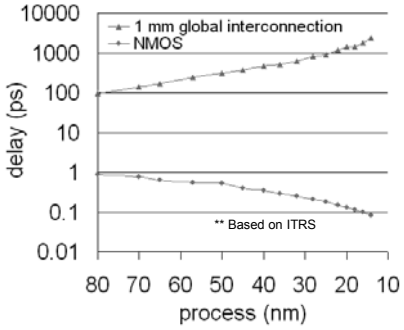
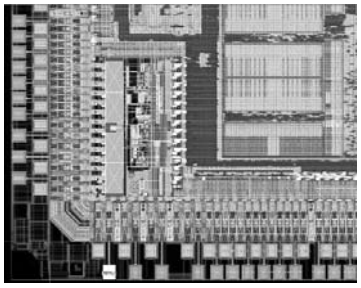
HUAWEI

Performance and Power Wall of Electrical Interconnects

- More cores require more communications
  - Hundreds on a chip and thousands in a rack
  - Cisco QuantumFlow (40), Intel Phi (61), Tilera Tile (72), Cisco SPP (188), PicoChip (300) …
- Higher power consumption
  - Dynamic and leakage power of drivers and buffers
  - Kilowatts of power by 2020*
- Larger latency
  - Multiple clock cycles are required to cross a chip
- Tighter chip I/O bandwidth
  - High pin count, packaging cost, and expensive PCB design

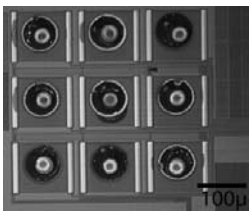
*R.G. Beausoleil, *et al.*, "Nanoelectronic and Nanophotonic Interconnect," Proceedings of the IEEE, Feb. 2008.





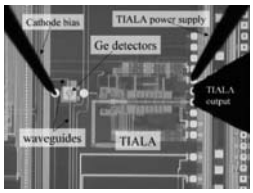
Optical/Photonic Interconnects

- Photonic technologies have been successfully used in WAN, LAN, and board level
  - Showed strengths in multicomputer systems and Internet core routers
- Base on waveguide and microresonator (MR)
  - Silicon based and CMOS compatible
  - MR is as small as 3μm in diameter
  - 30ps switching time has been demonstrated
- Commercialization efforts
  - Demonstrated by IBM, Intel (Omni-Scale), HP (Machine), NEC, Fujitsu, Oracle (UNIC/DARPA), NTT, STMicro, Huawei …
  - Startups: Luxtera, Lightwire/Cisco, Kotura/Mellanox, Caliopa/Huawei, Aurrion, OneChip, Skorpios …



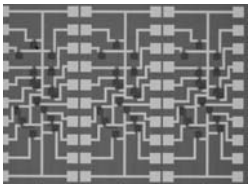
VCSEL Array

J. M. Perkins *et al.*, "Full Recess Integration of Small Diameter Low Threshold VCSELs within Si-CMOS ICs", Optics Express 2008



Integrated OE Interface

G. Masini, *et al.*, "A 1550nm 10Gbps monolithic optical receiver in 130nm CMOS with integrated Ge waveguide photodetector", IEEE International Conference on Group IV Photonics, 2007



On-Chip Optical Routers

R. Ji, J. Xu, L. Yang, "Five-Port Optical Router Based on Microring Switches for Photonic Networks-on-Chip", IEEE Photonics Technology Letters, March, 2013

A Different "Building Material"

- Advantages
  - Ultra-high bandwidth
  - Low propagation delay
  - Low propagation loss
  - Low sensitivity to environmental EMI
- Challenges
  - Thermal sensitivity
  - Crosstalk noise
  - Process variations
  - Electrical/optical conversion overheads
  - Optical signals are difficult to "buffer"

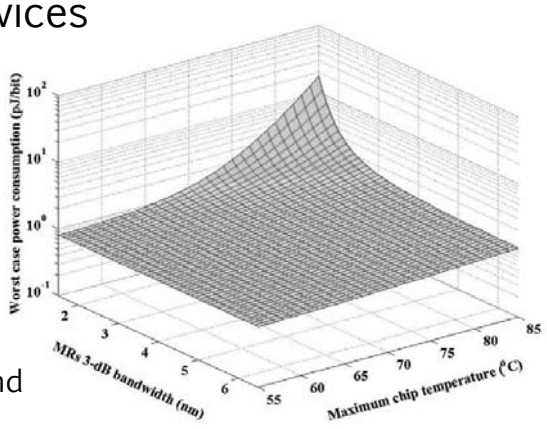
Stone
Solkan Bridge
Slovenia, 1906

Steel
Cold Spring Bridge
USA, 1963

Steel
Tsing Ma Bridge
Hong Kong, 1997

Optical Thermal Effects

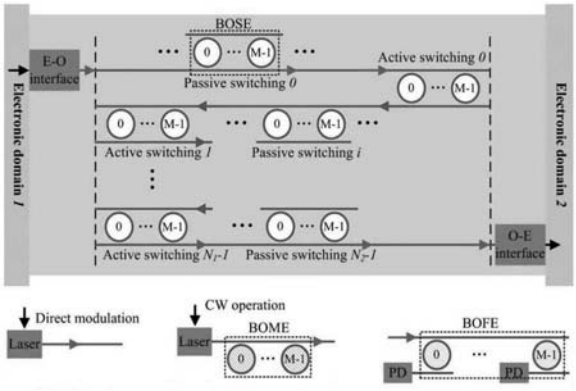
- Thermal sensitivity is a key issue of photonic devices
- Thermal effects can cause
  - Laser power efficiency degradation
  - Temperature-dependent wavelength shifting
  - Optical power loss caused by wavelength mismatch
- System-level thermal model needs to consider
  - Laser temperature-dependent wavelength shifting and power efficiency
  - Microresonator temperature-dependent wavelength shifting and optical power loss
  - Waveguide propagation loss variation
  - Photodetector sensitivity and dark current
  - Chip temperature distribution



* Yaoyao Ye, Zhehui Wang, Peng Yang, Jiang Xu, *et al.*, "System-Level Modeling and Analysis of Thermal Effects in WDM-Based Optical Networks-on-Chip," IEEE TCAD 2014
* Yaoyao Ye, Jiang Xu, *et al.*, "System-Level Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip", IEEE TVLSI 2013
* Yaoyao Ye, Jiang Xu, *et al.*, "Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip", ISVLSI 2011

Link-based Optical Interconnect Model

- Any optical interconnect network is a combination of optical links
- An optical link includes
  - Laser source
  - Basic optical modulation element (BOME)
  - Basic optical switching element (BOSE)
  - Basic optical filter element (BOFE)
  - Photodetector (PD)
- The necessary condition for an functional optical link
  - Optical power reaching the PD must be larger than the PD sensitivity



M-wavelength WDM optical link model

$$10\log\left(\left(I-\alpha-\beta\left(T_{\mathrm{VCSEL}}-T_{\mathrm{th}}\right)^2\right)\left(\varepsilon-\gamma\cdot T_{\mathrm{VCSEL}}\right)\right)-L_{\mathrm{BOME}\_x}-\sum_{i=0}^{N_1-1}L_{\mathrm{BOSE\_active}\_k}-\sum_{j=0}^{N_2-1}L_{\mathrm{BOSE\_parking}\_j}-L_{\mathrm{BOFE}\_x}-L_{\mathrm{WG}}\geq S_{\mathrm{RX}}$$

Laser Thermal Modeling

- Emission wavelength λ_{VCSEL}

$$l_{\mathrm{VCSEL}}\cdot n_{\mathrm{ave}}=m_{\mathrm{VCSEL}}\cdot\lambda_{\mathrm{VCSEL}}/2$$

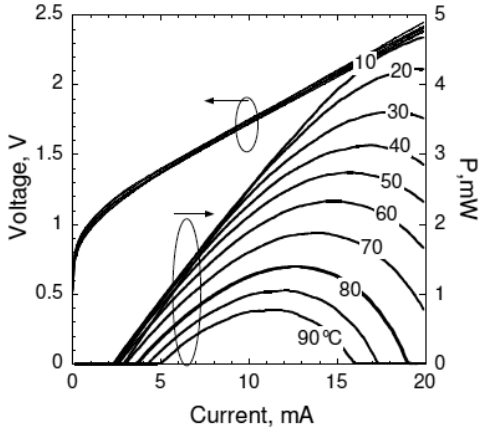
- Temperature-dependent wavelength shift

$$\lambda_{VCSEL}=\lambda_{VCSEL\_min}+\rho_{VCSEL}(T_{VCSEL}-T_{min})$$

- Output power under temperature T_{VCSEL}

$$P_{TX}=(I-\alpha-\beta(T_{VCSEL}-T_{th})^2)(\varepsilon-\gamma\cdot T_{VCSEL})$$

- On-chip laser source, T_{VCSEL} varies over the on-chip temperature range
- Off-chip laser source with temperature control, T_{VCSEL} is fixed



*Syrbu, OFC/NFOEC'08

BOSE Thermal Modeling

- For active switching, *M*-wavelength BOSE insertion loss to optical signal λ_n

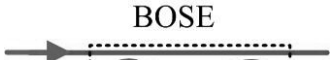
$$f_n = r_n - \frac{t_n^i t_n^o}{r_n - f_{n-1}^{-1} exp(j2\theta_{n-1})}$$

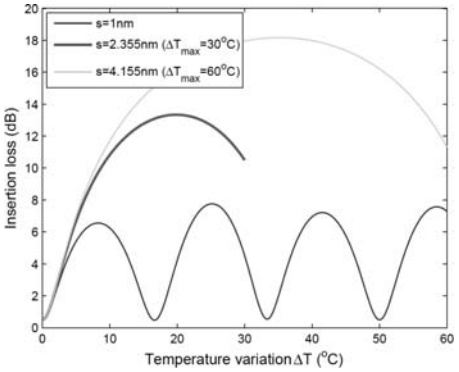
$$\omega_n = \frac{2\pi c}{\lambda_n + \rho_{MR} \cdot \Delta T}$$

$$r_n = \frac{2\kappa^2}{j2\tau(\omega - \omega_n) + (2\kappa^2 + \kappa_p^2)}$$

$$t_n^i = t_n^o = \frac{j2\tau(\omega - \omega_n) + \kappa_p^2}{j2\tau(\omega - \omega_n) + (2\kappa^2 + \kappa_p^2)}$$

$$L_{BOSE\_active} = -10log|f_{M-1}|^2$$





Insertion loss of an active 8-wavelength BOSE, Q=5000

BOME Thermal Modeling

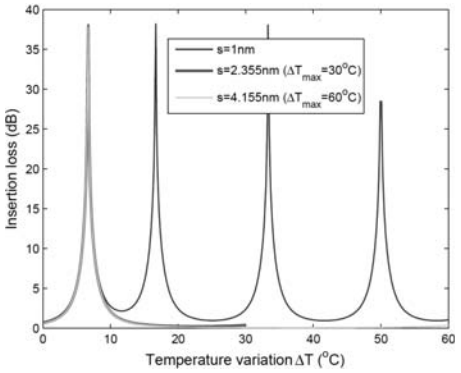
- BOME insertion loss to wavelength λ_0 under temperature variation ΔT

$$L_{BOME\_0} = \sum_{i=0}^{M-1} 10log \frac{(\frac{i \cdot s - b + \rho_{MR} \cdot \Delta T}{\delta})^2 + 1}{(\frac{i \cdot s - b + \rho_{MR} \cdot \Delta T}{\delta})^2 + (\frac{\kappa^2 - \kappa_p^2}{\kappa^2 + \kappa_p^2})^2}$$

- BOME insertion loss to wavelength λ_x under temperature variation ΔT

$$L_{BOME\_x} = \sum_{i=0}^{M-x-1} 10log \frac{(\frac{i \cdot s - b + \rho_{MR} \cdot \Delta T}{\delta})^2 + 1}{(\frac{i \cdot s - b + \rho_{MR} \cdot \Delta T}{\delta})^2 + (\frac{\kappa^2 - \kappa_p^2}{\kappa^2 + \kappa_p^2})^2} + \sum_{j=1}^{x} 10log \frac{(\frac{j \cdot s - \rho_{MR} \cdot \Delta T}{\delta})^2 + 1}{(\frac{j \cdot s - \rho_{MR} \cdot \Delta T}{\delta})^2 + (\frac{\kappa^2 - \kappa_p^2}{\kappa^2 + \kappa_p^2})^2}$$

- With a large channel spacing, loss can be controlled under 3dB, except for the temperature variation range between 4°C and 9°C



Insertion loss of an 8-wavelength BOME on λ_7, Q=5000

BOFE Thermal Modeling

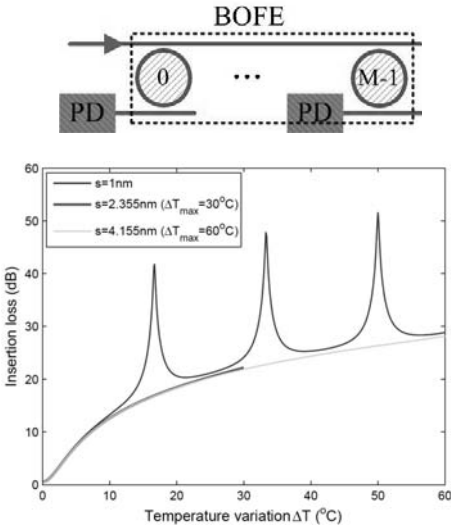
- BOFE insertion loss to wavelength λ_0 under temperature variation ΔT

$$L_{BOFE\_0} = 10log((\frac{2\kappa^2+\kappa_p^2}{2\kappa^2})^2 \cdot (\frac{(\rho_{MR}\Delta T)^2+\delta^2}{\delta^2}))$$

- BOFE insertion loss to wavelength λ_x under temperature variation ΔT

$$L_{BOFE\_x} = 10log((\frac{2\kappa^2+\kappa_p^2}{2\kappa^2})^2 \cdot (\frac{(\rho_{MR}\Delta T)^2+\delta^2}{\delta^2})) + \sum_{i=0}^{x-1} 10log\frac{((x-i)\cdot s+\rho_{MR}\Delta T)^2+\delta^2}{((x-i)\cdot s+\rho_{MR}\Delta T)^2+\delta^2 \cdot (\frac{\kappa_p^2}{2\kappa^2+\kappa_p^2})^2}$$

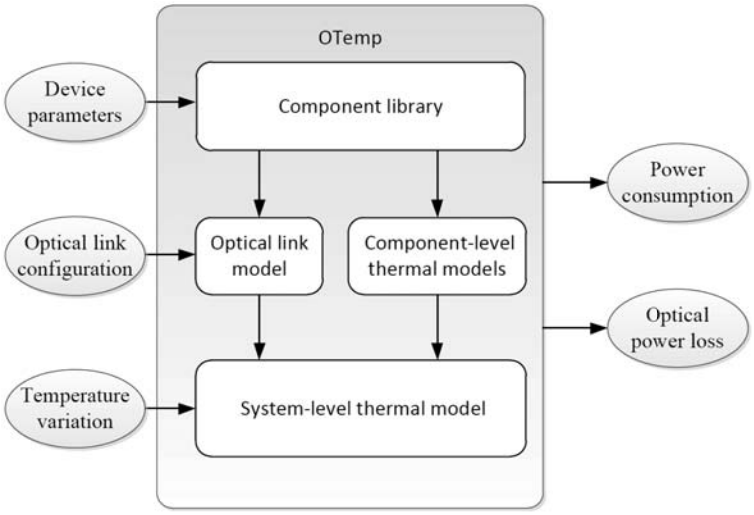
- A large channel spacing can reduce the insertion loss, but still as high as 20dB for ΔT=30°C



Insertion loss of an 8-wavelength BOFE to λ_7, Q=5000

OTemp

- Optical Thermal Effect Modeling Platform
  - For both inter- and intra-chip optical interconnects
  - For both single-wavelength and WDM-based optical interconnect networks
- Available at www.ece.ust.hk/~eexu/index_files/OTemp.htm



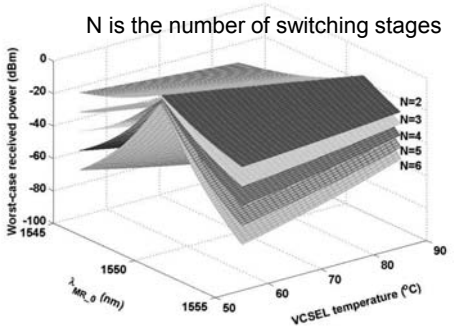
Key Findings

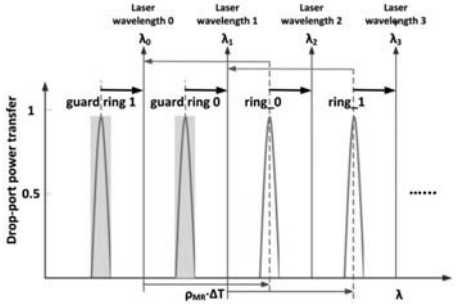
- Regardless of architectures, there are optimal initial device settings to minimize power consumption

$$\lambda_{MR\_i} = \lambda_{VCSEL\_i} + \frac{\rho_{VCSEL} - \rho_{MR}}{2} \cdot (T_{max} + T_{min} - 2T_0)$$

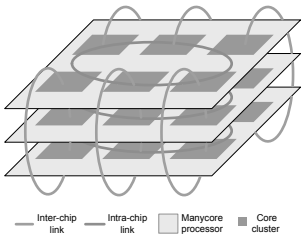
- The number of switching stages significantly affect power consumption
- Thermal tuning/adjustment with channel remapping and guard rings

N is the number of switching stages

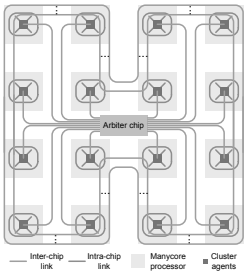




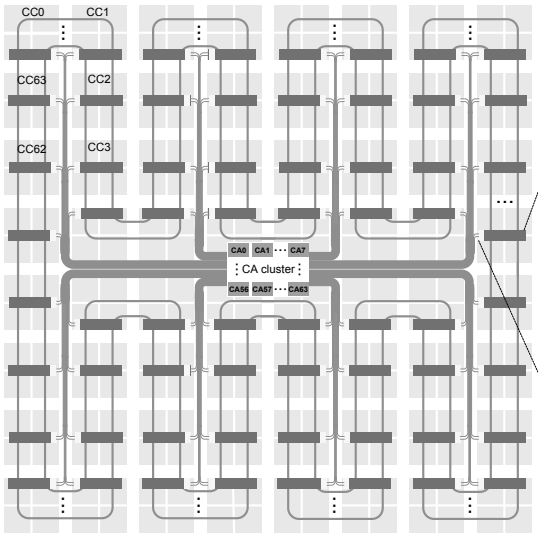
I²CON: Inter/Intra-Chip Optical Network

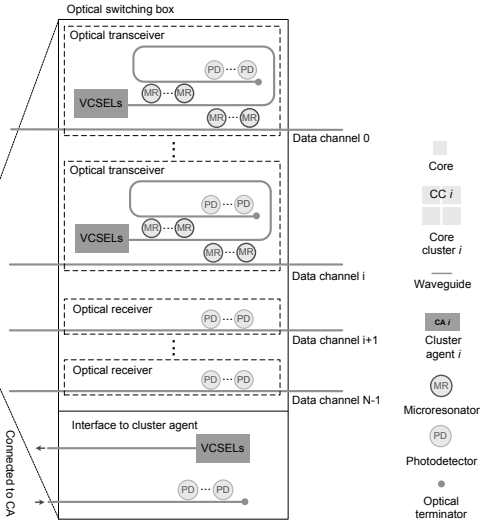


Logical view



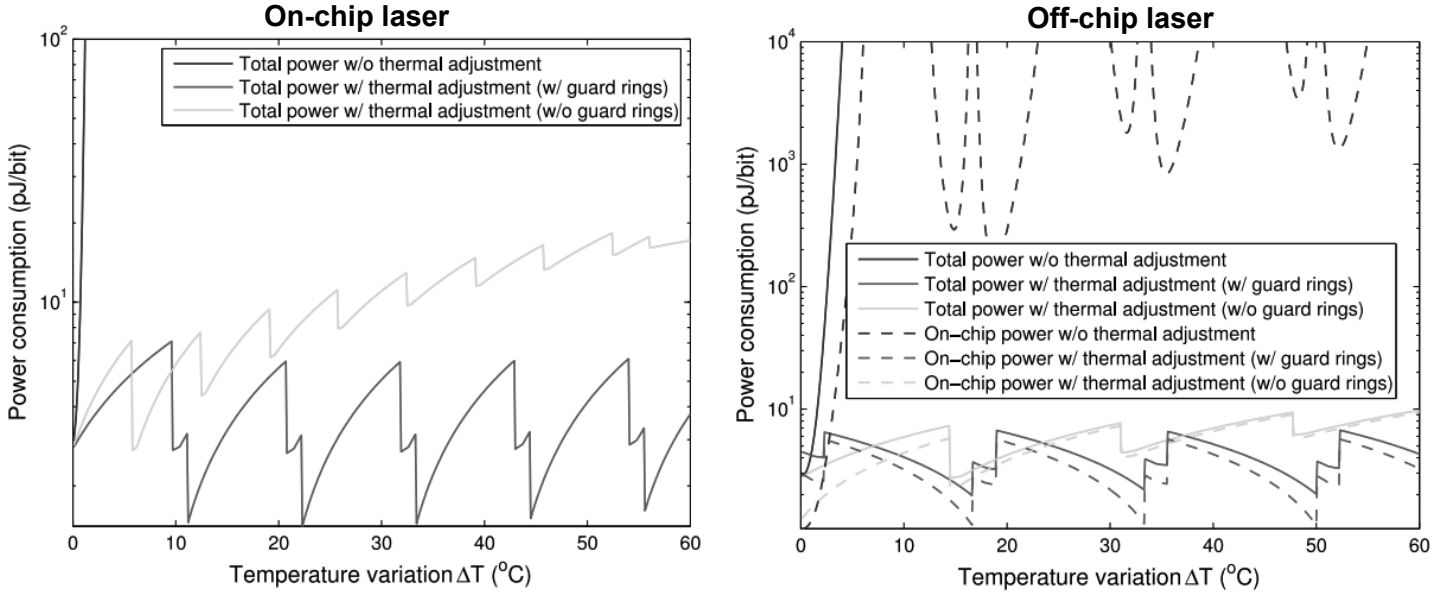
Multi-chip floorplan





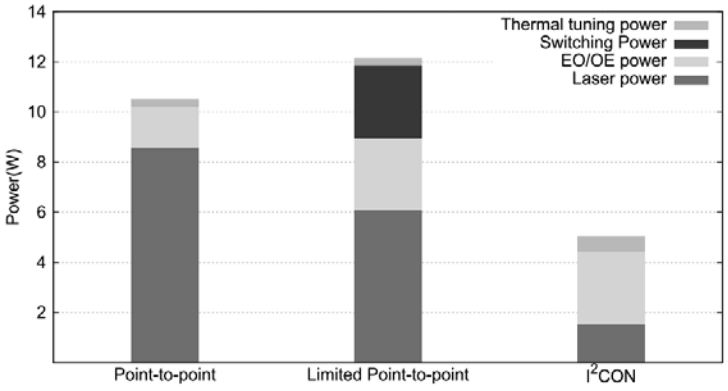
*Xiaowen Wu, Jiang Xu, *et al.*, "An Inter/Intra-chip Optical Network for Manycore Processors," TVLSI 2015

Worst-Case Power Consumption

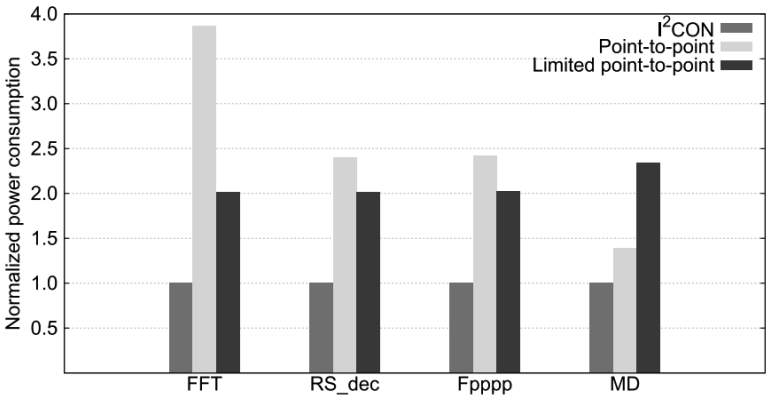


8 wavelengths, s=1nm, Q=5000

Average Power Consumption



Power breakdown of three designs under uniform traffic.



Power consumptions of three designs under real applications.

Summary

- Systematically modeled and analyzed thermal effects in optical interconnects
- Key findings
  - Optimal initial device settings to minimize power consumption
  - Switching stages have significantly negative impact on affect power consumption
  - Thermal tuning/adjustment with channel remapping and guard rings
- OTemp is released
- Case studies with worst and average case analysis

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Released Research and Development Tools

- COSMIC heterogeneous multiprocessor benchmark suite
- MCSL realistic network-on-chip traffic patterns
- PowerSoC power delivery system modeling and analysis platform
- CLAP optical crosstalk and loss analysis platform
- OTemp optical thermal effect modeling platform
- Inter/intra-chip optical network bibliography

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