

### **Motivation**





# The Communication Bottleneck of Parallel Computing



Collaborative Research Center 912: HAEC - Highly Adaptive Energy-Efficient Computing



Highly Adaptive Energy-Efficient Computing High-Rate Inter-Chip Communications



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GLOBALFOUNDRIES

amazon

#### **Optical Interconnect**

- adaptive analog/digital circuits for e/o transceiver
- embedded polymer waveguide
- packaging technologies
  (e.g. 3D stacking of Si/III-V hybrids)
- 90° coupling of laser

#### **Radio Interconnect**

- on-interposer/on-package
- antenna arrays
- analog/digital beam steering and interference minimization
- 100Gb/s
- 25 GHz channel @ 200GHz carrier
- 3D routing & flow management

## **Energy Optimization**



### Today's energy optimizations

- Are considered on a component level
- Mostly in isolation
- Unaware of applications and contexts

### Goal of project group B

- Address energy-efficiency at all system levels in an integrated holistic manner
- Ranging from the OS to software components to virtual machines

# HAEC B – Closed Energy-Control Loop

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#### **Energy-Optimization Control Loop**

- Measurement
- Analysis & verification
- Strategic regulation
- Adaptation

### **Energy-Adaptive Software Architecture**

- Global QoS optimization with "Energy-Utility Functions"
- Cross-layer adaptation: application - system - hardware





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## Example of Adaptivity by Software

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- Three in-memory database services
- All are using a scan to access their data
- → Under-utilized cores and interconnects

## Example of Adaptivity by Software



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#### How to optimize?

- 1) Exchange software implementations (dbscan  $\rightarrow$  index scan)
- 2) Migrate database service
- 3) Migrate memory
- 4) Turn off unnecessary interconnects

### Hardware and software adaptations

Necessary for optimal energy-efficiency/proportionality

## Example of Adaptivity



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# Highlights of Phase I (2011-2015)



**C**HAEC



# Selected HAEC A Highlights





# Selected HAEC A Highlights

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Vireless ntegration aging) Butler ADC Base-LNA Mixer DAC Matrix band EC Archit ellina Device A05 Bow-tie antenna (1mm x 0.6 mm) A01 200 GHz 18 mW A01 200 GHz A05 A01 24GSps 3bit LNA (low noise amplifier) 18 mW mixer Half cloversingle core leave antenna flash ADC (1.2mm x 0.7 mm)



## Selected HAEC B Highlights: HAECubie



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### The Outlook: The **HAEC Box** in 2030+



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Assume 64K processors per chip 160x chips stacked in 3D double-sided 4x4 chip-stacks on board 4x boards in a box





in 10x10x10 cm<sup>3</sup> (1 liter)

1.6K processor + 16K memory chips

- → 10<sup>8</sup> processors!
- → 10<sup>4</sup>x performance of today!

# HAEC Box Embedded Everywhere

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# High-Level Highlights / Conclusions



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- $\Box$  Adaptivity  $\rightarrow$  Energy proportionality
- □ Energy efficiency
- Revolutionary approach to computing hardware/software
- Impact onto more than computing applications
- Chance for scalability of the box and the software approach
- □ Chance for transfer

