MPSoC 2015, July 15th, 2015

Redefining SoC Design: Architecture Synthesis Platform for Multi-Core SoC

Sundari Mitra, CEO

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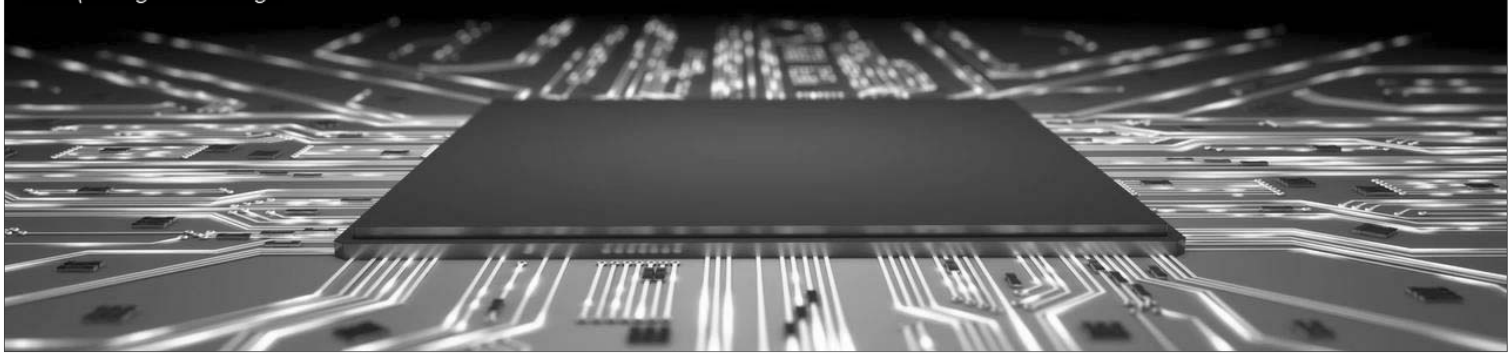

AGENDA

- MARKET TRENDS AND CHALLENGES
- SOLUTION
- KEY CHALLENGES AND INNOVATION

Discontinuities in the Compute Infrastructure

New Demand Profile Driving New Architectures

Compute

MAIN-FRAMES

Desktop

CLIENT/ SERVER

Internet

DATA CENTERS

Software Defined Everything

CLOUD COMPUTING

General Purpose → Workload specific

Hardware Acceleration for Software

Customized SKUs

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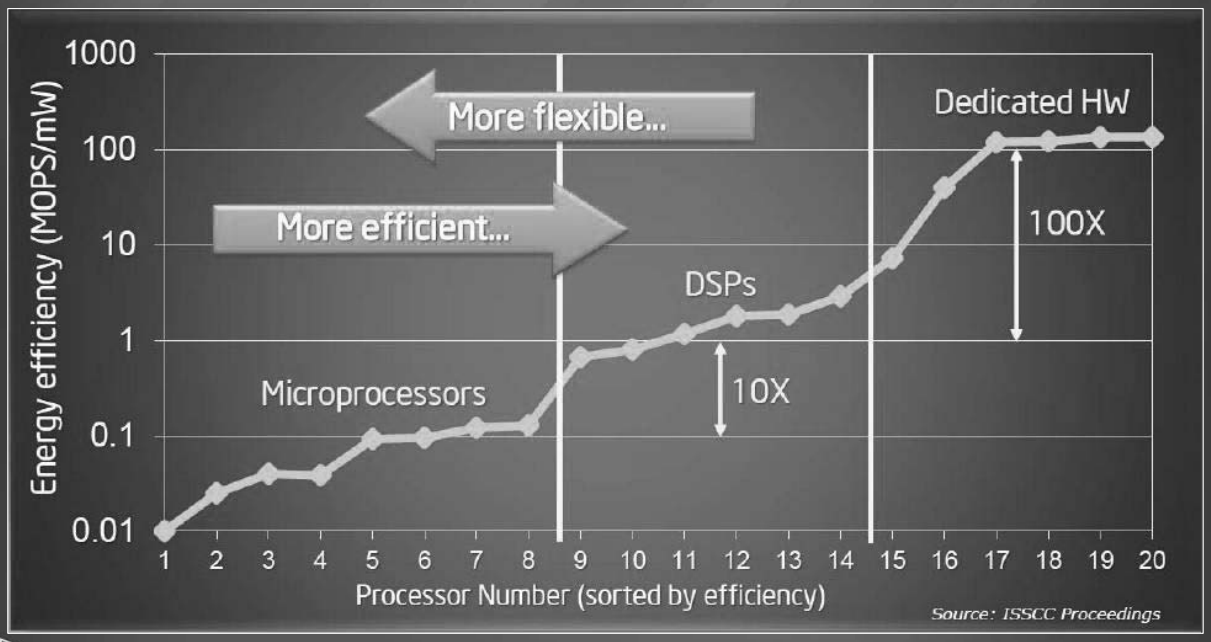
Cloud Architecture Driving Heterogeneous Computing

Increased Efficiency From Hardware Specialization



Source: ISSC Proceedings

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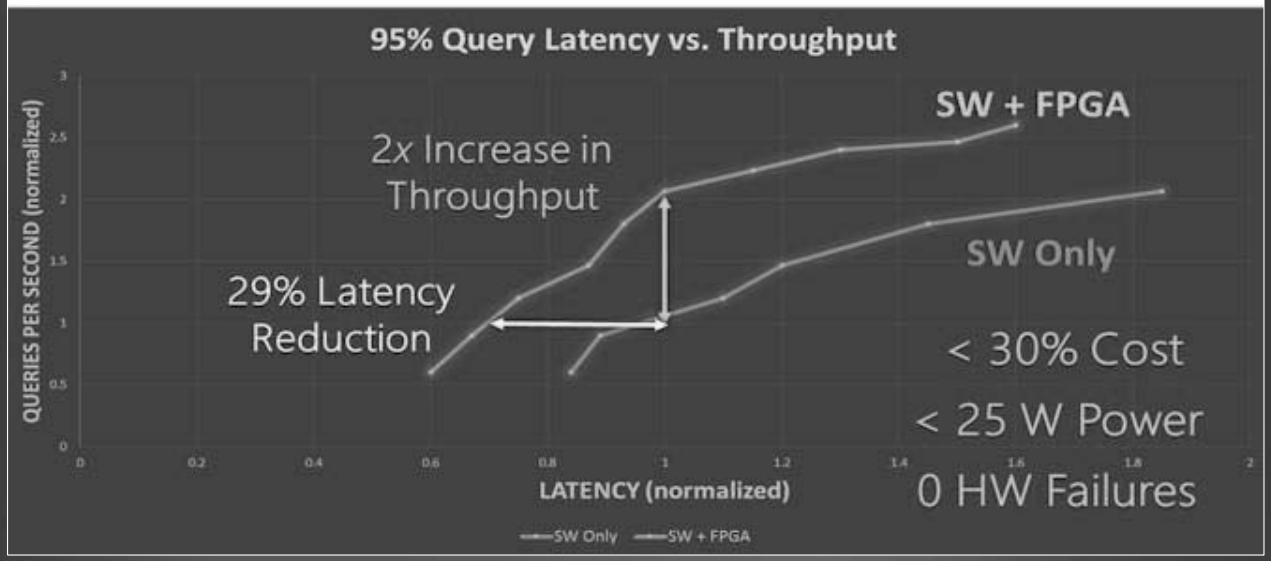
Cloud Architecture Driving Heterogeneous Computing

Reconfigurable Computing – ASIC + FPGA

1,632 Servers with FPGAs Running Bing Page Ranking Service (~30,000 lines of C++)



Source: Hot Chips 2014 Proceedings

Progressions in Chip Design

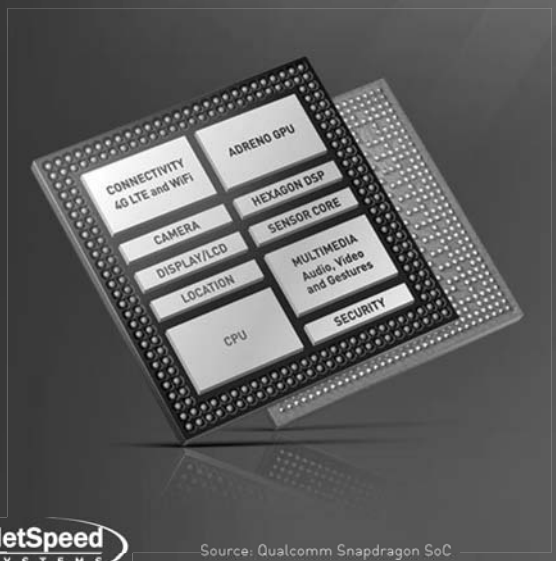
Changing Abstraction Levels

- Time-to-Market Pressure
- Performance Analysis from Day #1
- Create Differentiated Platforms

Time-to-market Pressure

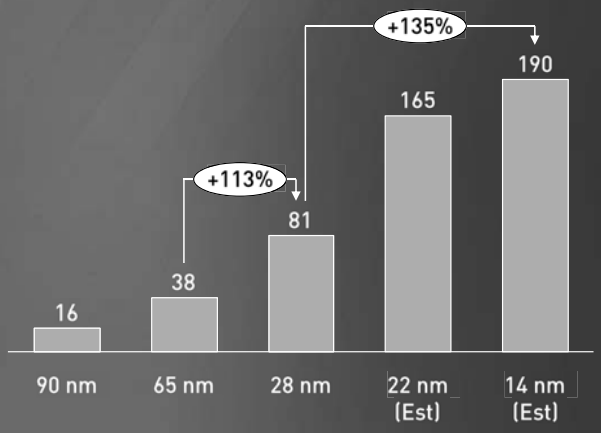
Decreasing TTM even with exploding complexity

Sophisticated Functionality Increasing Design Complexity



Source: Qualcomm Snapdragon SoC

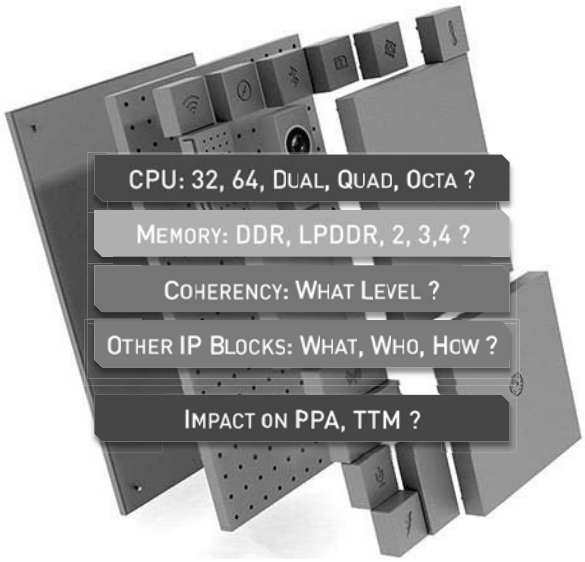
Ever Increasing Number of IP Blocks in an SoC

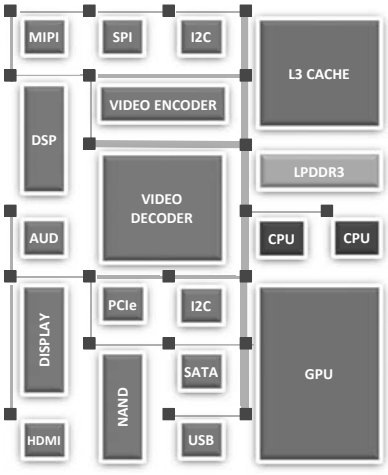


Source: IBS report, 2012

Creating Differentiated Platforms

Core Architecture and Derivative Products



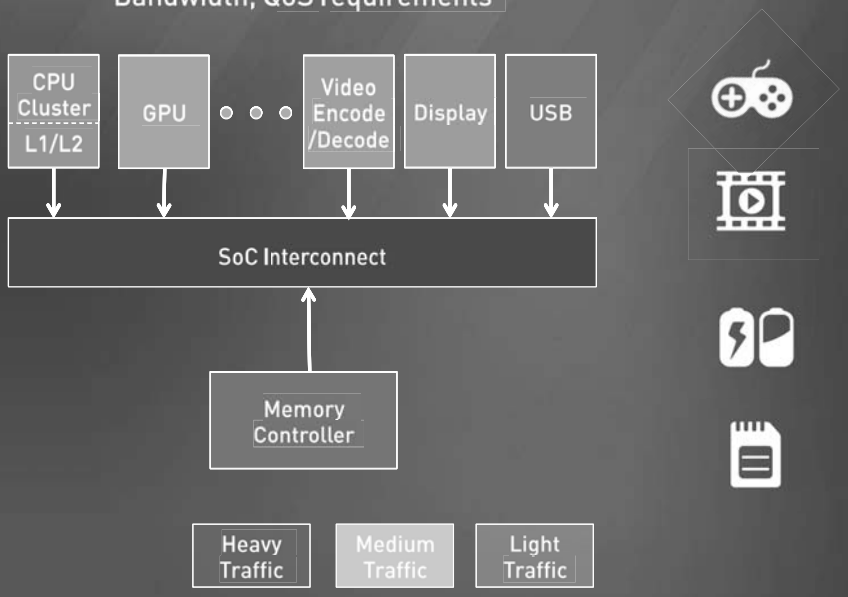


Source: Google Project ARA

Performance Analysis

Multiple Agents Contending for Memory

Multiple traffic profiles with sophisticated Bandwidth, QoS requirements



Heavy Traffic | Medium Traffic | Light Traffic

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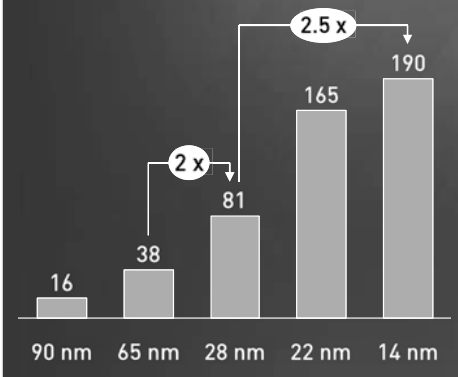
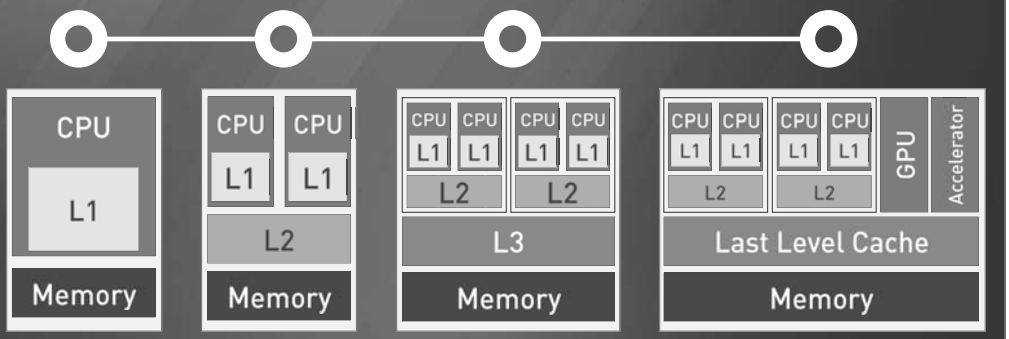
Evolution of Coherent Interconnect Solutions

Coherency Participation Has Increased



Source: IBS report



- Number of IP blocks have exploded and more agents are participating in coherency
- Requirements moving from homogeneous → heterogeneous

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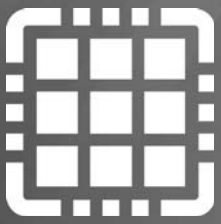
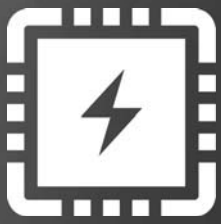
The Need for Flexible Interconnect Solutions

Flexibility Creates Opportunities





CUSTOMIZE FOR APPLICATION

- Improve latency of critical traffic
- Improve compute cluster latency

CUSTOMIZE FOR FLOORPLAN

- Reduce interconnect congestion
- Utilize unused die area

CUSTOMIZE FOR POWER

- Enhance energy efficiency
- Lower interconnect BW req

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NetSpeed Solution

SoC Architecture Synthesis Platform

SoC Interconnect IP

SoC Cache Coherency IP

Next-Gen Platform to help Build Faster, Efficient SoCs

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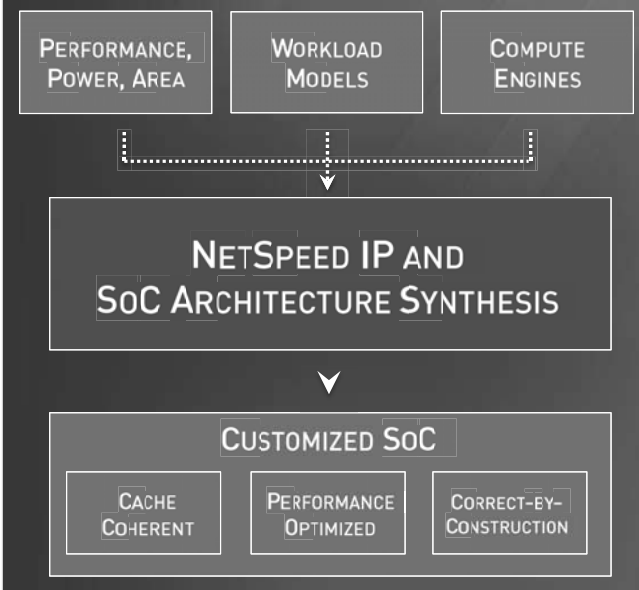
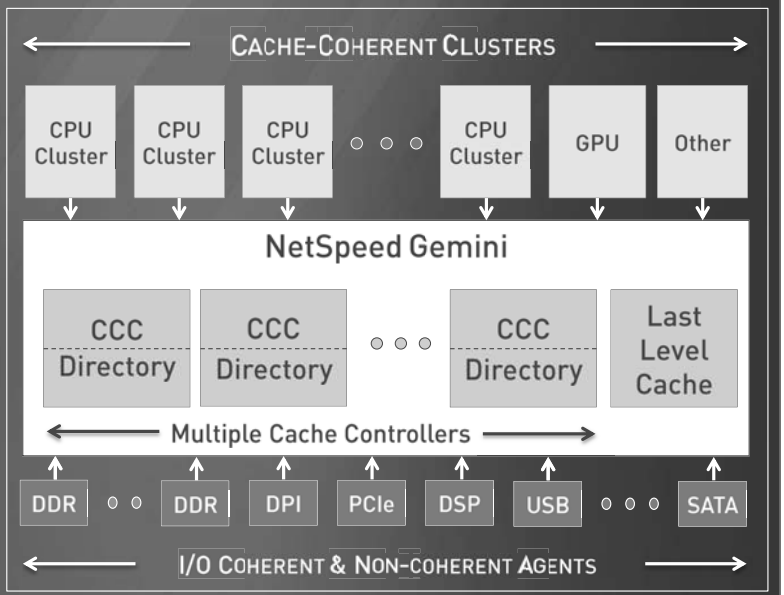
NetSpeed Technology Overview

Built From Requirements, Optimized For Specific Application





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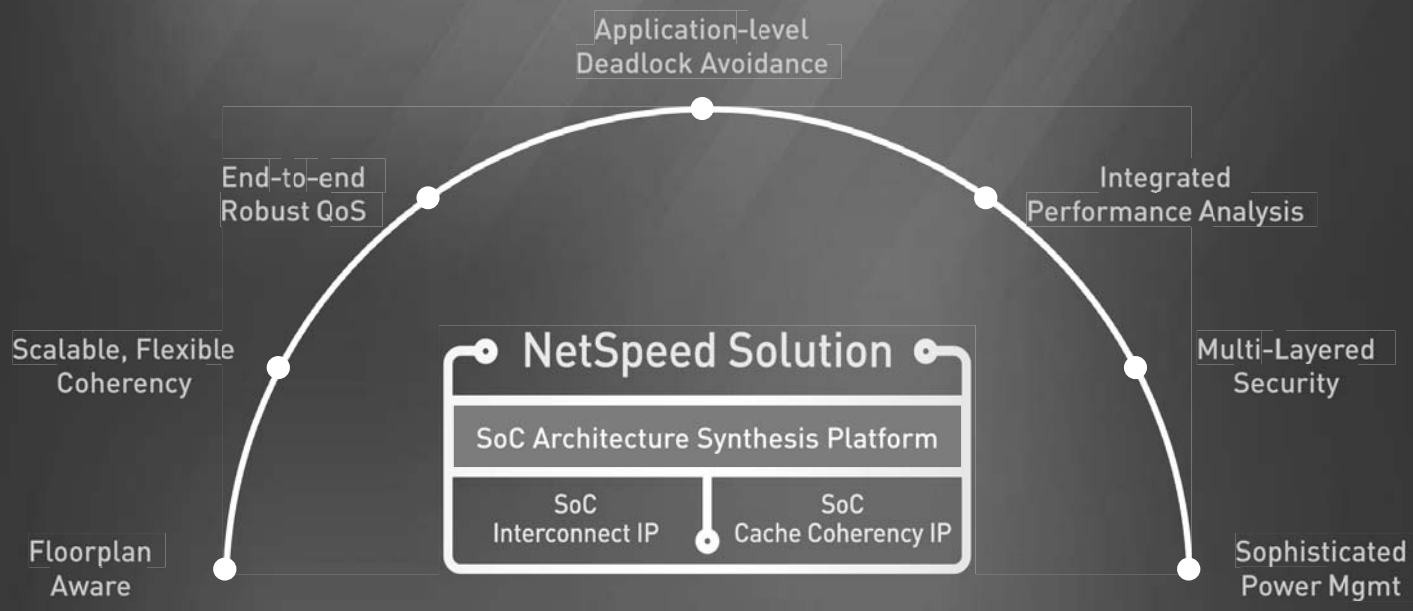
NetSpeed Architecture Synthesis Platform

Essential Toolkit for SoC Architecture



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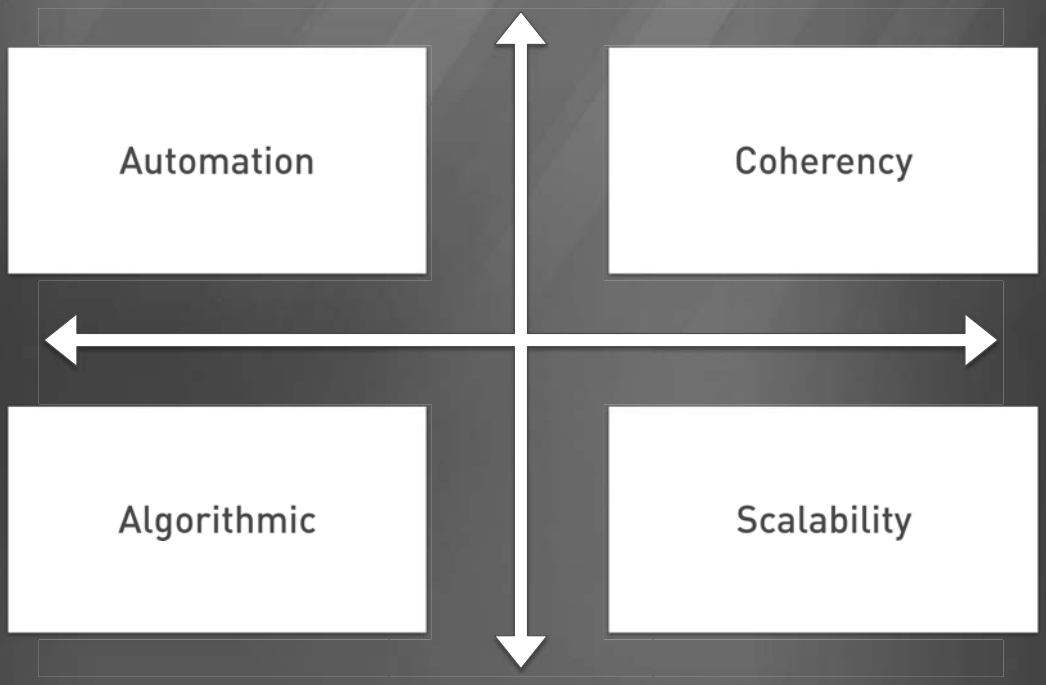

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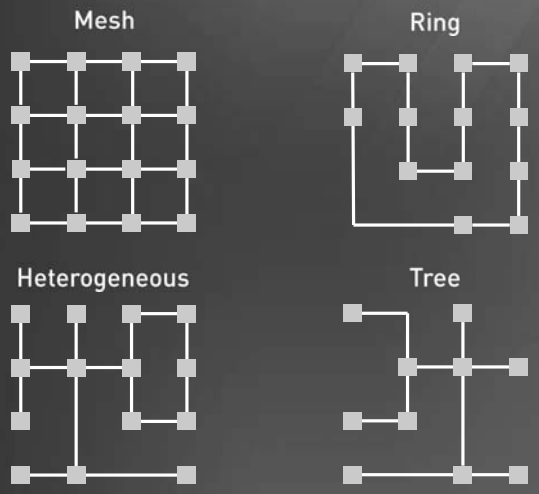
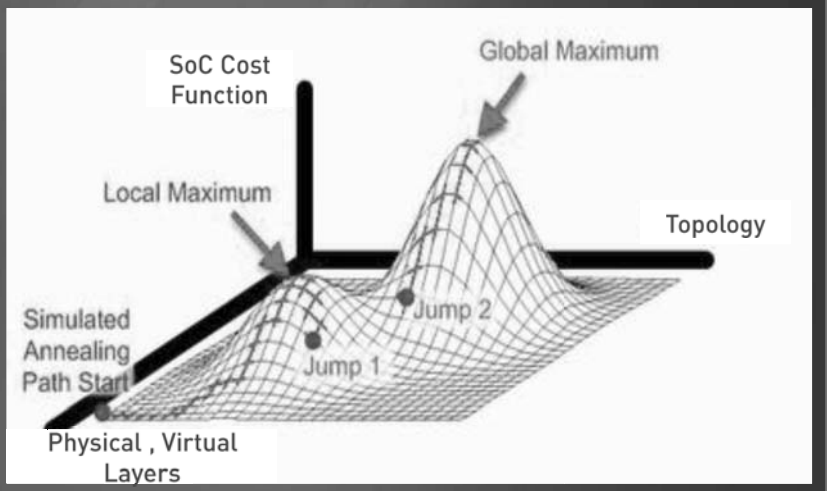
AUTOMATION

Traffic Based Rapid Reconfiguration

Bringing the Power of Synthesis to SoC Architecture

- Machine learning algorithms to determine optimal topology
- Fully heterogeneous in determining channel & buffer sizes





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NetSpeed Router

NetSpeed Auto-generated Links

Physically Aware Design Flow

Designed To Be Timing Clean

Step 1: Specify

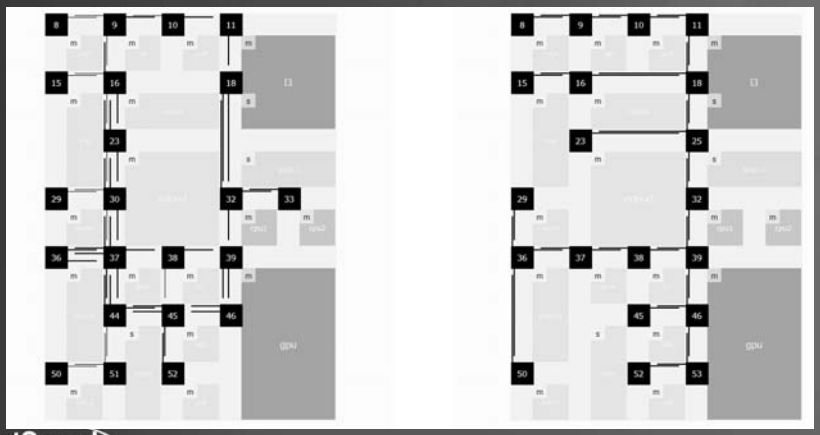
- Components, Connectivity
- PPA, Coherency Requirements
- SoC Level Use Cases

Step 2: Customize

- Rapid Architecture Exploration
- Real-time Customization
- Power Estimation & Optimization

Step 3: Generate

- Customized SoC Interconnect IP



Synthesizable RTL

Verification IP

C++ Functional Models

Physical Design Views

IPXACT, Custom Programmers Guide

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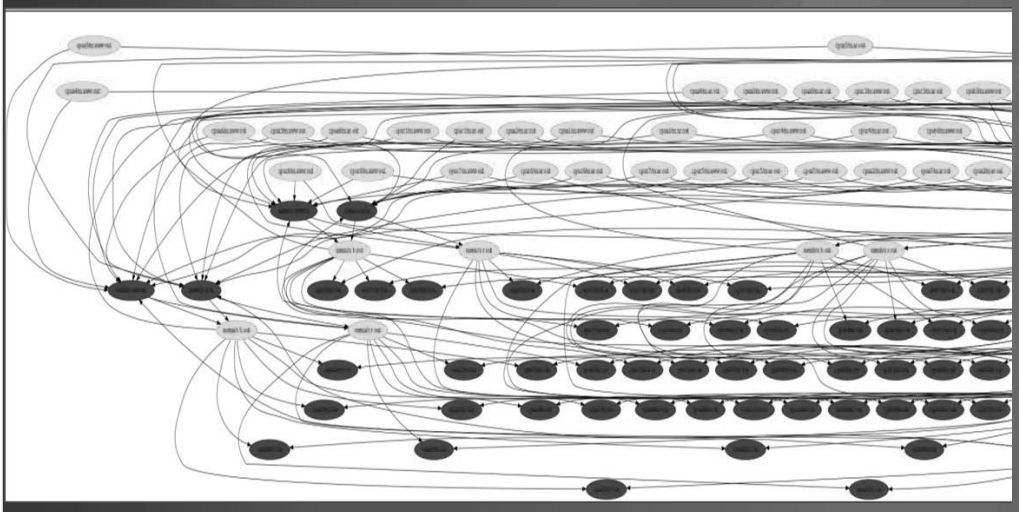
ALGORITHMIC

Deadlock-Free Solution

Formal Analysis to Build Correct-by-construction IP



- ✓ FORMALLY PROVEN
  - Formal techniques and graph theory algorithms
- ✓ CORRECT-BY-CONSTRUCTION
  - User-driven traffic dependencies
- ✓ ROBUST
  - Handles complex topologies and routing

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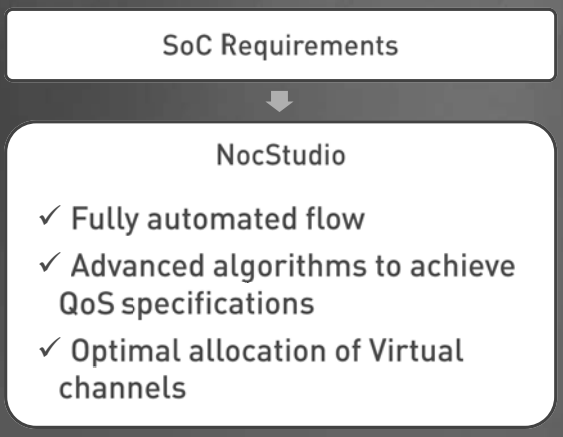
End-to-End Robust QoS

- QoS implementation part of design flow
- Strict priority & weighted bandwidth allocation schemes

NetSpeed Flow



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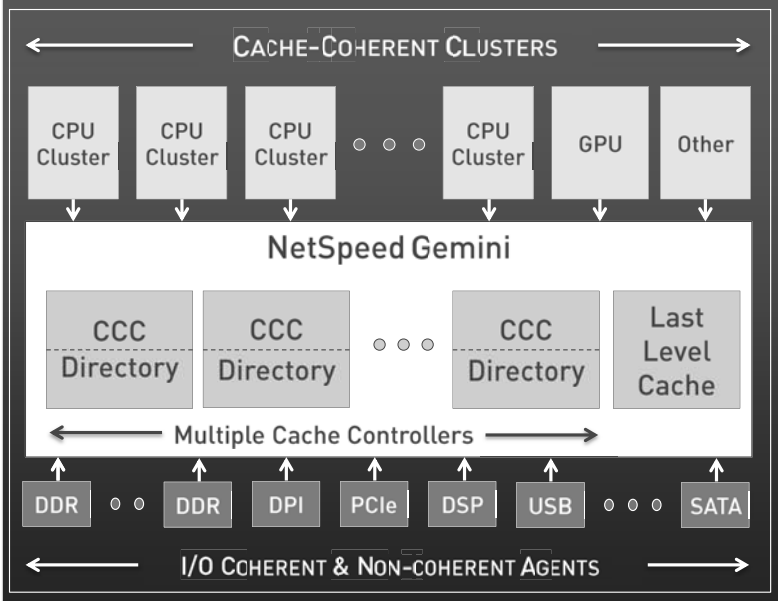
COHERENCY

NetSpeed Gemini Overview

Key Benefits



HIGHLY CONFIGURABLE

- Customized for floorplan
- Physically distributed coherency solution

LATENCY OPTIMIZED

- Latency optimized network with FastPath™
- Configurable cache hierarchies with LLC

BUILT-IN CORRECTNESS

- Application-level deadlock avoidance
- Integrated performance analysis toolkit

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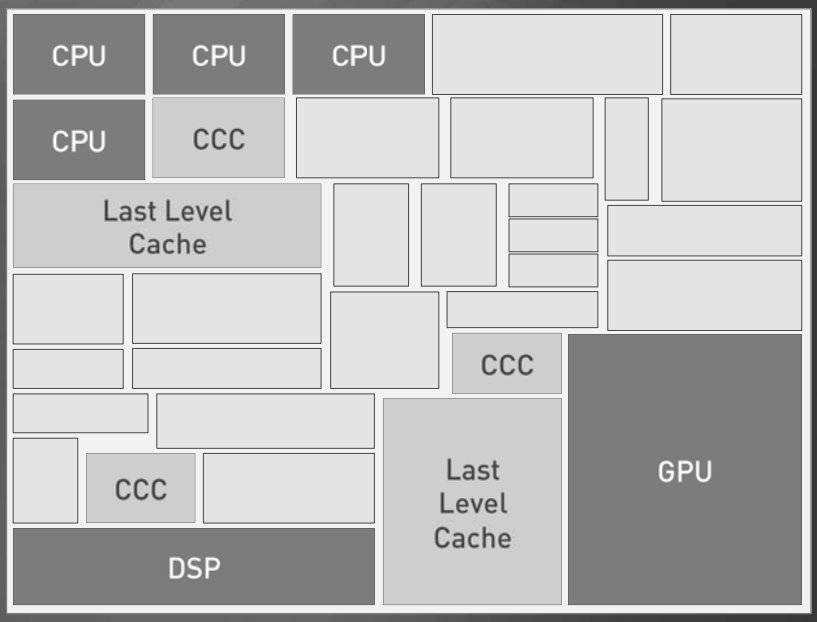
Physically Distributed Coherency

- Lower latency by placing coherency controllers and caches where they are accessed the most
- Reduce congestion by handling requests locally and using caches to reduce traffic to memory
- Adjust cache hierarchy to support floorplan requirements
- Improve die utilization by placing caches in empty die space



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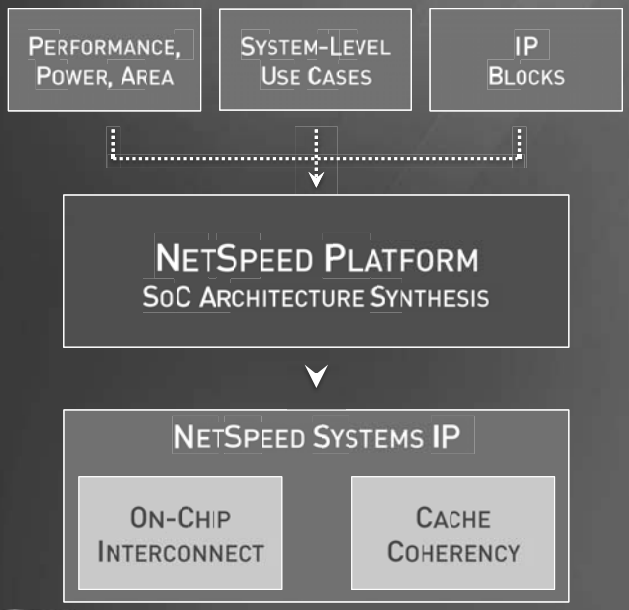
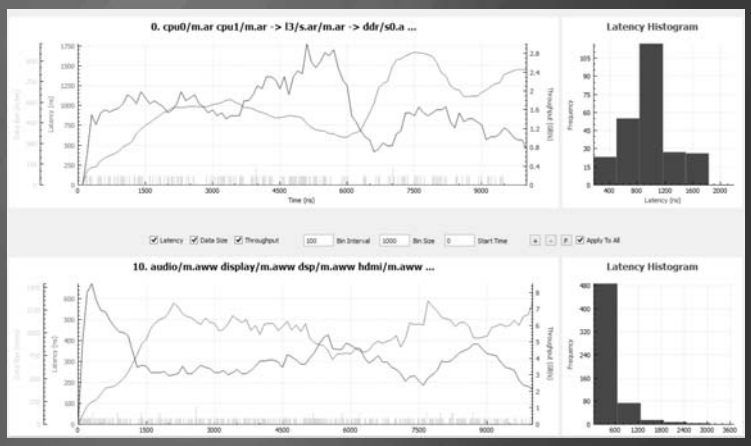
Integrated Performance Simulation





Listing power consumption levels in various power profiles

Power profile	Weight	Total links	Powered down links	Total routers	Powered down routers	Total bridges	Powered down bridges	% Power consumption
all	0	196	0	44	0	46	0	100
audio_only	1	196	105	44	25	46	18	31.62
compute	1	196	45	44	8	46	11	75.43
diplay_idle	1	196	88	44	16	46	18	52.46
gaming	1	196	81	44	18	46	13	46.88
video_playback	1	196	90	44	20	46	16	47.89

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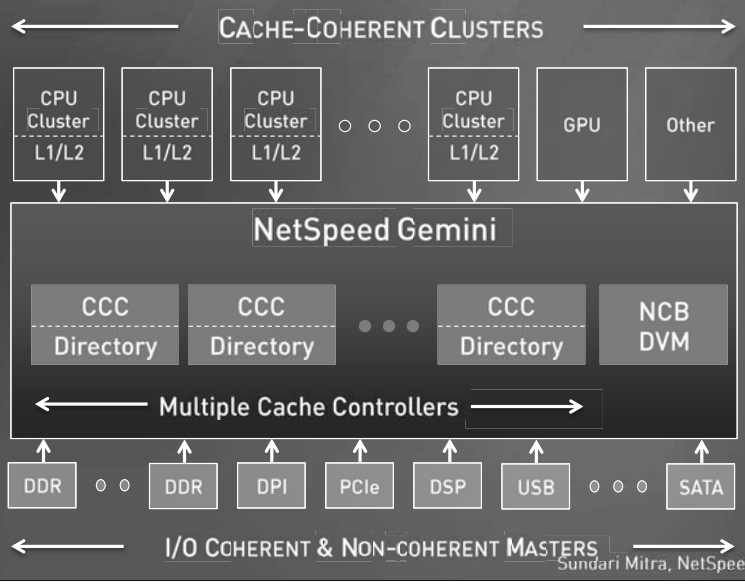
Scalability

Scalable Coherency Bandwidth

- More coherent lookups per cycle
  - Increased coherency bandwidth through address-sliced coherency controllers
  - Automated determination of coherency controllers



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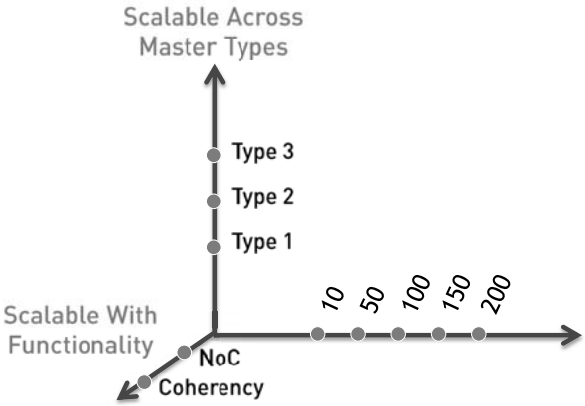
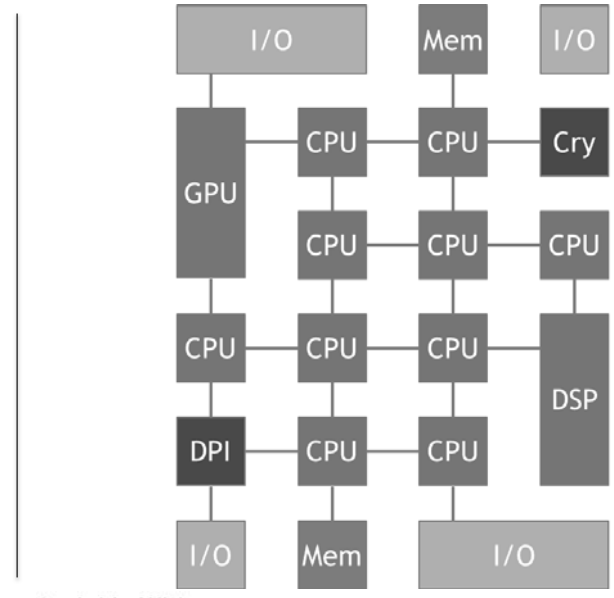
Scalable Across Many Dimensions

- Scalable NoC allows for heterogeneity in Master types, shapes and sizes
- Single NoC platform that scales up and down in size
- Scales with number of Coherent Masters in the SoC





Redefining SoC Design

Summary

PROBLEM	▪ Exploding complexity with shrinking timelines ▪ Need for application-specific, SoC-specific flexible solutions ▪ Current coherency solutions are static, isolated
SOLUTION	▪ NetSpeed Architecture Synthesis Platform ▪ NetSpeed Orion: Non-coherent NoC IP ▪ NetSpeed Gemini: Coherent NoC IP
BENEFITS	▪ Flexible, correct-by-construction IP ▪ Higher performance with lower latency ▪ Build customized application-specific solution

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