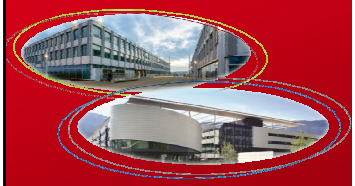

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Virtual prototyping acceleration on manycore architectures

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Introduction

- SoCs are becoming more and more complex
  - Complexity in a chip is increasing x1.6 every 2 years (ITRS 2013)
    - e.g. Apple A8 SoC owns 2B transistors
  - Development costs/TTM must be contained
- Virtual prototyping can
  - Improve design quality and performances with fast design exploration
    - Performance, power, temperature, reliability
  - Provide a virtual HW platform to SW developpers
    - Parallelize design phases and increase design productivity
- Limitation of VP
  - Simulation performance does not scale with complexity *(at constant accuracy)*

➡ Inevitable need for VP acceleration

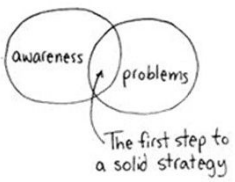
SystemC is mainly used as VP kernel

- SystemC
  - Accellera standard C++ library (IEEE Std. 1666™-2005)
  - A discrete event simulator (DES)
  - Current version is 2.3 + TLM 2.0.1

- SystemC is widely used for
  - Design-space exploration
  - Verification/validations

What about parallelizing SystemC?

- The evaluation of processes is potentially highly parallel
- But it is a very hard problem *(no industrial solution exists)*
  - A parallel implementation must keep the exact same behavior than the sequential one
    - It should not introduce new race conditions
    - Sequential phases modelling concurrency must be respected
  - Process lengths are usually shorts
    - Performances are very impacted by the kernel and synchronizations
  - Mainly irregular and control-oriented processing
    - Lots of function calls, branches and conditional executions
    - Only few simulations have data-parallelism



Related works

- Static scheduling (conservative)
  - Use of a global synchronization (at each δ-cycle)
  - Reduces synchronization and context switching overheads
  - Support shared variables between processes
    - Ensure that two processes accessing the same variable will never be run in parallel
  - Approaches
    - Local dependency analysis [BUCH07, MOU04, NAG07]
      - Suppose that a process only access to variables declared within its own module
    - Global static analysis [CHEN12, BLAN10]
      - Detect access to shared variables between Wait statements
      - Almost not practical with high level modeling (C++ or TLM)
    - TLM is not supported (e.g. RAM are shared array between components)
- HW acceleration (conservative)
  - Not fully compliant with SystemC (or limited use)
  - With the CELL processor [KAOU09]
  - With GP-GPU
    - Accelerate some processes on GPU [SINH12, VINC12, NANJ10]
    - Distribute multiple simulations [KUNZ12]
  - With a dedicated many-core [VENT14]

Related works

- Distributed SystemC (conservative and optimistic)
  - Use implicit communications (FIFO), synchronization or lock mechanisms or avoid shared variables
  - Works if few communications between clusters
    - Need to clusterize the simulated architecture
    - Modification of the simulated architecture to explicit the parallelism
  - Approaches:
    - Multiple SystemC schedulers
      - Conservative approaches [ZIYU09, CHOP06, CHUN14]
      - With speculation or relaxing methods [MEL10, COMB08, PESS10]
        - *Synchronizations on every communication, null messages...*
    - Distributed simulation on top of SystemC [HUAN08]
- Parallel SystemC kernel (conservative)
  - Use of a global synchronization (at each δ-cycle)
  - Execute the evaluation phase in parallel
  - Load-balancing techniques (work-stealing, work-sharing...)
  - Approaches
    - Not SystemC compliant [EZUD09, SCHU10, KHAL10]
      - Shared variable access atomicity is left to the user
      - Process order is not guaranteed
    - SystemC compliant
      - Run processes in parallel though they do not run at the same time [MOY14, CHEN12]
      - Partition simulation and preserve co-routine semantics within a partition [SCHU13]

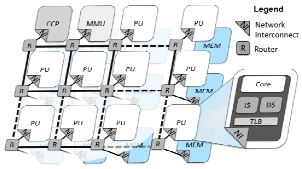
SCale

- Development of a new SystemC kernel, named SCale
  - Compliant with Accellera standards
    - TLM, TLM2.0, SystemC 2.3.1
  - Lightweight and think-parallel kernel
  - Conservative, in-order, global synchronization
  - Supports multiple architecture
    - Tilera64, AMD Bulldozer, i7 (for now)

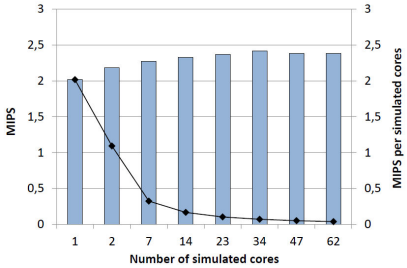
SCALE
Parallel SystemC Kernel

Results

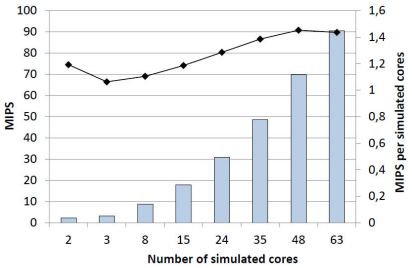
- Experiments with SESAM [VENT13] and SimSoC [HELM08] modeling a 64-core manycore architecture on a 64-core AMD Opteron machine
- Performances
  - 675 MIPS and 21x (SimSoC and BT)
  - 90MIPS and 36x (SESAM)



With Accelera (SESAM)



With SCale (SESAM)



Conclusion

- Designing large and complex systems need new methods and tools to accelerate simulations
- CEA LIST proposes a new SystemC kernel named *SCale* able to leverage the multiple cores of a many-core architecture
  - Guarantee accuracy and maintain sequential behavior and reproductivity
  - Up to 36x on a 48-core host x86

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Thank you for your attention

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