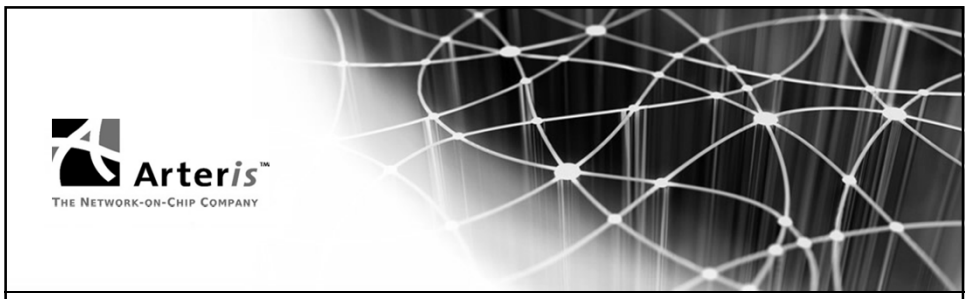


Using SoC Interconnect IPs to Improve Physical Layout

Adding Physical Awareness to Network on Chip Interconnect

K. Charles Janac
President and CEO, Arteris

 15 June 2015

FlexNoC® Network-on-Chip Interconnect

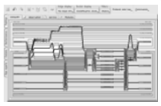
EDA Interfaces
Synopsys, Cadence
Mentor

FlexNoC Tools
Specification, models, exploration, physical awareness, synthesis, verification and more

EDA Tool Outputs
Models, test benches, synthesis scripts etc.

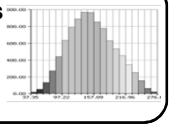
IP Protocol NIUs
ARM, Synopsys,Tensilica, Internal

FlexNoC Library
NIUs & transport:
Switches, buffers, domain crossings etc. + 100s other features



RTL Outputs
Synthesizable RTL

SoC Syst. Features
SoC Analytics, monitoring
Quality of Service, Security, Power management
Options: Resilience
Physical Awareness



Data/Analytics Outputs
Debuggers, Linters
Middleware

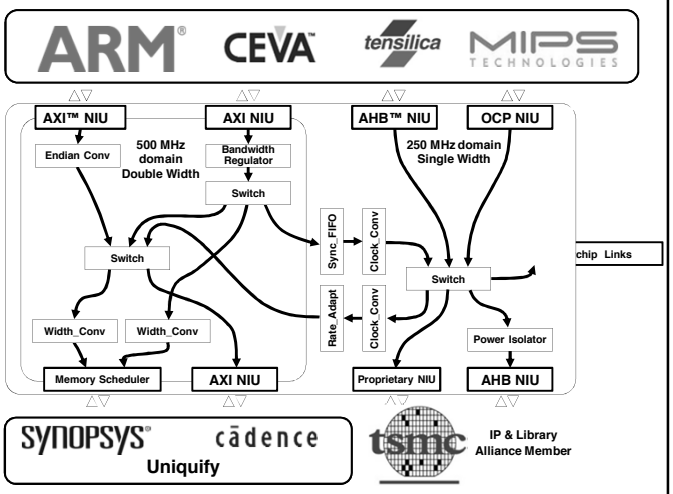
Unlimited Configurability → Unconstrained Differentiation

 2

Arteris FlexNoC® Interconnect IP Library

Automated, Scalable, Flexible Hardware Architecture

- Packetization Transactions
- NoC Transport
- SoC Services
- Interchip Links



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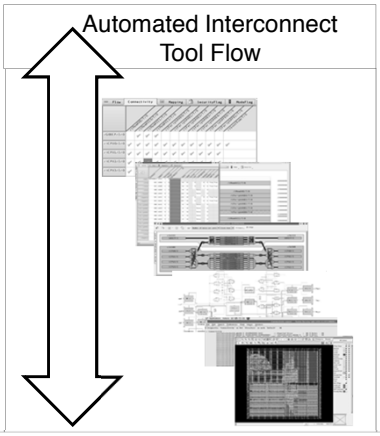
FlexNoC Interconnect Tools Enhance SoC Delivery



- Explore and Optimize Architectures
- Iterate Interconnect Faster and Easier
- Connect to Range of IPs and EDA tools

- **Specification**
  - Clocks & Resets & Domains
  - Sockets
  - Memory Map
- **Architecture**
  - Topology Exploration
  - Topology Development
  - Topology Optimization
- **RTL Design**
  - NoC Structural Synthesis
- **Verification**
  - Automated verification
  - 100% coverage
  - SystemVerilog
  - Verilog, System C, VHDL
  - Scripts, Benches, Constraints
  - Documentation & XML

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Physical Interconnect IP Challenges <28nm

Interconnect is more & more difficult to implement
@ 28nm & below

- Architects need to **visualize physical impact** of their SoC topologies
- RTL engineers can spend months **adding pipelines manually**
  - Start again with major interconnect changes such as derivatives
  - Overdesign area & timing slack, raising SoC cost & power
- Layout engineers given interconnect IP **RTL not physically verified**
  - Have little idea what the architect intended from physical perspective
  - Have to overcome routing congestion and timing closure problems
  - Timing is not closed at the RTL level, creating multiple P&R loops

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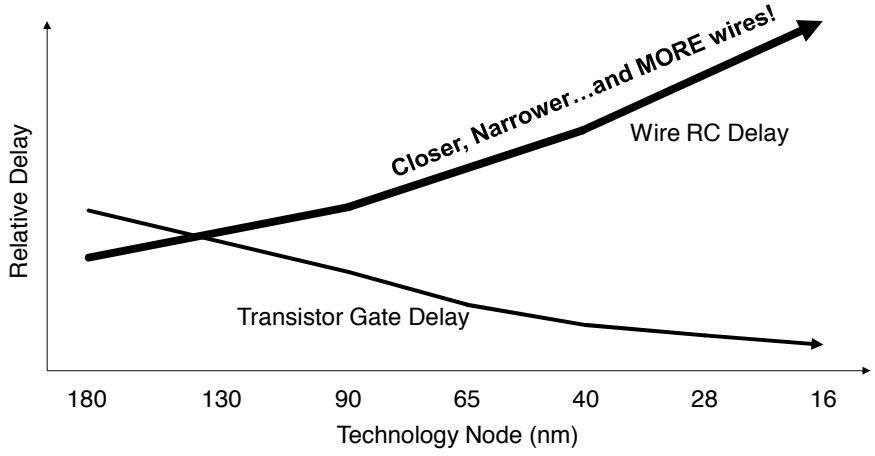
Wire RC vs. Gate Delay: Why is the Interconnect so impacted?



Sources: Synopsys, Intel

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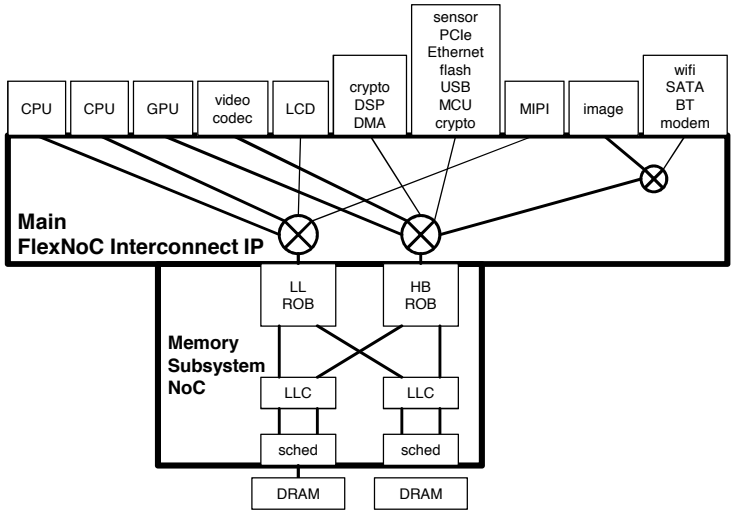
Network-on-Chip Interconnect IP View



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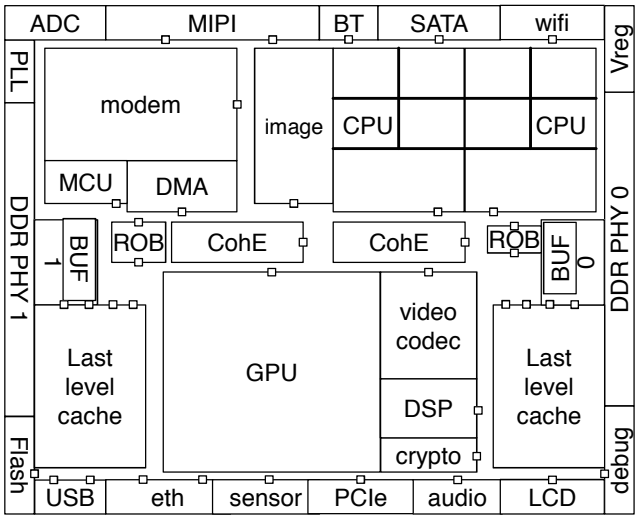
SoC IP Floor Plan View



□ high bandwidth socket interface □ relatively low bandwidth socket interface

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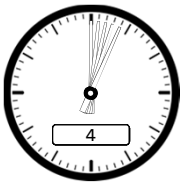
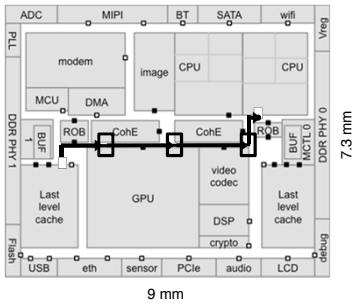
Can't cross 28nm SoC in one clock cycle

Physical distance dictates the number of pipeline stages





- NoC at clock of 600MHz = 1.67 ns cycle time, usable 1.42 ns
- Transport delay of 0.644 ns/millimeter (best in 28nm/TSMC 28HPM)
- Pipeline-to-pipeline maximum distance is 2.2 millimeter

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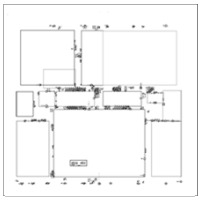
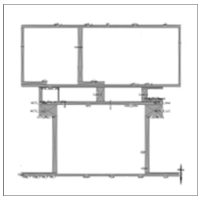
FlexNoC Physical™

Visualize



Isolate & Optimize



Automate Timing Closure

Accelerating Layout with **Physically Aware** Interconnect IP

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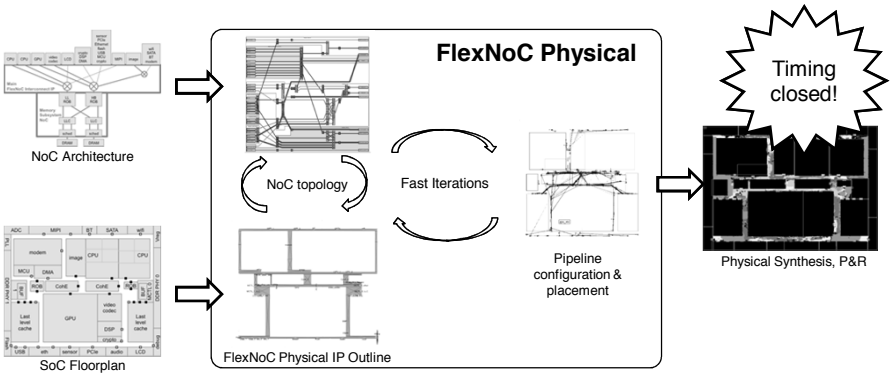
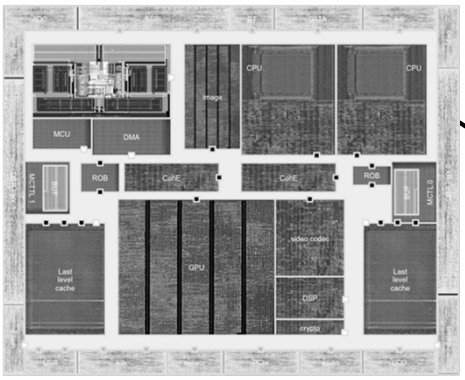
FlexNoC Physical™:
Physical Awareness & Automated Timing Closure



Isolate the NoC physical instance to optimize timing & routing



FlexNoC Physical screenshot

Optimize NoC physical instance independently of rest of the SoC

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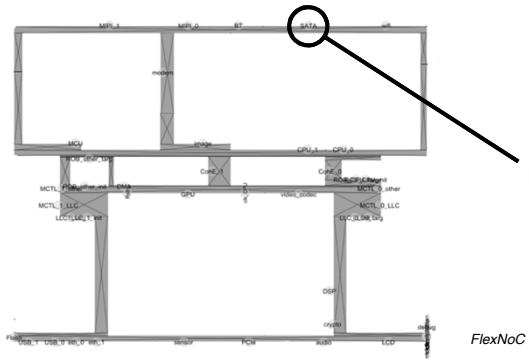
Isolate the NoC physical instance to optimize timing & routing



FlexNoC Physical screenshot

Optimize NoC physical instance independently of rest of the SoC

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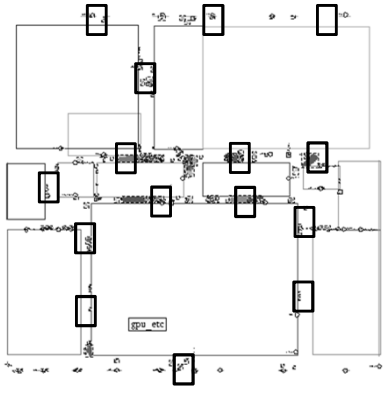
Adding Pipelines Automatically

- Evaluate all timing arcs in the NoC interconnect
- Distance and logic depth dictate number of pipeline stages
- Placement of the NoC units is predicted by FlexNoC

= New pipelines inserted by FlexNoC Physical to close timing



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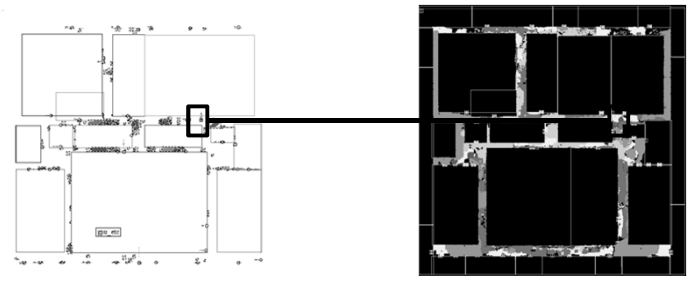
First pass timing closure example

	FlexNoC estimates		DC zero wire load		DC Topo Results	
	area	timing	area	timing	area	timing
Without pipelines	556795	VIOL	385111	met	830672	VIOL 1.26ns
After auto pipe	780631	**met**	534947	**met**	806232	**met**
With all pipelines on	940468	**met**	720882	**met**	1008348	**met**



Predicted Pipeline location

Implemented Pipeline location

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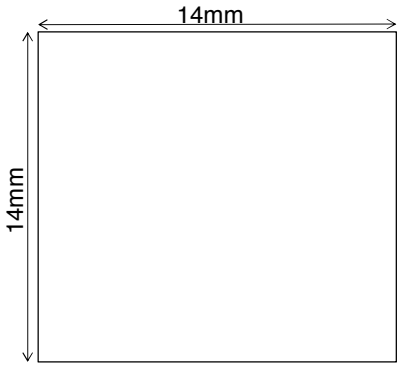
Real World Customer Example:
Automatic pipeline insertion decreases SoC area



- **Interconnect IP Area: -11%**
  - **Auto Pipe: 1,582,604 sq um**
  - Manual Design: 1,770,786 sq um
- **Closing Timing Productivity: +30x**
  - **Auto Pipeline Insertion: 1.5 days**
  - Manual Pipeline Insertion: 45.0 days
- Design Parameters
  - TSMC 28nm HPM process
  - Real customer design
    - FlexNoC used at top level
  - 20 power domains
  - 10 clock domains
  - 100MHz … 400MHz
  - 160 NoC Sockets

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FlexNoC Physical Benefits

1. **Save 1-3 months of iterations** with automatic pipeline insertion
2. **Save 5-15% of interconnect area** vs. having to overdesign with excessive number of pipelines
3. **Improve performance** by matching timing goals to implementation of each NoC IP version vs. overdesign
4. **Provide a better starting point** for layout process to cut place & route cycles and improve layout productivity

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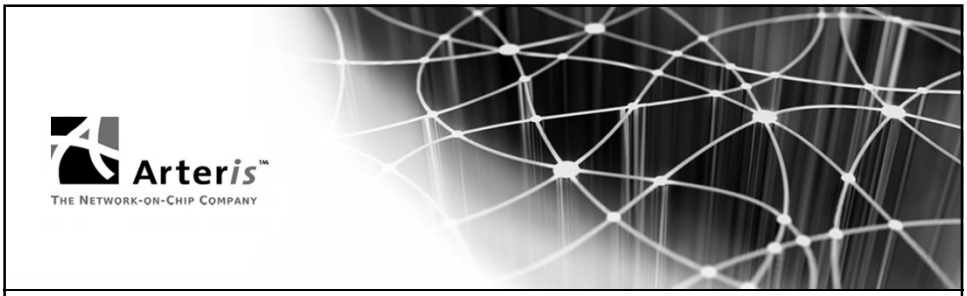

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Thank YOU

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