

FROM RESEARCH TO INDUSTRY
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SoC energy management via feedback control for data parallel applications with throughput constraints

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- Multi/many-core architecture and programming model
- Energy management via control theory
- Experimental results
- Conclusions

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Many-core systems (embedded)

Number of clock domains and voltage domains per SoC

Year	<=5	6-10	11-20	21+
2007	~55%	~35%	~10%	~0%
2008	~45%	~40%	~15%	~0%
2009	~35%	~45%	~20%	~0%
2010	~25%	~45%	~30%	~0%
2011	~15%	~45%	~40%	~0%
2012	~10%	~45%	~45%	~0%
2013	~5%	~45%	~50%	~0%

Year	1-3	4-5	6-10	11-20	>=21
2010	~60%	~35%	~5%	~0%	~0%
2011	~55%	~35%	~10%	~0%	~0%
2012	~40%	~35%	~20%	~0%	~0%
2013	~35%	~35%	~25%	~0%	~0%

source: Synopsys, 2015, "Addressing IP Integration & Software Development Challenges to Accelerate SoC Time-to-Market", whitepaper.

Parallela/Adapteva

MPPA/Kalray

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Tiled multi-/many-core template

Miro-Panades, E. Beigne, Y. Thonnart, L. Alacoque, P. Vivet, S. Lesecq, D. Puschini, A. Molnos, F. Thabet, K. Benchehida, S. Engels, R. Wilson, D. Fuin, "A fine-grain variation-aware dynamic Vdd-hopping AVFS architecture on a 32nm GALS MPSoC", JSSC 2014

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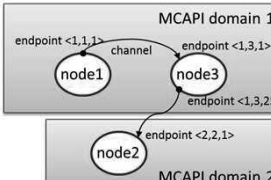



Programming model

- **MCAPI standard**
 - API and a semantic for communication and synchronization between processing cores in embedded systems.
 - message-passing for closely distributed (multiple cores on a chip and/or chips on a board) embedded systems
 - scalable, source-code compatibility (portability), virtually any number of cores
 - different processing architecture, same or a different operating system, or no OS at all.


- primitives:
 - node (independent thread of control, e.g., PE, software thread, HWIP...)
 - domain (logical set of nodes)
 - endpoint (communication port)
 - communication (message, packet channels, scalar channels)







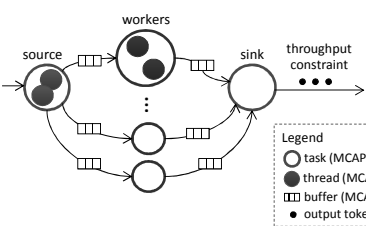
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Application model

- **Data-parallel, in MCAPI**
 - use-case: HMAX models [Serre05]
 - throughput oriented
 - number of tokens/second at sink
 - if throughput constraint not met
 - drop partially computed token
 - reuse partially computed token
 - multiple QoS levels
 - here, QoS = throughput
 - QoS_{max} = maximum throughput attainable at maximum frequency

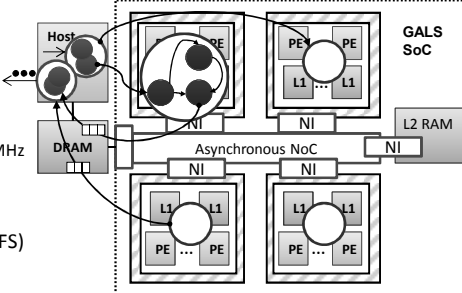
- **Experiments on STHORM test board**
 - 4 tiles, frequency scaling per tile
 - e.g., $F_{max} = 450MHz$, $F_{min} = 100MHz$, $F_{step} = 50MHz$
 - realistic performance, e.g., throughput, # dropped outputs
 - off-line power/energy model (assuming DVFS)




Legend

- task (MCAPI domain)
- thread (MCAPI node)
- buffer (MCAPI channel)
- output token

↓

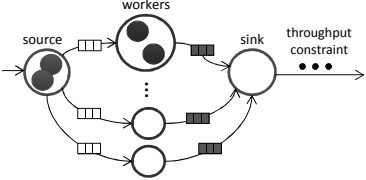




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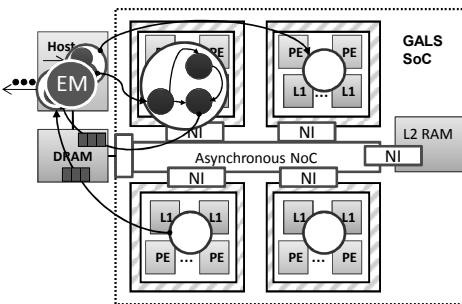
Energy management

- Should respect application throughput
 - ▬ keep output buffer filling at constant level
 - ▬ control theory: potential for good adaptation solutions for dynamic processes.



The diagram shows a flow from a 'source' to 'workers' and then to a 'sink'. The workers are represented by circles with dots inside. A 'throughput constraint' is indicated by an arrow pointing away from the sink.

- Energy manager
 - ▬ per tile, independently
 - ▬ (on the host processor)



The diagram illustrates a GALS SoC architecture. It features a central 'Host' with an 'EM' (Energy Manager) and 'DRAM'. The SoC is composed of multiple 'tiles' (PEs) connected via an 'Asynchronous NoC' (Network-on-Chip). Each tile contains a 'PE' (Processing Element) and 'L1' (Local Cache). The NoC is connected to 'L2 RAM' and 'NI' (Network Interface) blocks.

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State-of-the-art

- Simple controllers, low-overhead
 - ▬ Threshold-based [Alimonda09]
 - similar application model
 - ▬ Proportional integral (PI) [Wu04][Wu05][Carta07][Almeida11]
 - multiple clock-domain microprocessor, chip multi-processors
 - local vs. distributed
- Complex controllers, low-overhead
 - ▬ Custom control [Ogras09][Garg10] [David12]
 - multiple VFI systems
 - fully centralized vs. fully decentralized vs. partially centralized
 - ▬ Fractal controller [Bogdan13]
 - multi-processor system on a chip, multiple VFI systems
 - control the frequency of PEs and routers
 - ▬ Model predictive thermal control [Zanini12][Bartolini12]
- Most approaches validated only in simulation

Here:

- Energy management in relation to application QoS and buffer sizes
- Experiments on a test chip

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The graph shows 'output buffer filling' on the y-axis and 'time' on the x-axis. A dashed line represents the 'buffer size'. A solid line shows the buffer filling level, which rises to the buffer size and then plateaus. A horizontal dashed line below the buffer size is labeled 'throughput constraint'. The region between the buffer size and the throughput constraint is labeled 'Energy management region → PI'. The region below the throughput constraint is labeled 'Critical region → f_{max} '. A point where the buffer filling level drops below the throughput constraint is labeled 'skipped output'. A box labeled 'setpoint' points to the throughput constraint line. A box labeled 'blocked full' points to the top of the buffer size line.

- Assumptions
 - the application throughput is linear in the clock frequency
- Controller design – requirements
 - settling and rise time – no need for highly reactive controller
 - overshoot – not desired
 - steady state error – no strong constraint imposed

A root locus plot in the s-plane with poles marked as 'x' and zeros as 'o'. A box labeled 'poles' points to one of the poles.

Courtesy: "Feedback control of dynamic systems", Gene F. Franklin, 7th Edition, 2014
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ceatech **Results – controller settings**

The plots show Pareto-optimal points for different controller settings. The x-axis for all plots is 'controller reactivity' (high to low). The y-axes are: '% energy reduction (wrt. energy at f_{max})', '% time blocked in full buffers', '# frequency changes', and '# skipped outputs'. The top-left plot is for 'small buffer sizes, high QoS'. The top-right plot is for 'large buffer sizes, low QoS'. The bottom-left plot is for 'small buffer sizes, high QoS' with a different y-axis scale. The bottom-right plot is for 'large buffer sizes, low QoS' with a different y-axis scale. Three points are marked with circled numbers 1, 2, and 3 in all plots.

① high-amplitude frequency variations
 ② low-amplitude frequency variations
 ③ saturation

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output buffer filling vs time

variable trigger controller

output buffer filling vs time

variable trigger controller

- Threshold-based (setpoint) [Alimonda09]
- Variable trigger
 - trigger the controller when FIFO occupancy changes 'significantly'
 - scale up/down the frequency with F_{step}
- Sketch of stability proof

- Thresholds high/low
- Avoids frequent switching, e.g., in temperature regulation
- Variable trigger
 - trigger the controller when FIFO occupancy changes 'significantly'
 - scale up/down the frequency with F_{step}

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ceatech **Results – controllers comparison**

medium QoS level, various buffer size

small buffer size, various QoS levels


- The 3 controllers → energy reductions, 10% – 70%
- PI → less frequency changes
 - wrt 1-threshold, avg. 35% less
 - wrt 2-threshold, avg. 20% less
- PI → skips no output tokens
- Small buffer sizes → non-linear controllers skip output tokens
- The 3 controllers → very low overhead (< 0.2%)

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Conclusions

- MCAPI data-parallel application on a test chip with multiple (V)FI**
 - feedback control in system-level energy management indicates potential
- Proportional-integral based controller with 2 regions**
 - state-of-the-art energy savings
 - reduced number of frequency switches and number of failed application outputs
 - low overhead



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