FROM RESEARCH TO INDUSTRY
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SoC energy management via feedback control for data parallel applications with throughput constraints

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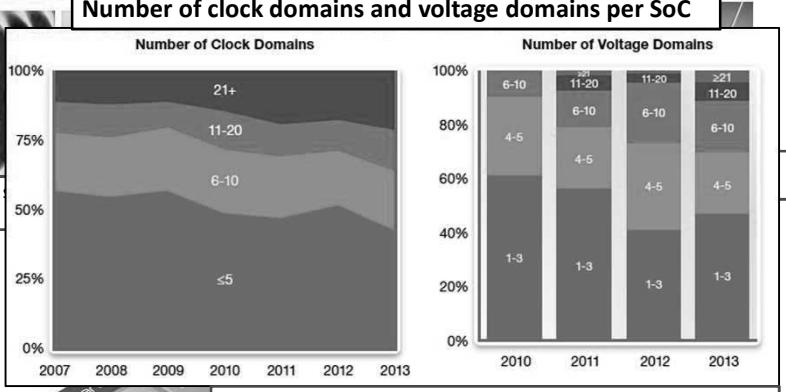
leti & list

- Multi/many–core architecture and programming model
- Energy management via control theory
- Experimental results
- Conclusions

Many-core systems (embedded)

Number of clock domains and voltage domains per SoC



source: **Synopsys, 2015**, "Addressing IP Integration & Software Development Challenges to Accelerate SoC Time-to-Market", whitepaper.

Sound

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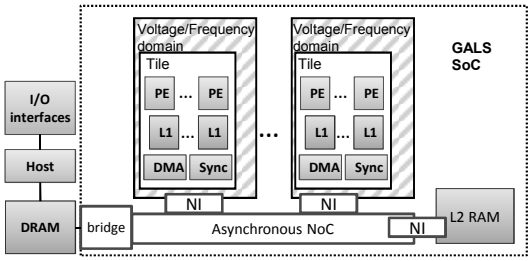
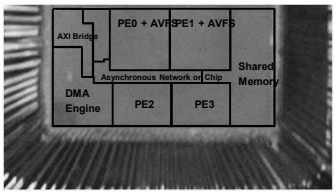
Parallela/Adapteva

MPPA/Kalray

Tiled multi/many–core template





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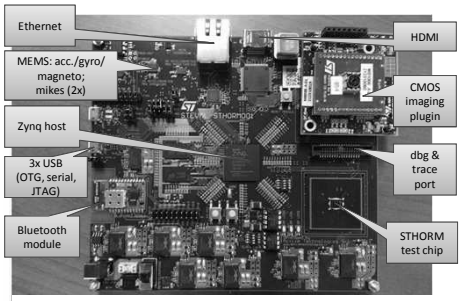

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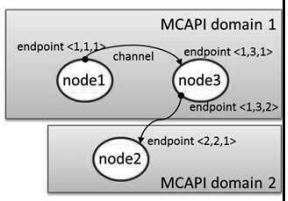
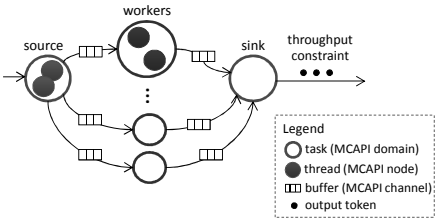
Programming model

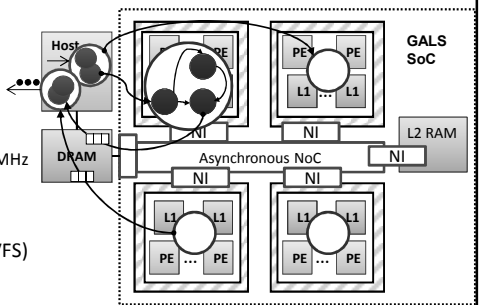
- MCAPI standard
  - API and a semantic for communication and synchronization between processing cores in embedded systems.
    - message-passing for closely distributed (multiple cores on a chip and/or chips on a board) embedded systems
  - scalable, source-code compatibility (portability), virtually any number of cores
    - different processing architecture, same or a different operating system, or no OS at all.
  - primitives:
    - node (independent thread of control, e.g., PE, software thread, HWIP…)
    - domain (logical set of nodes)
    - endpoint (communication port)
    - communication (message, packet channels, scalar channels)



Application model

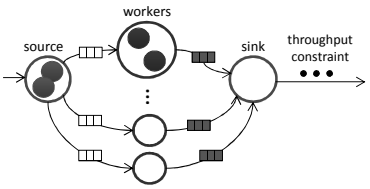
- Data-parallel, in MCAPI
  - use-case: HMAX models [Serre05]
  - throughput oriented
    - number of tokens/second at sink
    - if throughput constraint not met
      - drop partially computed token
      - reuse partially computed token
  - multiple QoS levels
    - here, QoS = throughput
    - QoS_{max} = maximum throughput attainable at maximum frequency
- Experiments on STHORM test board
  - 4 tiles, frequency scaling per tile
    - e.g., F_{max} = 450MHz, F_{min}=100MHz, F_{step}=50MHz
  - realistic performance, e.g., throughput, # dropped outputs
  - off-line power/energy model (assuming DVFS)



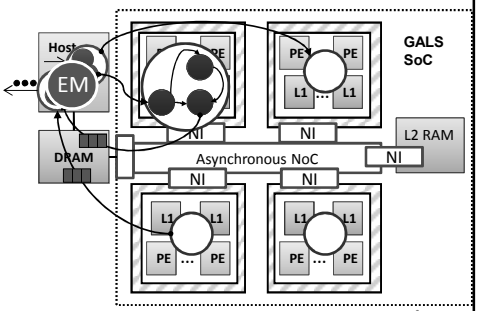


Energy management

- Should respect application throughput
  - keep output buffer filling at constant level
  - control theory: potential for good adaptation solutions for dynamic processes.



- Energy manager
  - per tile, independently
  - (on the host processor)



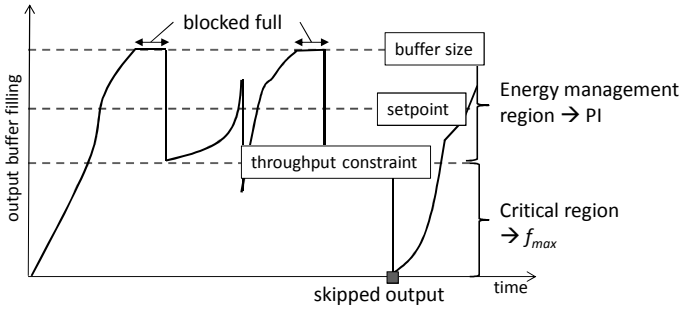
State-of-the-art

- Simple controllers, low-overhead
  - Threshold-based [Alimonda09]
    - similar application model
  - Proportional integral (PI) [Wu04][Wu05][Carta07][Almeida11]
    - multiple clock-domain microprocessor, chip multi-processors
    - local vs. distributed
- Complex controllers, low-overhead
  - Custom control [Ogras09][Garg10] [David12]
    - multiple VFI systems
    - fully centralized vs. fully decentralized vs. partially centralized
  - Fractal controller [Bogdan13]
    - multi-processor system on a chip, multiple VFI systems
    - control the frequency of PEs and routers
  - Model predictive thermal control [Zanini12][Bartolini12]
- Most approaches validated only in simulation

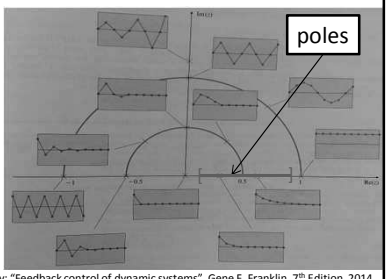
Here:

- Energy management in relation to application QoS and buffer sizes
- Experiments on a test chip

PI–based controller



- Assumptions
  - the application throughput is linear in the clock frequency
- Controller design – requirements
  - *settling and rise time* – no need for highly reactive controller
  - *overshoot* – not desired
  - *steady state error* – no strong constraint imposed

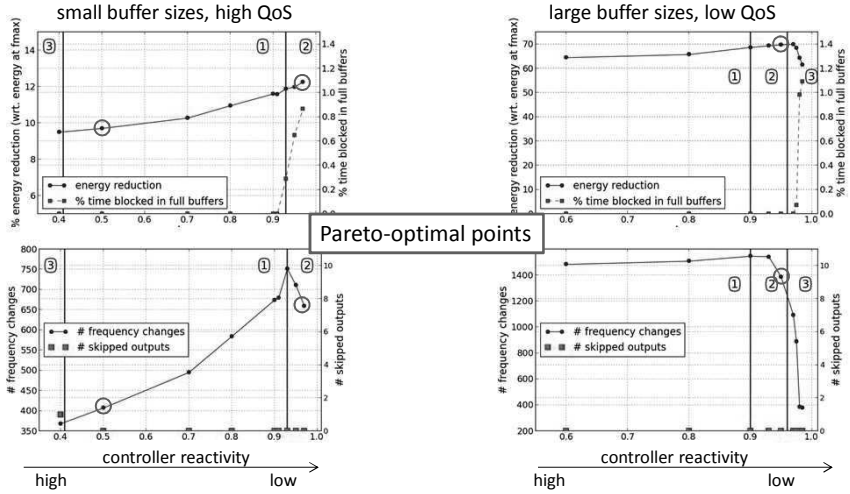


Courtesy: "Feedback control of dynamic systems", Gene F. Franklin, 7th Edition, 2014

Results – controller settings

small buffer sizes, high QoS

large buffer sizes, low QoS

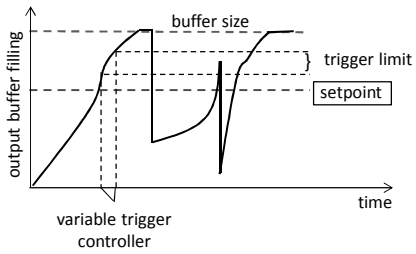


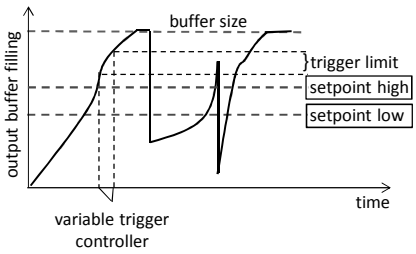
① high-amplitude frequency variations

② low-amplitude frequency variations

③ saturation

Comparison – non-linear controllers





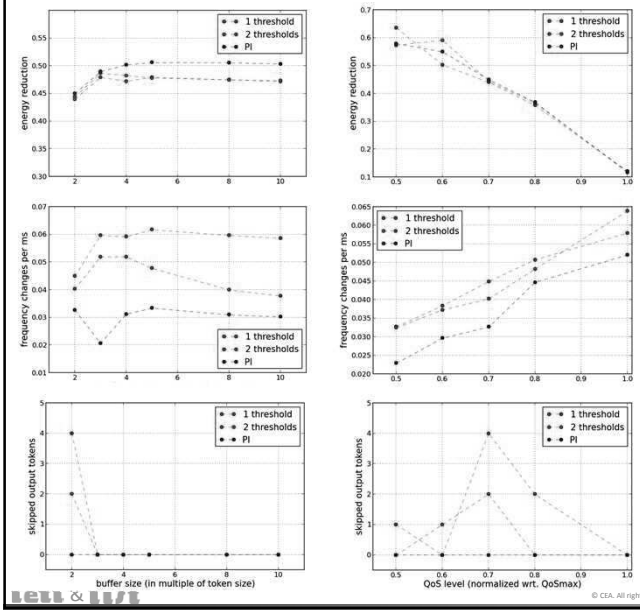
- Threshold–based (setpoint) [Alimonda09]
- Variable trigger
  - trigger the controller when FIFO occupancy changes 'significantly'
  - scale up/down the frequency with F_{step}
- Sketch of stability proof

- Thresholds high/low
- Avoids frequent switching, e.g., in temperature regulation
- Variable trigger
  - trigger the controller when FIFO occupancy changes 'significantly'
  - scale up/down the frequency with F_{step}

Results – controllers comparison

medium QoS level, various buffer size

small buffer size, various QoS levels



- The 3 controllers → energy reductions, 10% – 70%
- PI → less frequency changes
  - wrt 1-threshold, avg. 35% less
  - wrt 2-threshold, avg. 20% less
- PI → skips no output tokens
- Small buffer sizes → non-linear controllers skip output tokens
- The 3 controllers → very low overhead (< 0.2%)

Conclusions

- MCAPI data-parallel application on a test chip with multiple (V)FI
  - feedback control in system-level energy management indicates potential
- Proportional-integral based controller with 2 regions
  - state-of-the-art energy savings
  - reduced number of frequency switches and number of failed application outputs
  - low overhead

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Thank you!

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