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## SoC energy management via feedback control for data parallel applications with throughput constraints

Anca Molnos  
CEA LETI, Grenoble, France

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**leti & list**

- Multi/many-core architecture and programming model
- Energy management via control theory
- Experimental results
- Conclusions

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## Many-core systems (embedded)

### Number of clock domains and voltage domains per SoC

Year	<=5	6-10	11-20	21+
2007	~55%	~35%	~10%	~0%
2008	~50%	~35%	~15%	~0%
2009	~45%	~30%	~20%	~5%
2010	~40%	~25%	~25%	~10%
2011	~35%	~20%	~30%	~15%
2012	~30%	~15%	~35%	~20%
2013	~25%	~10%	~40%	~25%

Year	1-3	4-5	6-10	11-20	>=21
2010	~60%	~35%	~5%	~0%	~0%
2011	~55%	~30%	~10%	~5%	~0%
2012	~40%	~25%	~20%	~10%	~0%
2013	~35%	~20%	~25%	~15%	~5%

source: Synopsys, 2015, "Addressing IP Integration & Software Development Challenges to Accelerate SoC Time-to-Market", whitepaper.

Parallela/Adapteva

MPPA/Kalray

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## Tiled multi/multi-core template

Miro-Panades, E. Beigne, Y. Thonnart, L. Alacoque, P. Vivet, S. Lesecq, D. Puschini, A. Molnos, F. Thabet, K. Benchehida, S. Engels, R. Wilson, D. Fuin, "A fine-grain variation-aware dynamic Vdd-hopping AVFS architecture on a 32nm GALS MPSoC", JSSC 2014

D. Meljignano, L. Berini, E. Flamand, B. Jégo, T. Lepley, G. Haugou, F. Clermidy, D. Dutail, "Platform 2012, a many-core computing accelerator for embedded SoCs: performance evaluation of visual analytics applications." DAC 2012: 1137-1142

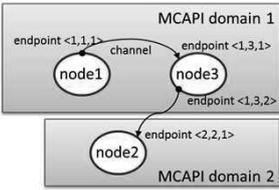
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# Programming model

- **MCAPI standard**
  - API and a semantic for communication and synchronization between processing cores in embedded systems.
    - message-passing for closely distributed (multiple cores on a chip and/or chips on a board) embedded systems
  - scalable, source-code compatibility (portability), virtually any number of cores
    - different processing architecture, same or a different operating system, or no OS at all.
  
- primitives:
  - node (independent thread of control, e.g., PE, software thread, HWIP...)
  - domain (logical set of nodes)
  - endpoint (communication port)
  - communication (message, packet channels, scalar channels)





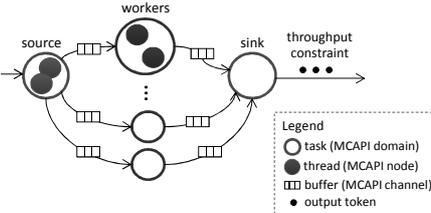


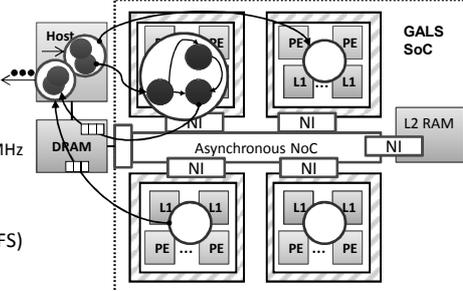
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# Application model

- **Data-parallel, in MCAPI**
  - use-case: HMAX models [Serre05]
  - throughput oriented
    - number of tokens/second at sink
    - if throughput constraint not met
      - drop partially computed token
      - reuse partially computed token
  - multiple QoS levels
    - here, QoS = throughput
    - $QoS_{max}$  = maximum throughput attainable at maximum frequency
  
- **Experiments on STHORM test board**
  - 4 tiles, frequency scaling per tile
    - e.g.,  $F_{max} = 450MHz$ ,  $F_{min} = 100MHz$ ,  $F_{step} = 50MHz$
  - realistic performance, e.g., throughput, # dropped outputs
  - off-line power/energy model (assuming DVFS)



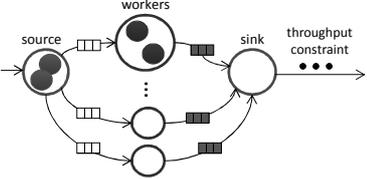




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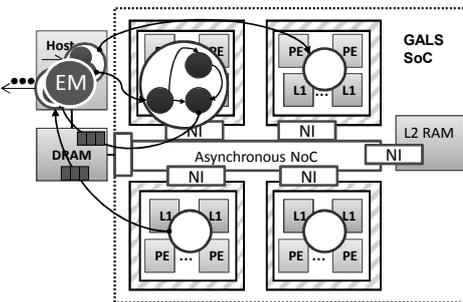
**Energy management**

- Should respect application throughput
  - ▬ keep output buffer filling at constant level
  - ▬ control theory: potential for good adaptation solutions for dynamic processes.



The diagram shows a flow from a 'source' to 'workers' and then to a 'sink'. A 'throughput constraint' is indicated by an arrow pointing away from the sink. The workers are represented by circles with internal components, and the source and sink are also circles with internal components. Arrows indicate the direction of flow.

- Energy manager
  - ▬ per tile, independently
  - ▬ (on the host processor)



The diagram illustrates a GALS SoC architecture. It features a central 'Asynchronous NoC' (Network-on-Chip) connecting multiple processing tiles. Each tile contains a 'PE' (Processing Element) and 'L1' (Local Cache). The system is connected to a 'Host' and 'DRAM' via an 'EM' (Energy Manager). 'L2 RAM' is also shown. The architecture is labeled 'GALS SoC'.

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**State-of-the-art**

- Simple controllers, low-overhead
  - ▬ Threshold-based [Alimonda09]
    - similar application model
  - ▬ Proportional integral (PI) [Wu04][Wu05][Carta07][Almeida11]
    - multiple clock-domain microprocessor, chip multi-processors
    - local vs. distributed
- Complex controllers, low-overhead
  - ▬ Custom control [Ogras09][Garg10] [David12]
    - multiple VFI systems
    - fully centralized vs. fully decentralized vs. partially centralized
  - ▬ Fractal controller [Bogdan13]
    - multi-processor system on a chip, multiple VFI systems
    - control the frequency of PEs and routers
  - ▬ Model predictive thermal control [Zanini12][Bartolini12]
- Most approaches validated only in simulation

Here:

- Energy management in relation to application QoS and buffer sizes
- Experiments on a test chip

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## PI-based controller

The graph shows 'output buffer filling' on the y-axis and 'time' on the x-axis. A dashed line represents the 'buffer size'. A solid line shows the buffer filling level, which rises to the buffer size and then plateaus. A horizontal dashed line below the buffer size is labeled 'throughput constraint'. The region between the buffer size and the throughput constraint is labeled 'Energy management region → PI'. The region below the throughput constraint is labeled 'Critical region →  $f_{max}$ '. A vertical dashed line marks the 'setpoint'. A point where the buffer filling level drops below the throughput constraint is labeled 'skipped output'. A label 'blocked full' points to the top of the buffer size line.

- Assumptions
  - the application throughput is linear in the clock frequency
- Controller design – requirements
  - settling and rise time – no need for highly reactive controller
  - overshoot – not desired
  - steady state error – no strong constraint imposed

The pole-zero plot shows the real and imaginary parts of poles and zeros. A label 'poles' points to a pair of poles in the right half plane.

Courtesy: "Feedback control of dynamic systems", Gene F. Franklin, 7<sup>th</sup> Edition, 2014  
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## Results – controller settings

**small buffer sizes, high QoS**

Y-axis: % energy reduction (wrt. energy at  $f_{max}$ ) and % time blocked in full buffers. X-axis: controller reactivity (high to low). Legend: energy reduction (circles), % time blocked in full buffers (squares). Three Pareto-optimal points are marked with 1, 2, and 3.

**large buffer sizes, low QoS**

Y-axis: energy reduction (wrt. energy at  $f_{max}$ ) and % time blocked in full buffers. X-axis: controller reactivity (high to low). Legend: energy reduction (circles), % time blocked in full buffers (squares). Three Pareto-optimal points are marked with 1, 2, and 3.

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① high-amplitude frequency variations  
 ② low-amplitude frequency variations  
 ③ saturation

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## Comparison – non-linear controllers

variable trigger controller

variable trigger controller

- Threshold-based (setpoint) [Alimonda09]
- Variable trigger
  - trigger the controller when FIFO occupancy changes 'significantly'
  - scale up/down the frequency with  $F_{step}$
- Sketch of stability proof

- Thresholds high/low
- Avoids frequent switching, e.g., in temperature regulation
- Variable trigger
  - trigger the controller when FIFO occupancy changes 'significantly'
  - scale up/down the frequency with  $F_{step}$

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## Results – controllers comparison

medium QoS level, various buffer size

small buffer size, various QoS levels

- The 3 controllers → energy reductions, 10% – 70%
- PI → less frequency changes
  - wrt 1-threshold, avg. 35% less
  - wrt 2-threshold, avg. 20% less
- PI → skips no output tokens
- Small buffer sizes → non-linear controllers skip output tokens
- The 3 controllers → very low overhead (< 0.2%)

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## Conclusions

- MCAPI data-parallel application on a test chip with multiple (V)FI
  - feedback control in system-level energy management indicates potential
  
- Proportional-integral based controller with 2 regions
  - state-of-the-art energy savings
  - reduced number of frequency switches and number of failed application outputs
  - low overhead



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CEA-LETI, FR

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**let**  
Centre de Grenoble  
17 rue des Martyrs  
38054 Grenoble Cedex

**list**  
Centre de Saclay  
Nano-innov PC 172  
91191 Gif sur Yvette Cedex