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Higher reliable multiprocessor system for embedded systems considering power source fluctuation

Yoshinori TAKEUCHI
Graduate School of Information Science and Technology
Osaka University

Osaka University

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Introduction

- Requirement for embedded systems
  - Low power
  - High performance
- MPSoC is expected for one of solutions as software defined hardware
  - High-performance and multi-function SoC
    - Multiple Processing Elements (PE)
    - Multicore or many core implementation
  - Strict design constraints
    - Advancement in process technology supports high performance, small area, low power consumption
- Operating supply voltage is shrinking in order to save power consumption

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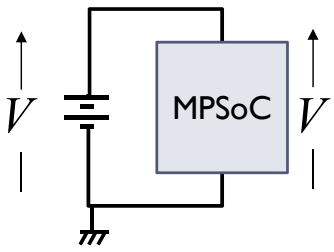
Reliability considering power supply noise

- Reason
  - Low operating voltage by advancement of technology
  - Near or sub-threshold operations on low power operation
- Noise from power supply swing becomes relatively-large
  - Noise by peak current I_{max}

$$Ev = L\frac{di}{dt}$$

    - This effect becomes large when clock frequency becomes higher and peak current becomes larger
  - Noise by electrical resonance on power line

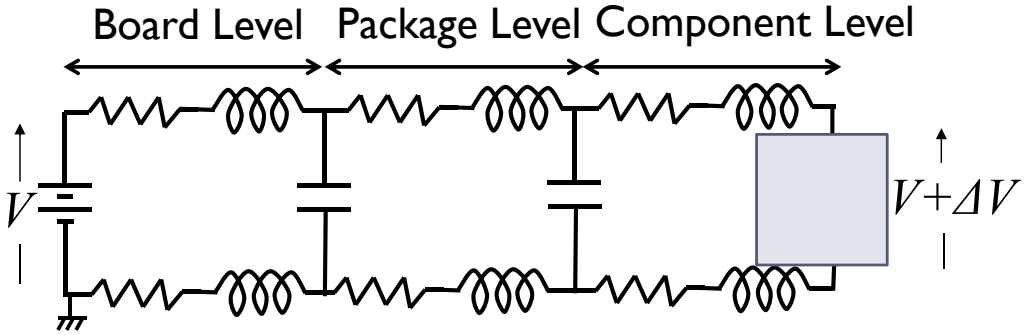
Power supply model for SoC



Long wires
Large capacitors

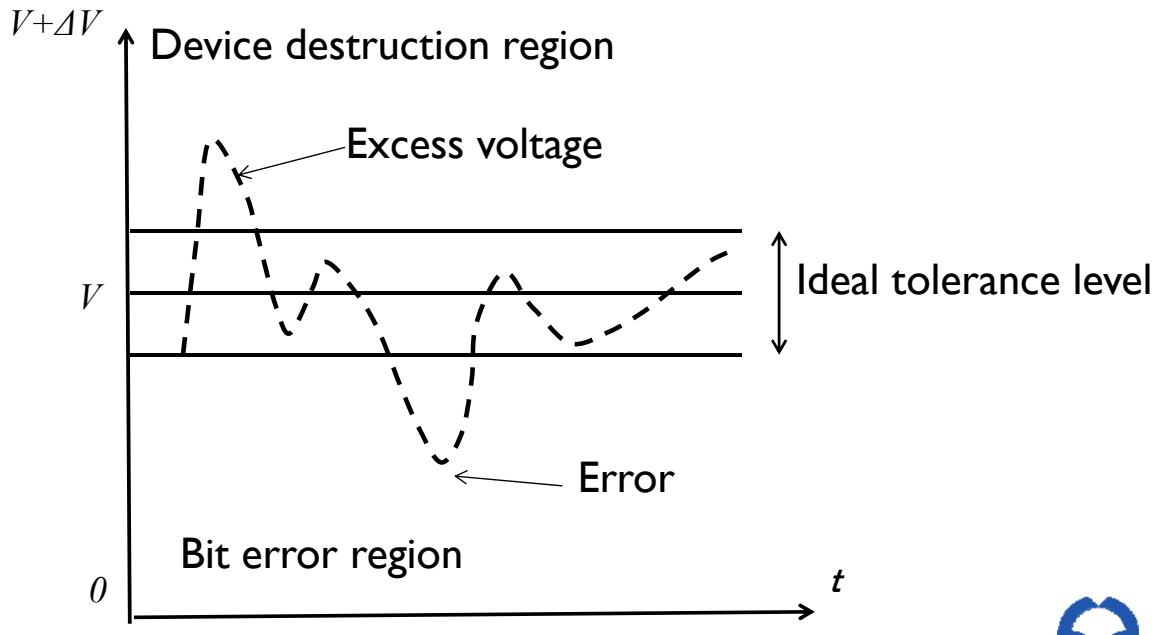
+Parasitic elements

ideal



Real circuit

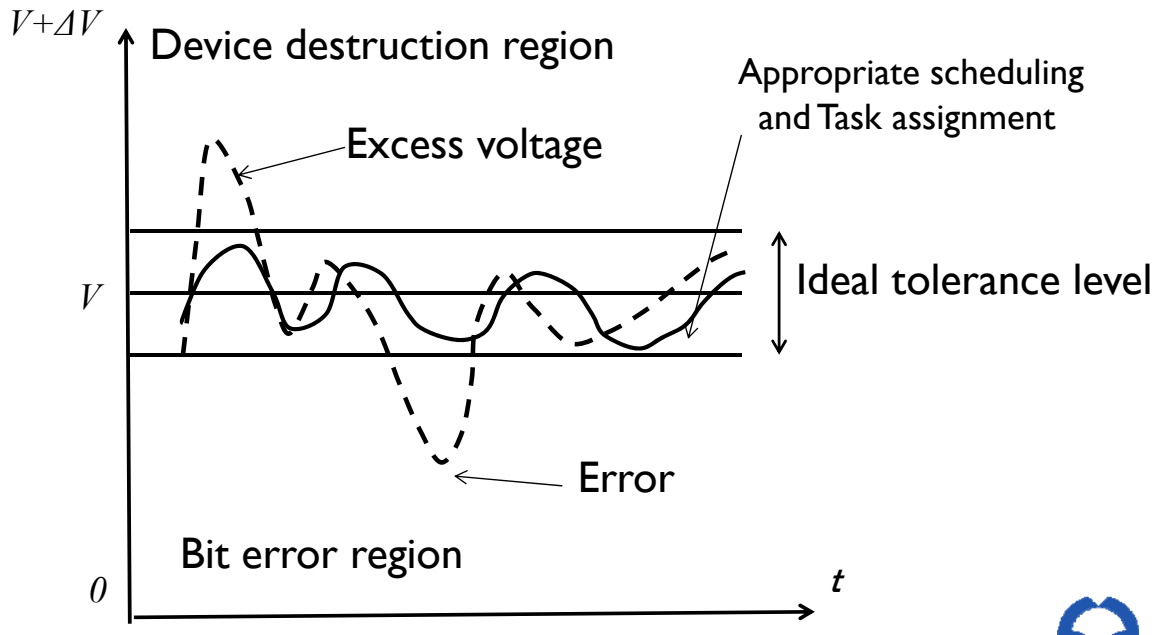
Power supply swing



Approach to tolerance to power noise at each level

- Architecture level design
  - Topology
- Circuit level design
  - Impedance
- Software level design
  - Task assignment
  - Instruction scheduling

Power supply swing



Preliminary study

- Scheduling considering peak current
  - Processor like VLIW issues multiple operations at a time
  - Current largely changes time by time
  - Conservative design tolerant to worst case (the largest) current
- Propose instruction scheduling limiting the peak current

Related work for instruction scheduling

- Xiao [1]
  - Reduce power keeping performance
  - Not appropriate method for limiting peak current
- Toburen [2]
  - Limit peak current accepting performance loss
  - Not model pipeline behavior

[1] S. Xiao and E. M.-K. Lai, "A rough programming approach to power-balanced instruction scheduling for VLIW digital signal processors," IEEE Transactions on Signal Processing, vol. 56, no. 4, pp. 1698–1709, Apr. 2008.

[2] M. Toburen, T. M. Conte, and M. Reilly, "Instruction scheduling for low power dissipation in high performance microprocessors," in Proceedings of the Power Driven Micro-architecture Workshop in conjunction with the ISCA ' 1998.

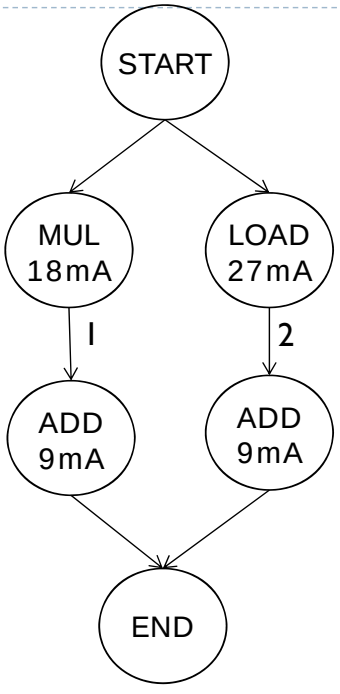
Example of ref [2]

- No current constraint

	slot1	slot2	current [mA]
cycle1	LOAD	MUL	45
cycle2	ADD		9
cycle3	ADD		9

- Current constraint = 30mA

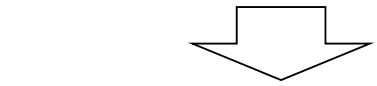
	slot1	slot2	current [mA]
cycle1	LOAD		27
cycle2	MUL		18
cycle3	ADD	ADD	18



DDG

Limitation of ref [2]

- Current is computed by issued instructions
  - In pipeline architecture, current transition of each stage depends on instruction



Unexpected current

Current by instruction [mA]

LOAD	27
ADD	9
MUL	18

Current by stage [mA]

	IF	ID	EX	WB
LOAD	30	2	3	22
ADD	30	4	3	2
MUL	30	4	12	2

Current estimation by proposed method

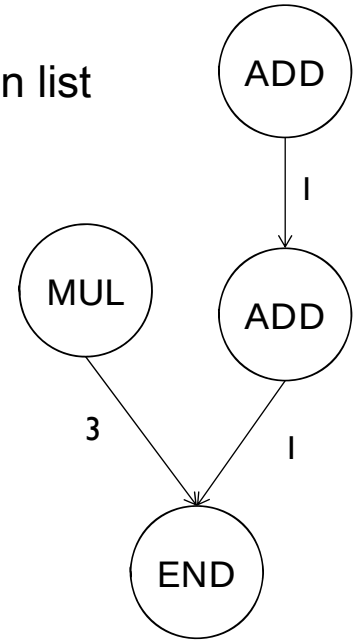
- Current estimation by each stage

Current computation example[mA]

	IF	ID	EX	WB	Sum
Cycle 1	MUL: 30				30
Cycle 2	ADD: 30	MUL: 4			34
Cycle 3	LOAD: 30	ADD: 4	MUL: 12		46
Cycle 4	NOP: 30	LOAD: 2	ADD: 3	MUL: 2	37
Cycle 5	NOP: 30	NOP: 0	LOAD: 3	ADD: 2	35
Cycle 6	NOP: 30	NOP: 0	NOP: 0	LOAD: 22	52

Proposed algorithm

- List scheduling based algorithm
  - Assign inst. from available instruction list
- Priority evaluation
  - Delay time total between inst.
  - MUL is highest in the right example
- Current check at assigning inst.



DDG example

Experimental setup

- Benchmark: DSPstone
  - Comparisons with opt.: loop
  - Comparisons with ref [2]: program
- Functional units : Right table
- Max multiple issued instructions : 4
- Current constraint : from 12mA to 20mA

Functional unit

Function	#
ALU	4
Mul	2
Div	1
Shifter	2
Load/Store	2

Experimental results

Above: Optimal Ex. Cycles
Below: Ex. Cycles by proposed method

	conv.	fir	dot_p.	lms	real_up.	mat.1	mat.2	fft	sum	ratio
12mA	N/A	N/A	N/A	10	10	9	14	N/A	43	1.14
	30	30	31	11	11	11	16	90	49	
13mA	20	21	N/A	8	8	7	11	N/A	75	1.12
	21	22	21	10	10	8	13	63	84	
14mA	17	20	18	7	7	6	10	N/A	85	1.07
	20	20	20	7	7	7	10	56	91	
15mA	17	N/A	N/A	7	7	4	9	N/A	44	1.11
	18	22	20	7	7	7	10	51	49	
16mA	16	N/A	N/A	7	7	4	8	N/A	42	1.07
	17	18	18	7	7	4	10	52	45	
17mA	15	N/A	N/A	7	7	4	8	N/A	41	1.07
	15	18	17	7	7	5	10	45	44	
18mA	15	N/A	N/A	7	7	3	N/A	N/A	32	1.03
	15	18	16	7	7	4	10	44	33	
19mA	15	N/A	N/A	7	7	3	N/A	N/A	32	1.03
	15	18	16	7	7	4	8	44	33	
20mA	N/A	N/A	N/A	7	7	3	N/A	N/A	17	1.06
	15	18	16	7	7	4	8	43	18	
sum									428/394	1.09

Experimental result

Constraint	Ex. cycles		Peak/Constraint		Violation count	
	Ref[2]	Proposed	Ref[2]	Proposed	Ref[2]	Proposed
12mA	N/A	232,104	N/A	0.99	N/A	0
13mA	187,010	192,846	1.17	0.99	13,632	0
14mA	186,105	178,655	1.08	0.99	5,607	0
15mA	175,973	175,207	1.09	1.00	2,351	0
16mA	172,583	165,566	1.01	0.99	901	0
17mA	170,008	161,091	1.08	1.00	27	0
18mA	159,318	158,801	1.07	1.00	68	0
19mA	159,159	158,298	1.09	1.00	52	0
20mA	158,882	158,247	1.04	0.99	1	0

- Ref2 violates 8% cycles under 13mA constraint

Conclusion and Future Work

- Conclusion
  - Proposes noise reduction method by limiting peak current using instruction scheduling as a preliminary study
  - Proposes a method considering pipeline architecture behavior
- Future Work
  - Reduce peak current by task assignment for MPSoC
  - Reduce electrical resonance effect by task assignment and instruction scheduling for MPSoC

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Acknowledgement

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Thank you for your attention!

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