A Few Open Problems in Vertically-Partially-Connected 3D-NoC

Frédéric Pétrot and Hamed Sheibanyrad

System-Level Synthesis Group
TIMA Laboratory
46, Av Félix Viallet, 38031 Grenoble, France

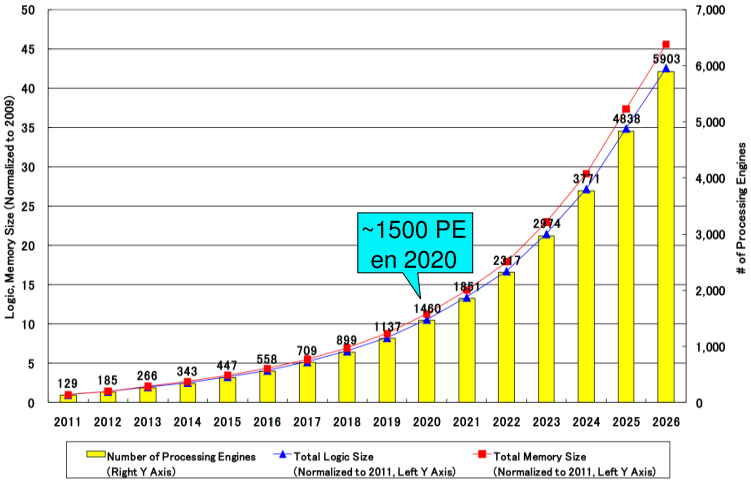
July 17th, 2015

3D Integration, an opportunity

Transistor, Bell Labs, Murray Hill, New Jersey, 1947

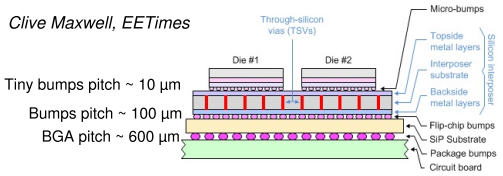
3D Integration, an opportunity

A way to follow ITRS roadmap



# of PE in consumer products

For SIP/SIP++: μBumps

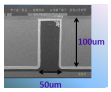


For SoC: TSV

TSV parameters	2011 2014	2015 2018
Diameter	4 to 8 μm	2 to 4 μm
Pitch	8 to 16 μm	4 to 8 μm
Layers	2 to 3	2 to 4

Via First, Polysilicon filled
Source : G. Pares CEA-LETI

diamètre ≈ 5 µm
pas ≈ 10 µm



diamètre ≈ 35 µm
pas ≈ 50 µm

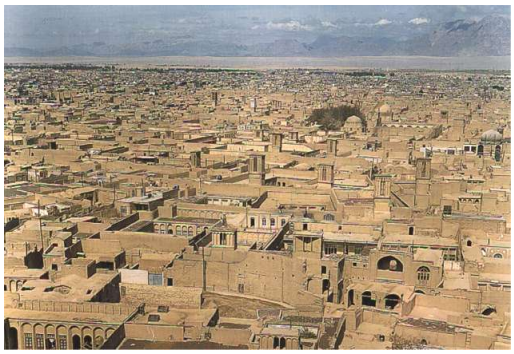
Via Last, Cu liner
Source : Allvia, 2011

3D Integration, a reality, but ...

Technological and micro-architectural uncertainties

3D Integration, a reality, but ...

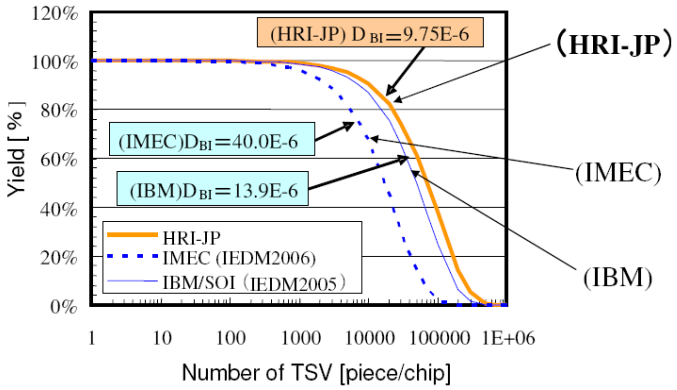
Technological and micro-architectural uncertainties



3D Integration, a reality, but ...

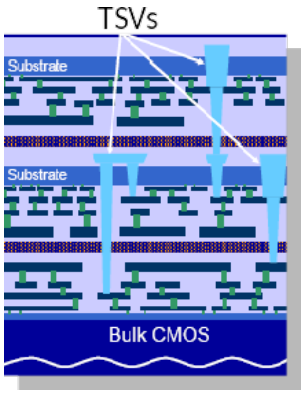
Technological and micro-architectural uncertainties

- What yield for a full circuit with TSV?



C. Seiculescu et al.

- What area can be dedicated to TSV?

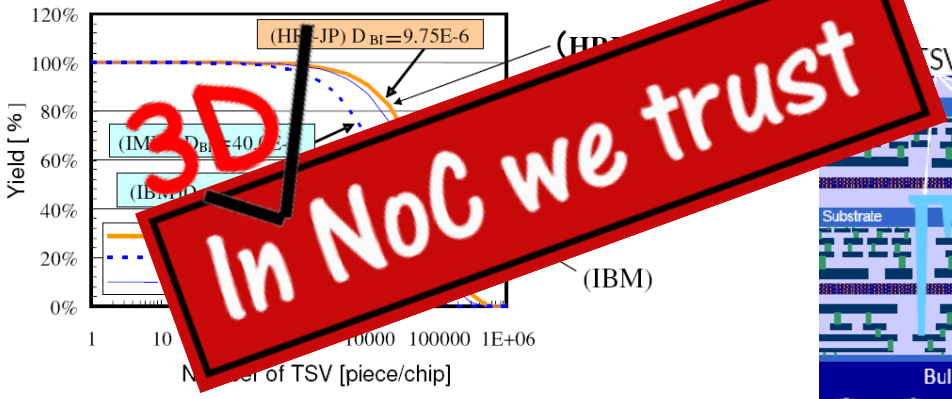


Frédéric Pétrot (TIMA Lab) MPSoC'15 July 17th, 2015 3 / 14

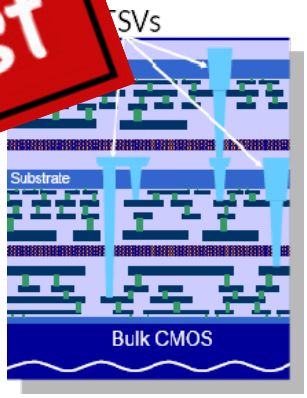
3D Integration, a reality, but ...

Technological and micro-architectural uncertainties

- What yield for a full circuit with TSV?
- What area can be d ed to TSV?



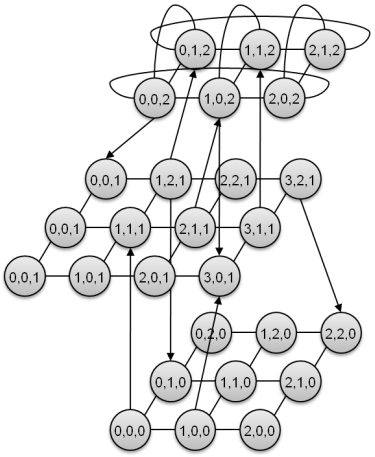
C. Seiculescu et al.

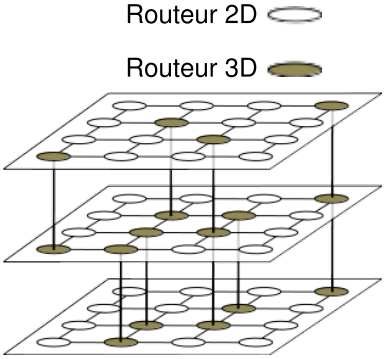


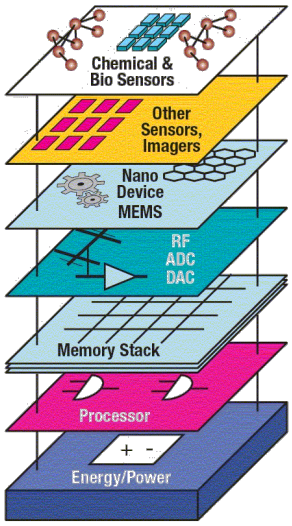
Vertically-Partially-Connected 3D-NoC

- Number of vertical connections necessarily limited
- Making use of tiers fabricated independently
  - heterogeneous technologies
  - irregular topologies

Vertically-Partially-Connected topologies as solution



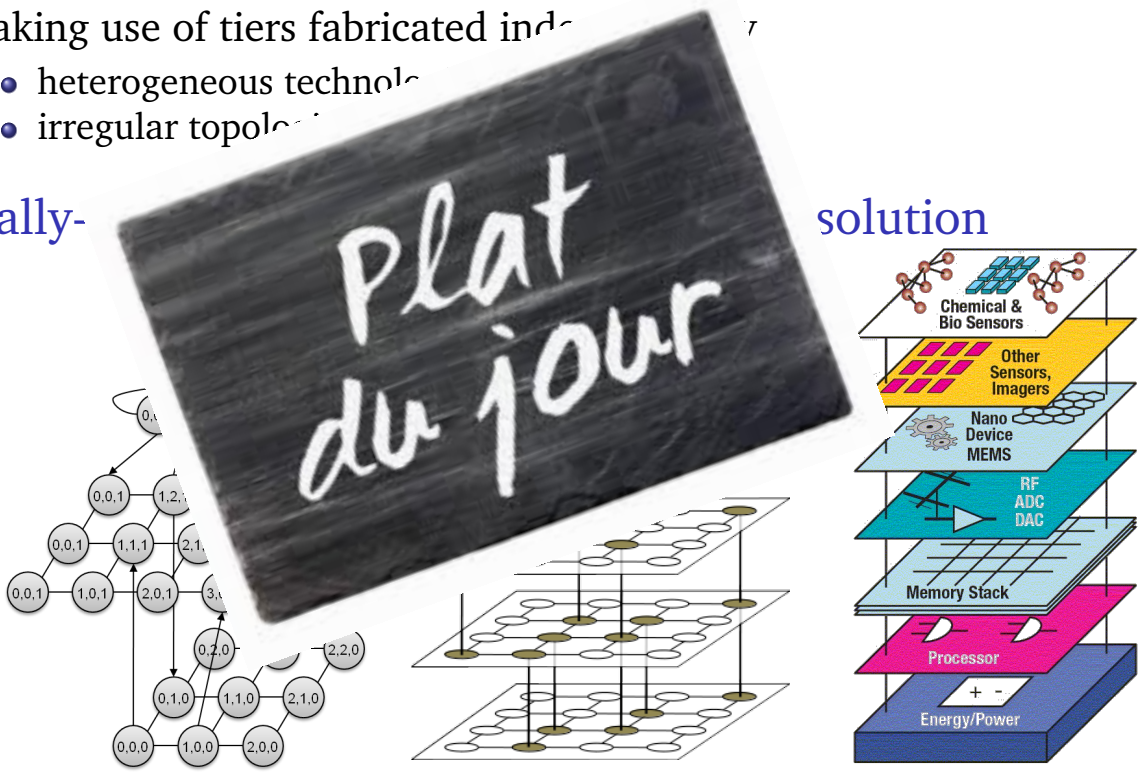




Vertically-Partially-Connected 3D-NoC

- Number of vertical connections necessarily limited
- Making use of tiers fabricated ind
  - heterogeneous technol
  - irregular topol

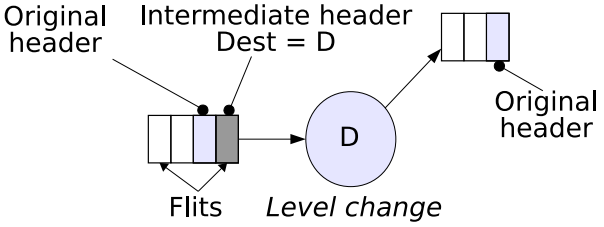
Vertically- solution



Routing in VPC 3D-NoC (*c.f.* MPSoC'12)

Principle[1]

- Accessible up link (x_{up}, y_{up}) and downlink (x_{dn}, y_{dn}) coordinates assigned to each router
  - Message internal to a plane: use the algorithm defined for this plane
  - Message traveling between planes:
    - use plane relative algorithm towards (x_{up}, y_{up}) if destination in an upper plane, towards (x_{dn}, y_{dn}) otherwise
    - do this again until reaching destination
- Implementation



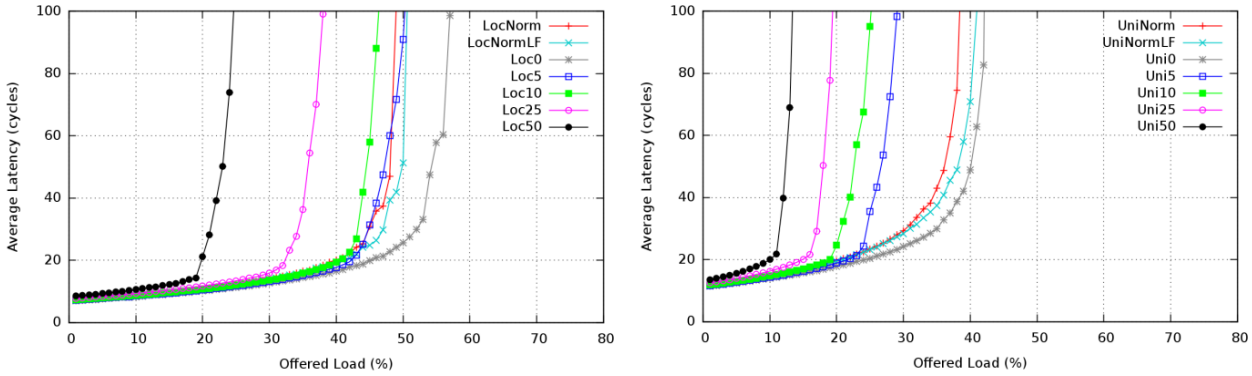
- But only the tip of the Iceberg, . . .

[1] Florentine Dubois, Abbas Sheibanyrad, Frédéric Pétrot, Maryam Bahmani. *Elevator-First: A Deadlock-Free Distributed Routing Algorithm for Vertically Partially Connected 3D-NoCs.* IEEE Trans. Computers 62(3): 609-615 (2013).

Number of Elevators

Up link and downlink routers

$5 \times 5 \times 5$ Cube, Uniform Random and Localized Traffic,
Random Elevator Placement, Closest Neighbour Node Assignment



Constrained by technology:

- TSV size, circuit size
- TSV throughput
- Target yield

Design time decision

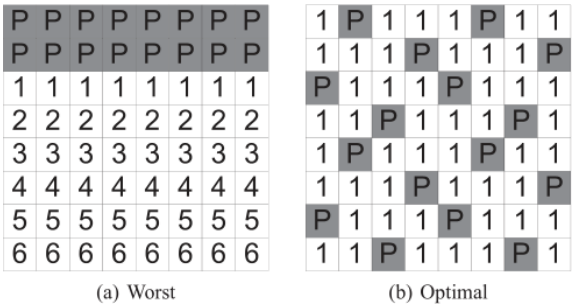
Elevator Placement

For a given traffic pattern/application domain, where should the elevators be placed?

Example for a 8x8x2 3D mesh,
Uniform random traffic,
Adaptive routing:
Optimal minimizes hop-count, ...

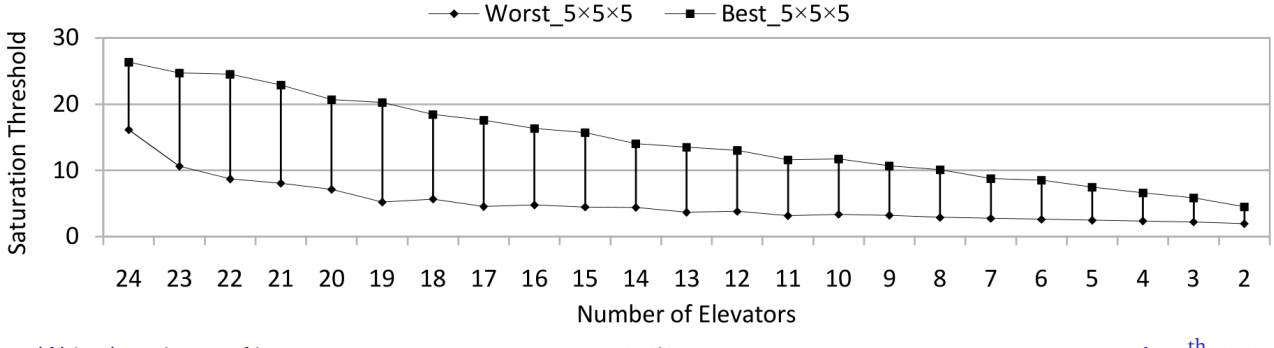
What about deterministic routing?
Hot-spot or domain specific traffic?

Source: Xu *et al.*



(a) Worst (b) Optimal

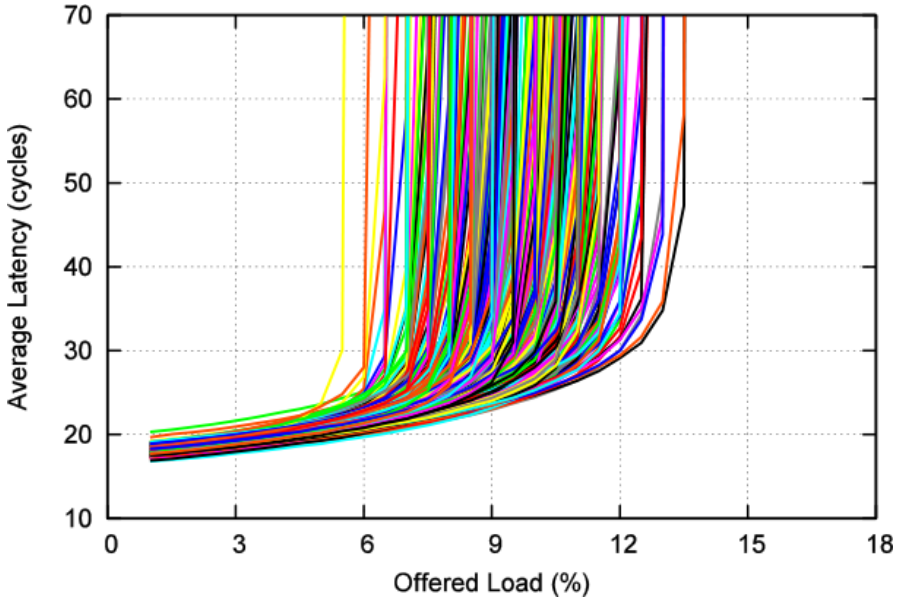
Placing 16 vertical connections (P)



Elevator Assignment

For a given placement of the elevators, which elevator is to be assigned to any given node?

$5 \times 5 \times 5$ Cube, Uniform Random Traffic, 50% Nodes are Elevator, Fixed Position, Random Elevator Assignment



Saturation threshold varies by more than 250%

Elevator Assignment

Problem Statement

Average Saturation Threshold Optimization by Assigning Elevators to Nodes

Solution Space

Number of possible solution for a $5 \times 5 \times 5$ Cube with 50% Elevators:

$$\overbrace{\left(\underbrace{12.5^{12.5}}_{\text{per tier}}\right)^4}^{\text{Up Elevator}} \times \overbrace{\left(\underbrace{12.5^{12.5}}_{\text{per tier}}\right)^4}^{\text{Down Elevator}} = 12.5^{100}$$

Complexity

NP-Complete General Assignment Problem (GAP)

Elevator Assignment

Tabu search

Identified as the most efficient heuristic for GAP problems

Principle

Identify the first link which saturate and deflect it on a less loaded one

Cost Function

$$f = \sum_{l \in L} BU(l) \times e^{BU(l)}$$

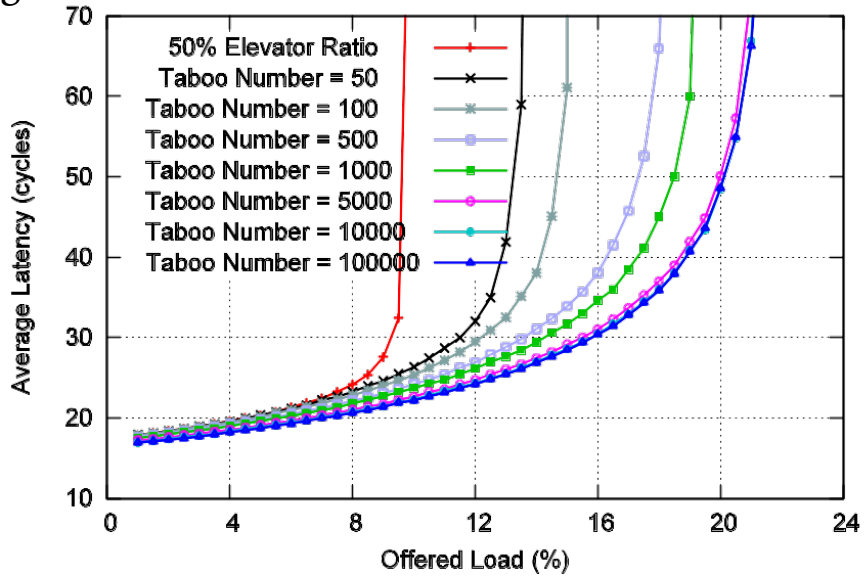
L : set of links
$BU(l)$: utilization ratio of link l in the new assignment[2]
$e^{BU(l)}$: arbitrary function growing very fast if $BU(l)$ grows

[2]Sahar Foroutan, Yvain Thonnart, Frédéric Pétrot. *An Iterative Computational Technique for Performance Evaluation of Networks-on-Chip,* IEEE Trans. Computers 62(8): 1641-1655 (2013)

Elevator Assignment

Convergence and Execution Time

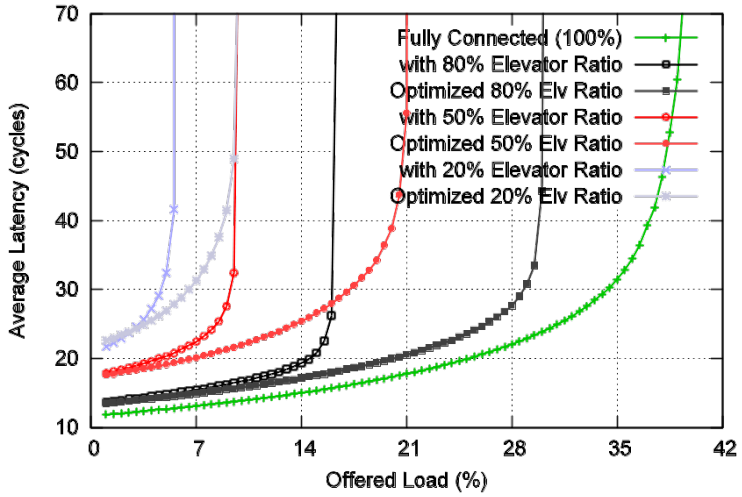
Initial Assignment: one of the nearest



Tabu Number	Hop Count	Run Time
0	5.78	-
100	5.98	41 s
1000	6.34	617 s (10 m)
10000	6.37	13449 s (4 h)

Elevator Assignment

Comparison with a random assignment



Mode details in [3]

[3] Sahar Foroutan, Abbas Sheibanyrad, Frédéric Pétrot: *Assignment of Vertical-Links to Routers in Vertically-Partially-Connected 3-D-NoCs.* IEEE Trans. on CAD of Integrated Circuits and Systems 33(8): 1208-1218 (2014).

Conclusion

Vertically-Partially-Connected 3D-NoC

- Still relatively academic issue
- Many classical problems to look at in this context
  - Routing algorithms
  - Elevator number and position, as a function of routing
  - Elevator assignment
  - Dimensioning
  - 2D/3D Topologies
  - Fault tolerance
  - ...
- First solutions on Routing and Assignment

Acknowledgments

Many thanks to

Maryam Bahamani (PhD, now with Arteris),
Florentine Dubois (PhD, now with Synopsys EV)
Sahar Forourtan (Post-Doc, now with Synposys EV)