TOSHIBA
Leading Innovation

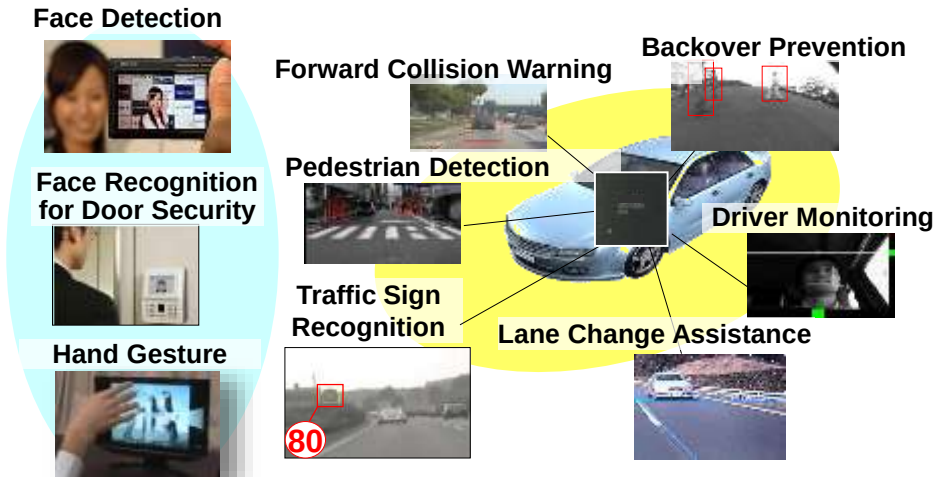
Design of Heterogeneous Multi-Core SoCs for ADAS and Image Recognition Applications

Takashi Miyamori, Senior Manager
Digital Media SoC Dept.
Center for Semiconductor Research & Development
Semiconductor & Storage Products Company

TOSHIBA Corporation
July 13, 2015

Background

Image recognition technology ⇨ A variety of products



The Top 10 Causes of Death

2015	
Rank	Cause
1	Ischaemic heart disease
2	Stroke
3	Lower respiratory infections
4	Chronic obstructive pulmonary disease
5	Diarrhoeal diseases
6	HIV/AIDS
7	Trachea, bronchus, lung cancers
8	Diabetes mellitus
9	**Road injury**
10	Hypertensive heart disease

1.4 million

2030	
Rank	Cause
1	Ischaemic heart disease
2	Stroke
3	Chronic obstructive pulmonary disease
4	Lower respiratory infections
5	Diarrhoeal diseases
6	Trachea, bronchus, lung cancers
7	**Road injury**
8	HIV/AIDS
9	Diarrhoeal diseases
10	Hypertensive heart disease

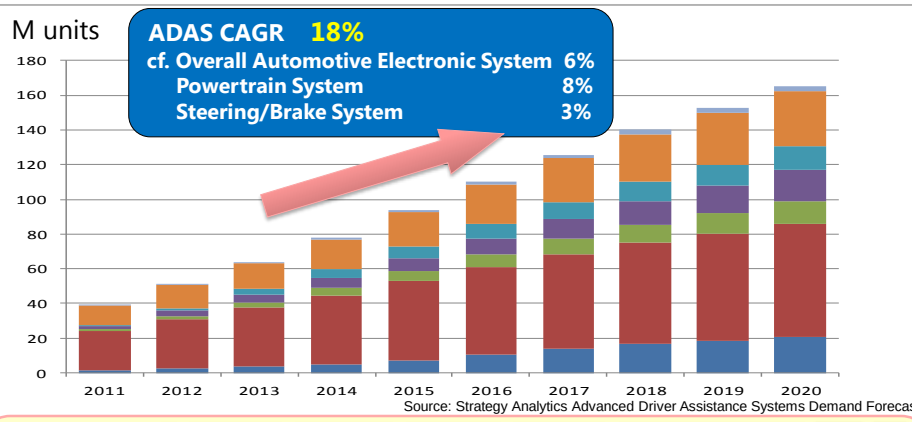
1.9 million

Source: World Health Organization (WHO) Projections of mortality and causes of death, 2015 and 2030

- More than **1 million** people die in traffic accidents every year
- **50 million** people are injured in non-fatal accidents

How can we decrease Road Injuries?

ADAS(Advanced Driving Assistant System) Market Growth



Source: Strategy Analytics Advanced Driver Assistance Systems Demand Forecast

2004	2013	2014	2016	2017	2018
Euro NCAP Requirements	Lane Departure Warning Forward Collision Warning		Pedestrian Detection (Daytime)	Pedestrian Detection (Daytime & Night)	Cyclists Detection (Daytime & Night)

NCAP: New Car Assessment Programme

Roadmap of Image Recognition SoCs

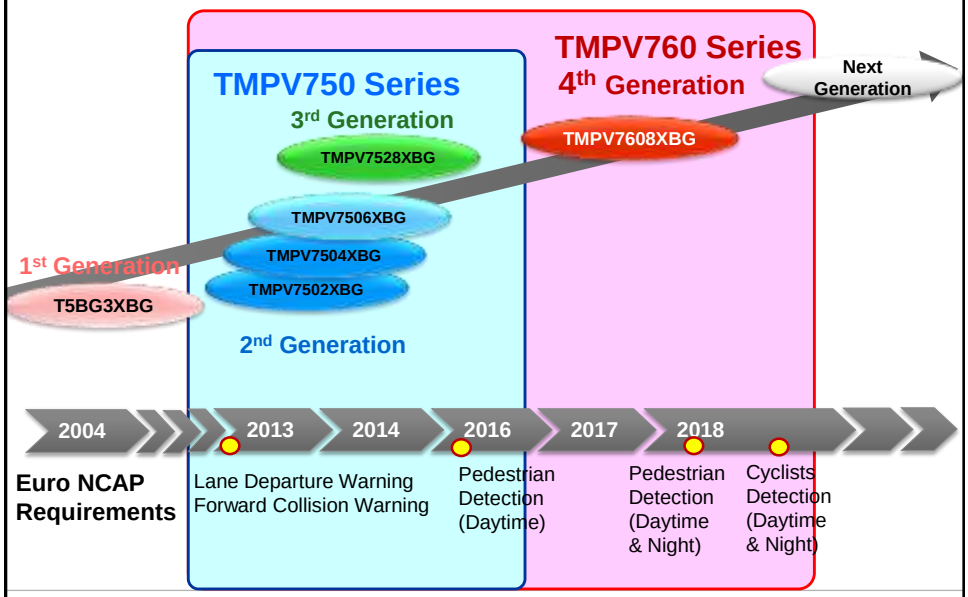
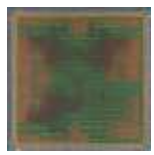


Image Recognition SoCs

1st Gen. T5BG3XBG [CICC 2004]



- **0.13µm CMOS**
- **1W@1.5V**
- **Core x3 + HWA x1**

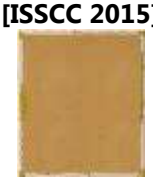
Single application (Lane Detection Forward Collision Warning, or Night Vision)

2nd Gen. TMPV7506XBG [ISSCC 2012]

- **40nm CMOS**
- **1W@1.1V**
- **Core x4 + HWA x6**
- **464GOPS**
- **617GOPS/W**

4 apps. execution including Pedestrian Detection(PD)

4th Gen. TMPV7608XBG [ISSCC 2015]



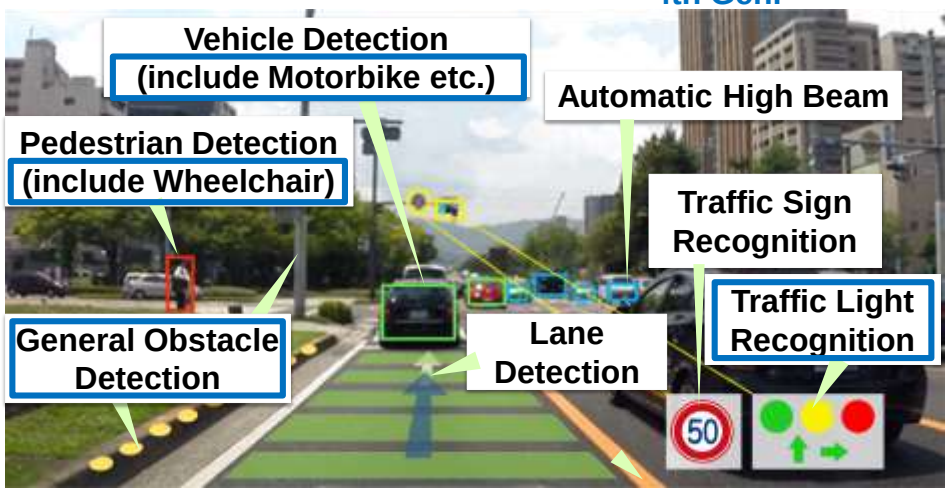
- **40nm CMOS**
- **3W@1.1V**
- **Core x8 + HWA x14**
- **1900GOPS**
- **564GOPS/W**

8 apps. execution including PD at night-time

Multiple ADAS Applications

4th Gen.

New features of 4th Gen.



Design Concept of Image Recognition SoCs

Requirements:

- High performance with low power consumption
- High accuracy of object recognition

Heterogeneous Multi-core Architecture

- Energy efficient multi-core
- Hardware accelerators
  - Performance bottlenecks and frequently used tasks
  - High accurate image recognition features

Adopted "Highly parallelized" approach rather than "High clock frequency" approach

Why Heterogeneous Multi-Core Architecture?

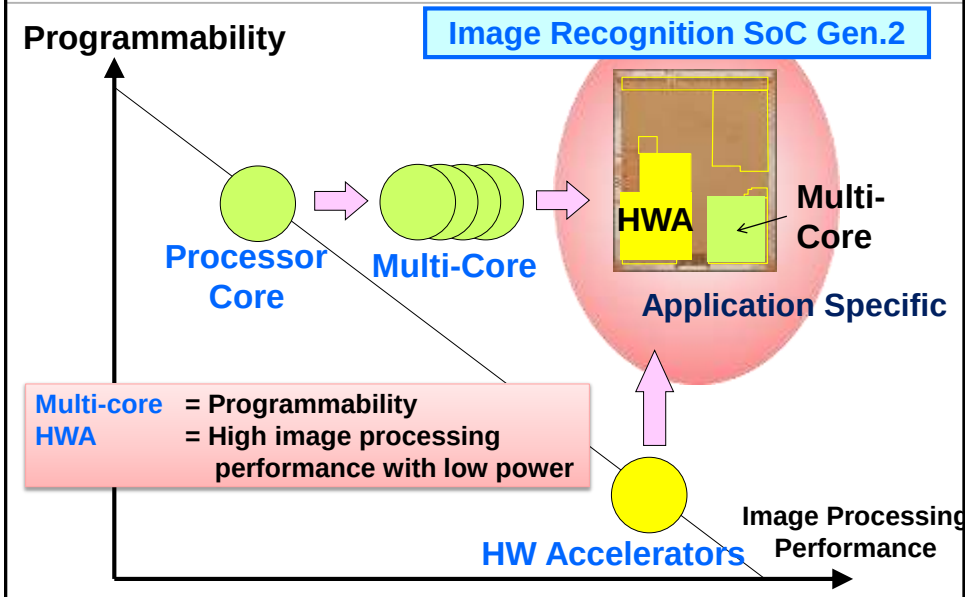
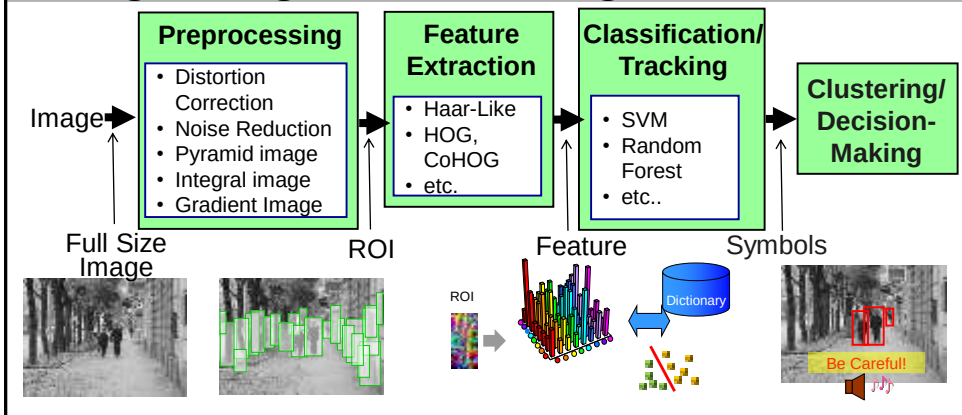
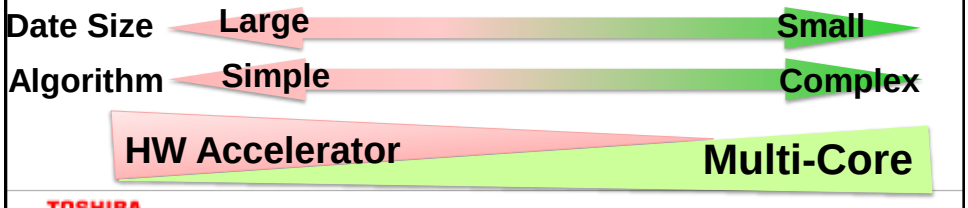
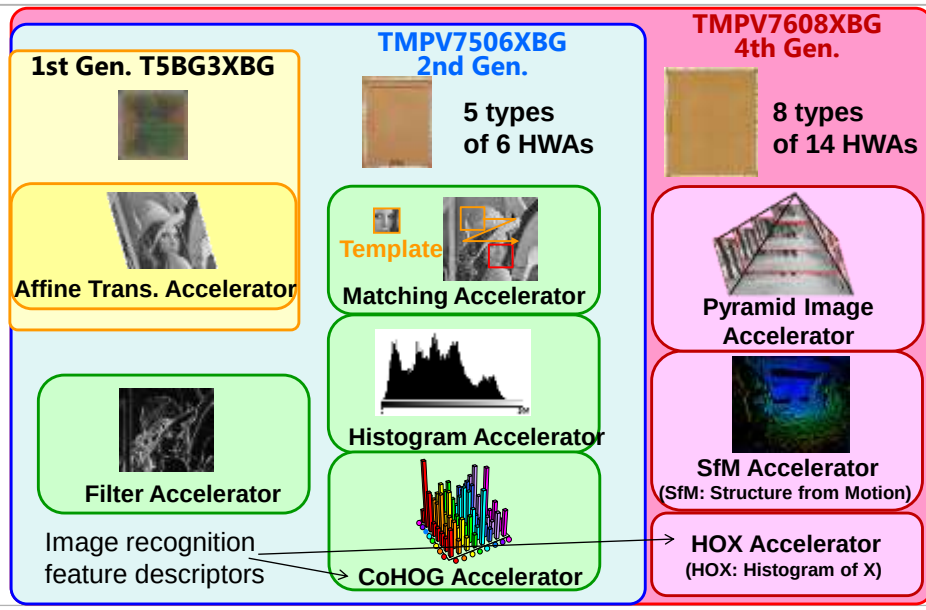


Image Recognition Processing

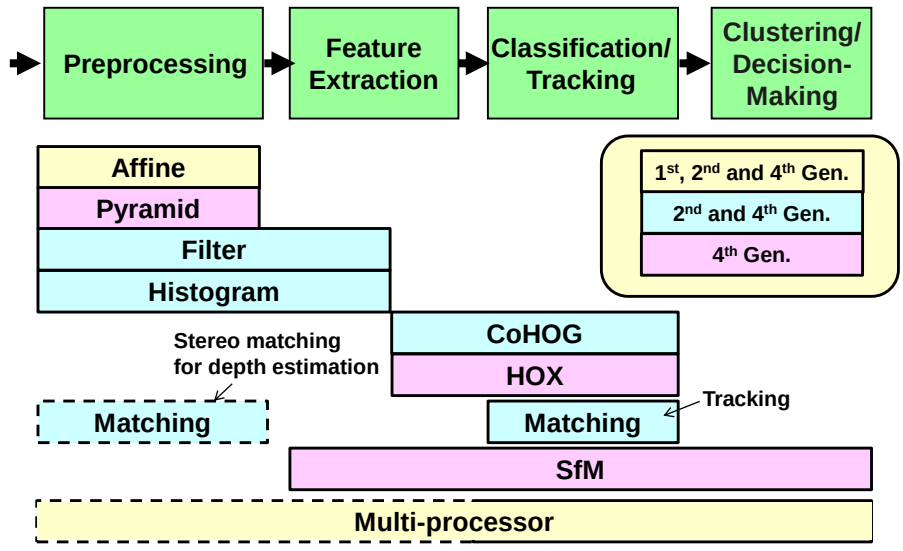




Hardware Accelerators

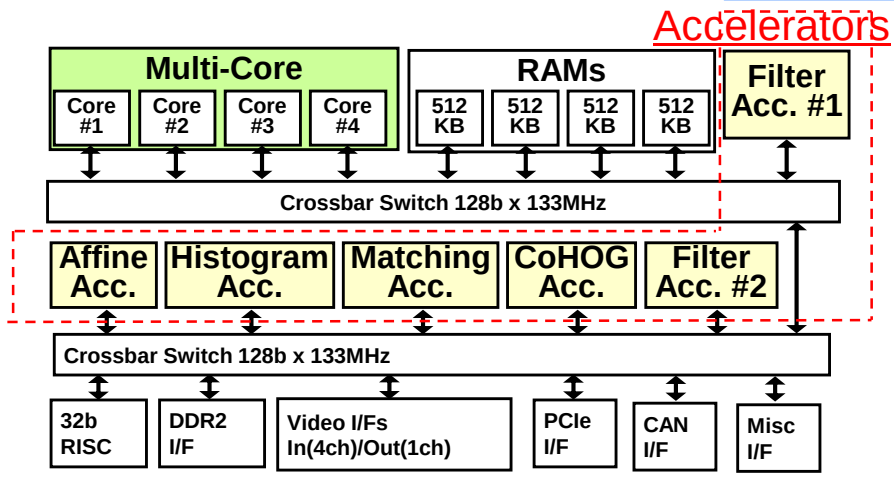


Use of HWA in Image Recognition Processing



Block Diagram of TMPV7506XBG

2nd Gen.



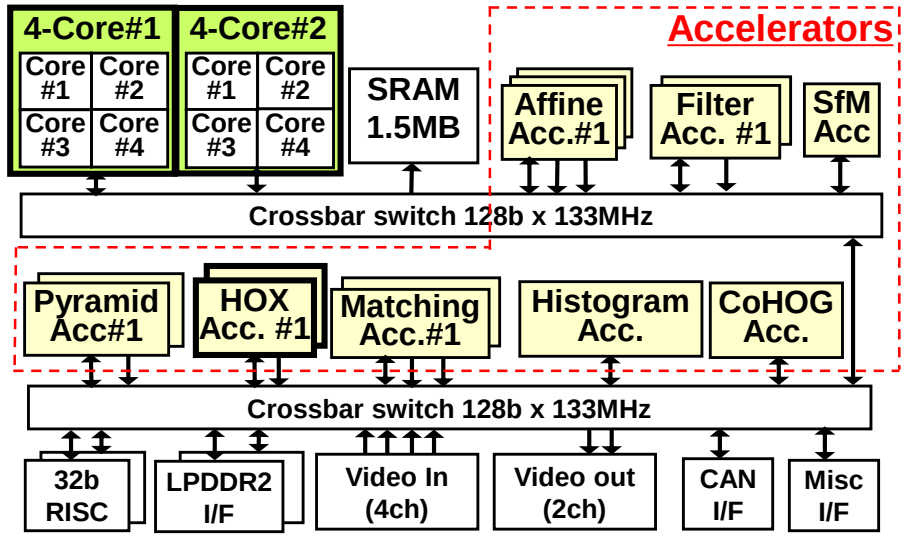
Memory Bandwidth

DDR2: Peak 2GB/sec (32b x 532MHz)

On chip RAMs: 2GB/sec x 4ch. (128b x 133MHz x 4ch.)

Block Diagram of TMPV7608XBG

4th Gen.

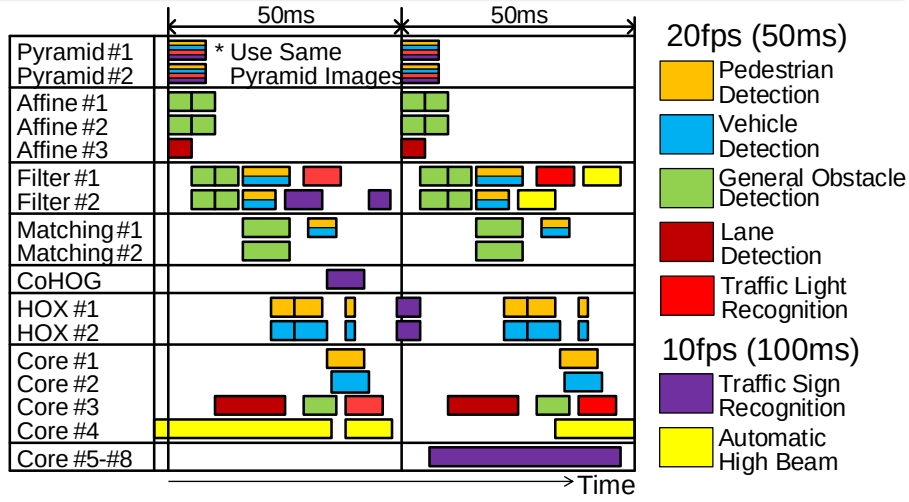


Memory Bandwidth: LPDDR2 64-bit x 2ch: 12.8GB/sec

Execution Flow of 7 Applications

4th Gen.

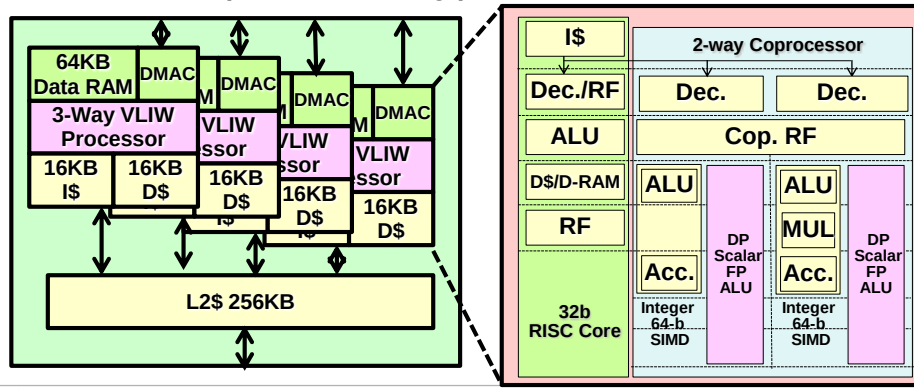
- **Design SoC architecture**
  - ✓ **Number of accelerators and cores, memory BW, and so on**



4-Core Processor Clusters

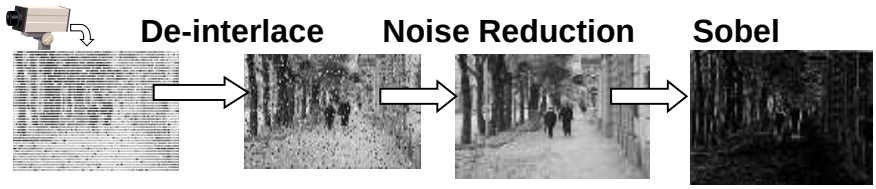
4th Gen.

- **Each cluster has four 3-way VLIW processors**
  - **3-way VLIW: 32b RISC core + 2-way coprocessor**
  - **Coprocessor supports**
    - **Integer 8/4/2-parallel 8/16/32-bit SIMD instructions**
    - **Double precision floating-point instructions**



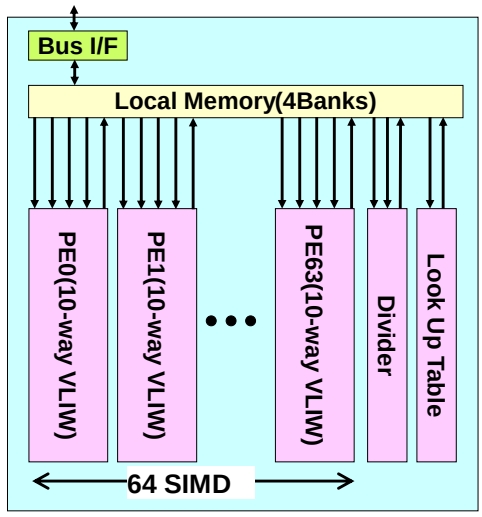
Filter Accelerator

- **Function**
  - **Execution of various filter tasks**
- **Many computations**
  - **About 100 operations / pixel**
  - **Need to process whole image**



Various image filters are used for pre-processing

Implementation of the Filter Accelerator

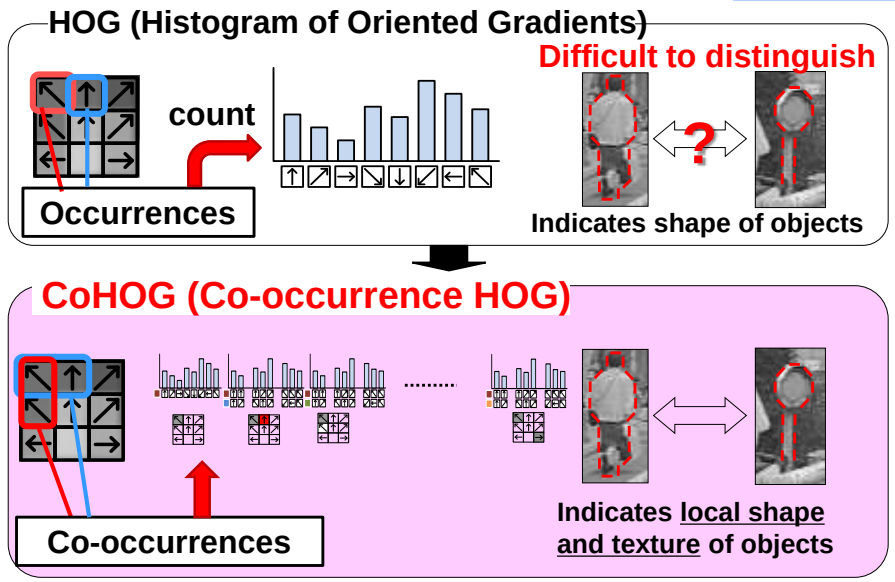


- SIMD architecture
  - 64 Processing Elements (PEs)
  - Process 64 pixels simultaneously
- PE
  - 10-way VLIW
  - Up to 9 operands from local memory, vector registers, and table registers

- 230.4GOPS(640 ops. @180MHz x 2 accelerators)
- Example: 7x7 Gaussian filter, VGA size : 1.1msec (by one accelerator)

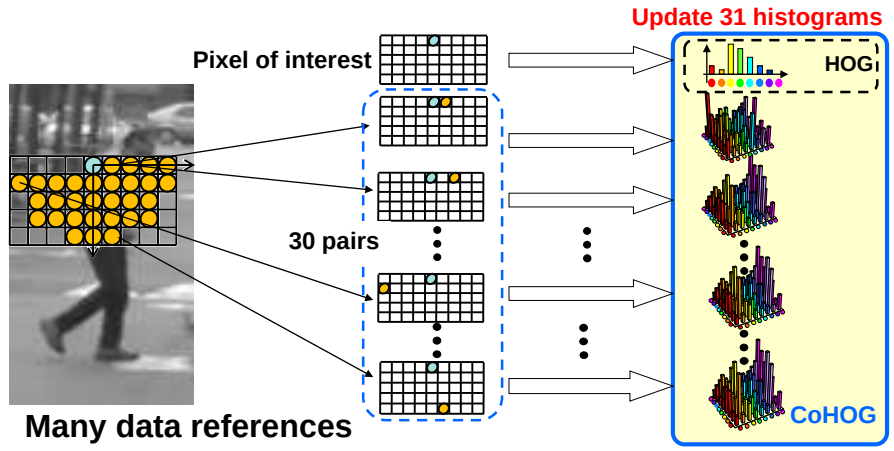
CoHOG Feature

2nd Gen.



Calculation of CoHOG Feature

2nd Gen.



- Many data references
  - 31 references / pixel ⟺ (cf. 1 pixel @HOG)
- Many calculations
  - Update 31 histograms for each pixel ⟺ (cf. 1 hist. @HOG)

Over 3GHz processor is required!

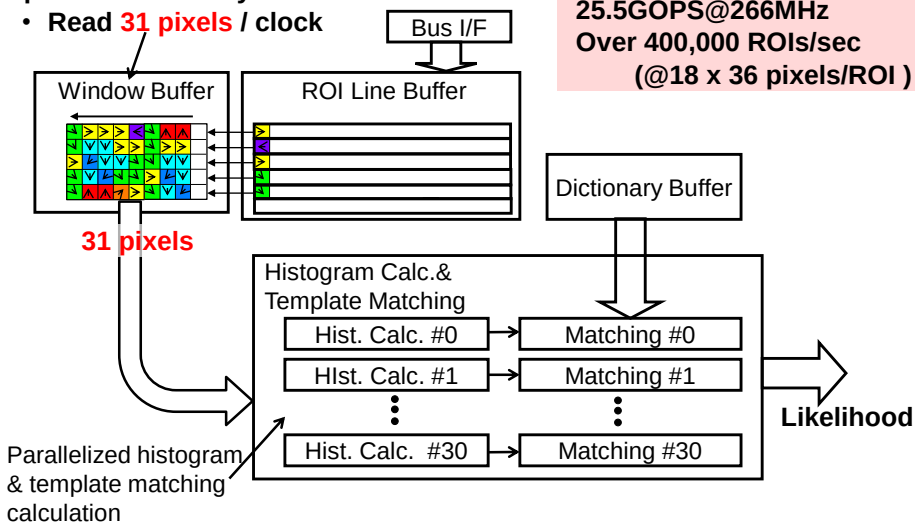
Implementation of CoHOG Accelerator

2nd Gen.

Optimized for many data references

- **Read 31 pixels / clock**

25.5GOPS@266MHz
Over 400,000 ROIs/sec
(@18 x 36 pixels/ROI)



Improvement by Color-Based Feature

4th Gen.

Euro NCAP will adopt Automatic Emergency Braking (AEB) test (with pedestrian and cyclist detection) in darkness in 2018.

- **Improved recognition accuracy using a new image feature**
  - Color-based image features to describe shape and texture
  - Extension to CoHOG feature

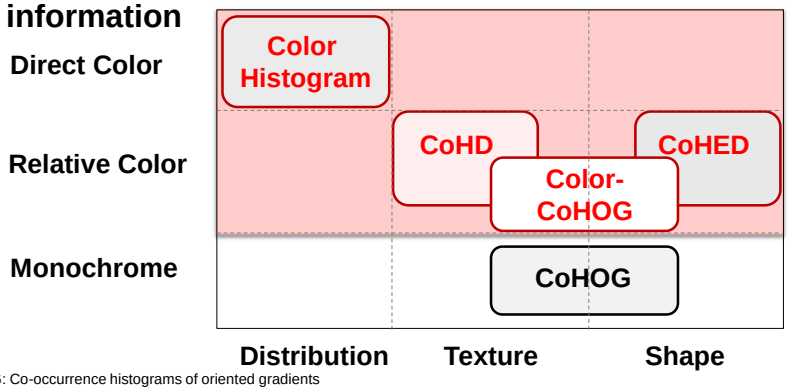
Background object
is similar luminance

Color information can tell us boundary of pedestrians

Four Color-Based Feature Descriptors*

4th Gen.

- Four feature descriptors work complementarily
  - Color Histogram, CoHD, Color-CoHOG, and CoHED
- They are designed to capture different types of information



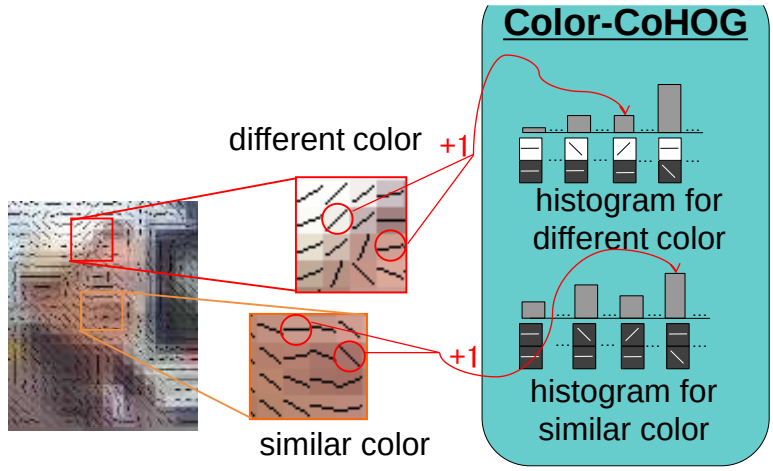
CoHOG: Co-occurrence histograms of oriented gradients
CoHED: Co-occurrence histograms of pairs of edge orientations and color differences
CoHD: Co-occurrence histograms of color differences

*) Satoshi Ito and Susumu Kubota, "Object Classification Using Heterogeneous Co-occurrence Features," Computer Vision – ECCV 2010, Lecture Notes in Computer Science Volume 6315, 2010, pp 701-714

Color-CoHOG : Color Version of CoHOG

4th Gen.

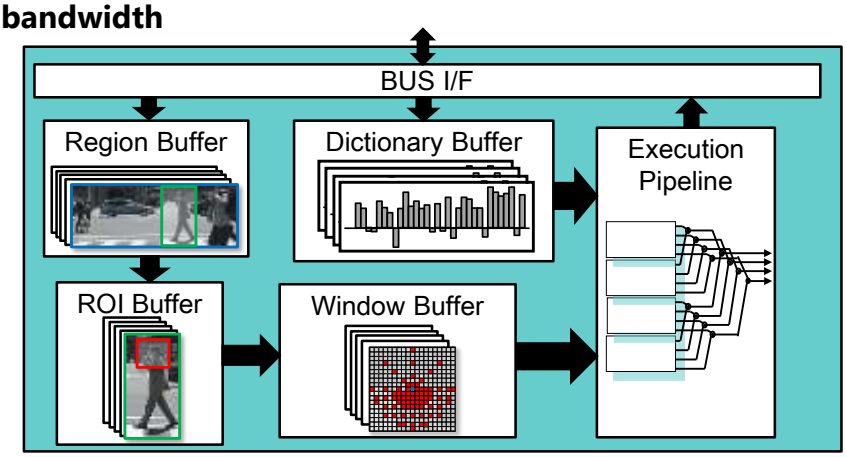
- Make two co-occurrence histograms of edge orientation
  - Similar color and different color



HOX (Histogram of X) Accelerator

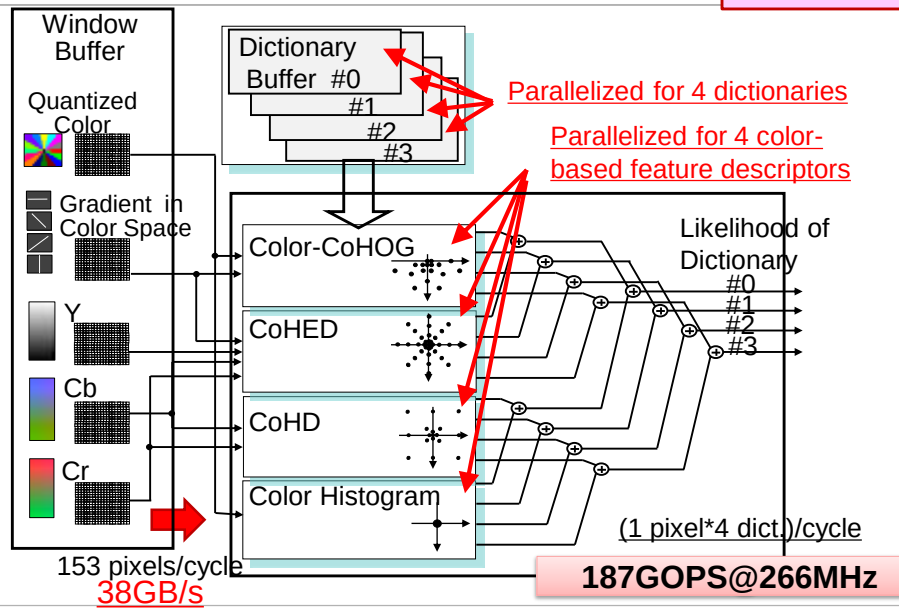
4th Gen.

- **Support both CoHOG and four color-based features (Color Histogram, CoHD, Color-CoHOG, and CoHED)**
- **Three-level hierarchical image buffer to reduce memory bandwidth**



Execution Unit of HOX Accelerator

4th Gen.



Performance of HOX Accelerator

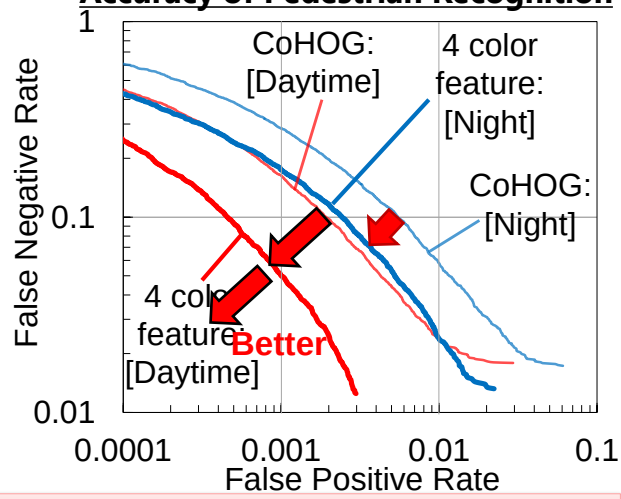
4th Gen.

[Daytime dataset]

[Night-time dataset]

* Original dataset

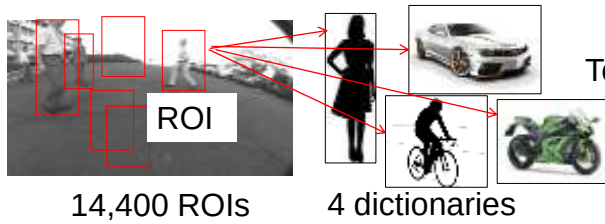
Accuracy of Pedestrian Recognition



Accuracy **at night** using HOX accelerator is almost the same as **at daytime** using CoHOG accelerator

Performance of HOX Accelerator

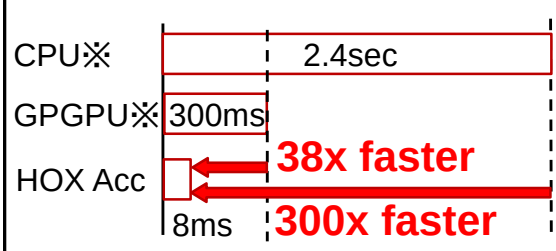
4th Gen.



14,400 ROIs

4 dictionaries

Total: 57,600 likelihoods

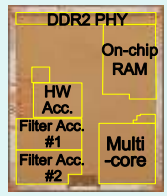


※ Intel® Core™ i7-2600k 3.4GHz (1 thread)

※ NVIDIA® GTX550Ti
192 CUDA Cores,
900MHz@40nm
with our optimized code

Chip Micrograph and Features

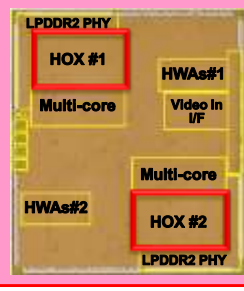
2nd Gen. TMPV7506XBG



Process	40nm CMOS LP		
Chip Size	44.54mm²		
Peak Performance			
Multi-core	266MHz	46.8GOPS	Total 464GOPS
Affine	266MHz	10.6GOPS	
CoHOG	266MHz	25.5GOPS	
Filter (x2)	180MHz	230.4GOPS	
Histogram	266MHz	5.3GOPS	
Matching	266MHz	145.2GOPS	
Performance /W	617GOPS/W		

0.87W @Typ., PD

4th Gen. TMPV7608XBG



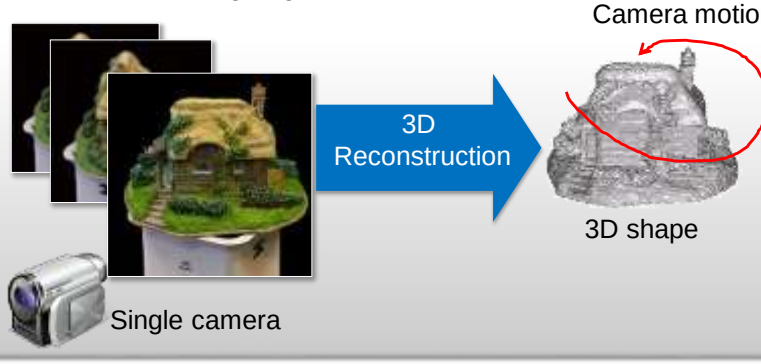
Process	40nm CMOS LP		
Chip Size	105.6mm² (9.60mmx11.0mm)		
Peak Performance			
Multi-core (x2)	266MHz	93.6GOPS	Total 1900GOPS
Affine(x3)	266MHz	134.9GOPS	
Pyramid (x2)	266MHz	352.2GOPS	
CoHOG	266MHz	25.5GOPS	
HOX (x2)	266MHz	373.5GOPS	
Filter (x2)	180MHz	230.4GOPS	
Histogram	266MHz	5.3GOPS	
Matching (x2)	266MHz	594.6GOPS	
SfM	266MHz	90.0GOPS	
Performance /W	564GOPS/W		

0.9W @Typ., PD+VD+LD

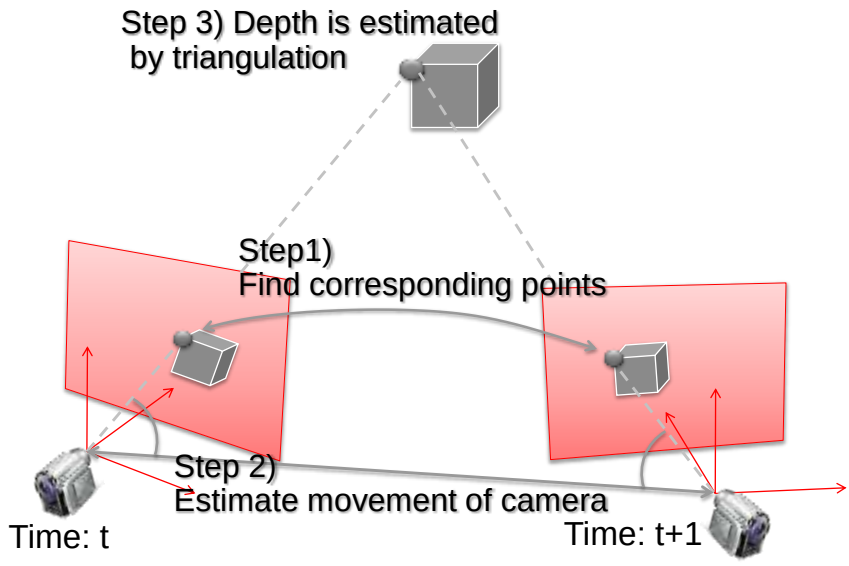
3D Reconstruction (SfM: Structure from Motion) 4th Gen.

TMPV7608XBG (4th generation SoC) supports 3D reconstruction using a "single" camera for general obstacle detection

Multiple images are taken from different viewing angles



Principle of SfM: Triangulation



Conclusion

- **Heterogeneous multi-core SoCs dedicated for image recognition**
  - **High performance with low power consumption**
    - **Energy efficient multi-core**
    - **Highly parallelized hardware accelerators**
  - **High accurate recognition**
    - **CoHOG and four color-based features (Color Histogram, CoHD, Color-CoHOG, and CoHED)**
    - **Accurate detection for pedestrian even at night**
- **For the future Autonomous Driving**