Nanophotonics for low-latency optical pass gate logic circuits

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Ultra low-latency optical computing

Target

Light-speed processor

・Eliminating latency bottleneck

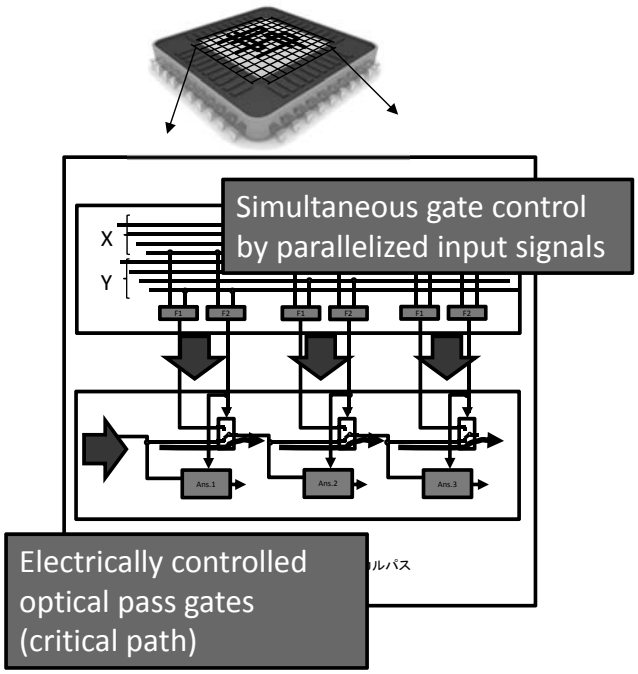
・New optical computing technology

Approach

Replacement of critical path with photonic devices.

Calculation simply by propagating the light through the electrically controlled optical pass gates.

Nanophotonics for shortening the critical path

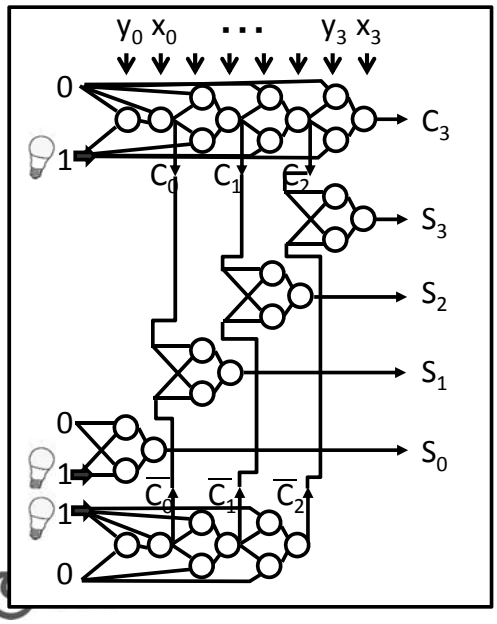


Critical path = signal route determining calculation time

Binary Decision Diagram (BDD) based photonic circuit

Simplified tree structure for 4-bit adder

Hokkaido Univ., T. Asai et al.
IEICE Electronics (1), 386 (2000)



Merits

(1) Instantaneous construction of output path via simultaneous gate control [ps]

(2) Calculation simply by propagating the light through the pathway.

(3) Calculation with light propagation speed! (no CR-limitation)

Demerits

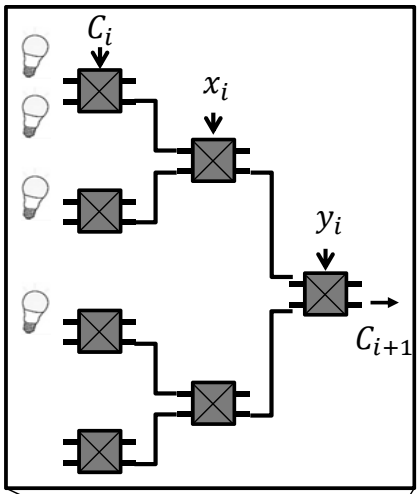
(1) Complicated circuit configuration for optics (many branches, crossing points).

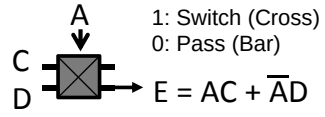
BDD does NOT necessarily optimize the circuit.

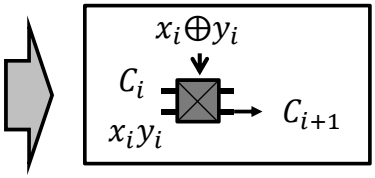
Optically suitable tree reconstruction

Lookup table of full adder

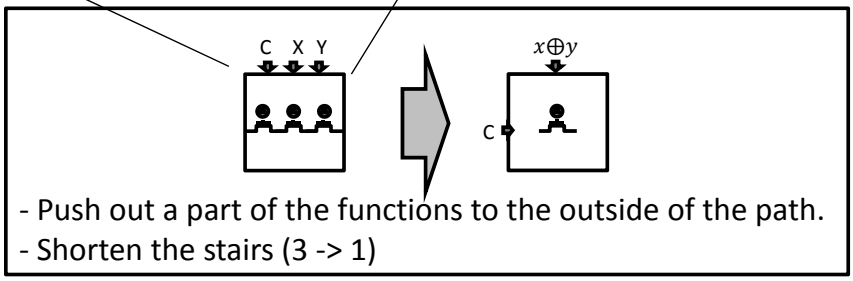
C_i	X_i	Y_i	C_{i+1}
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0







$$C_{i+1} = (x_i \oplus y_i)C_i + \overline{(x_i \oplus y_i)}x_i y_i$$



- Push out a part of the functions to the outside of the path.
- Shorten the stairs (3 -> 1)

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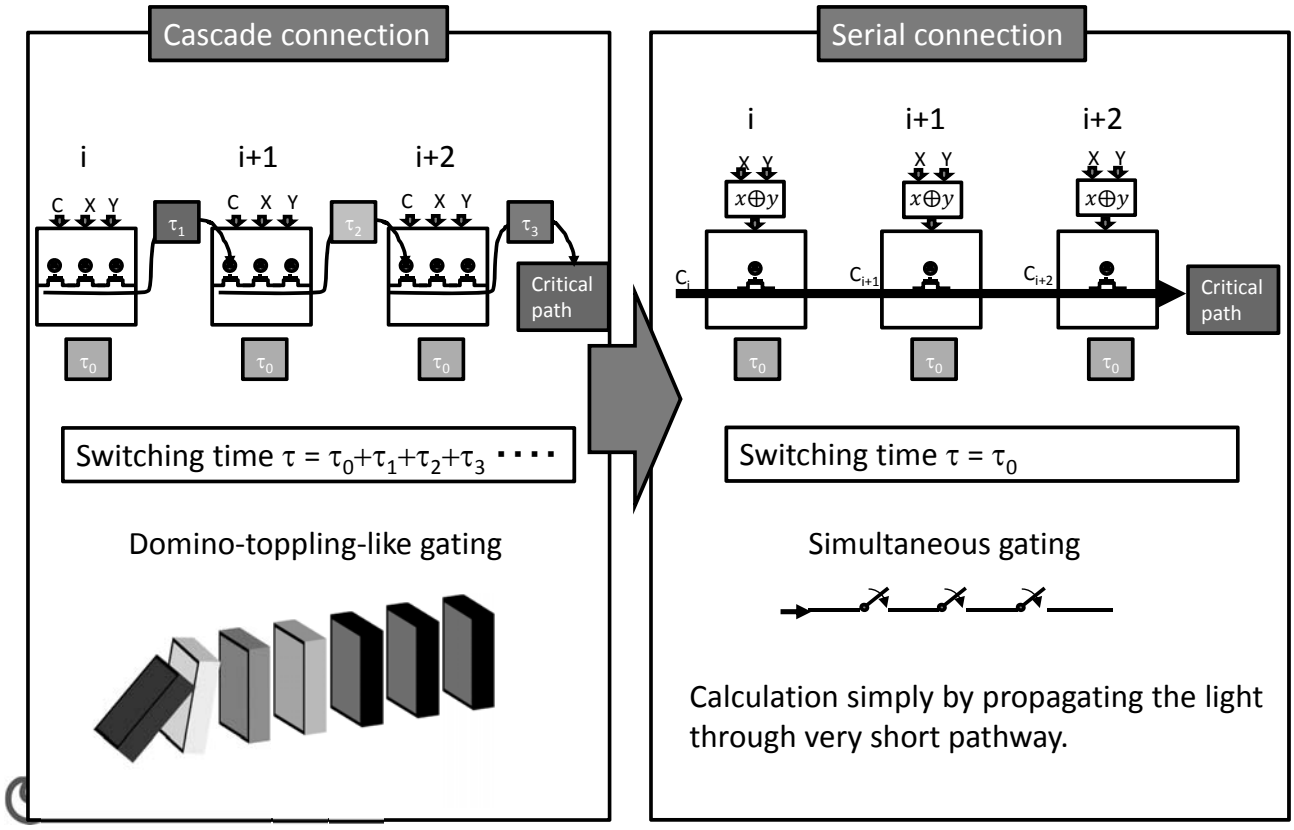
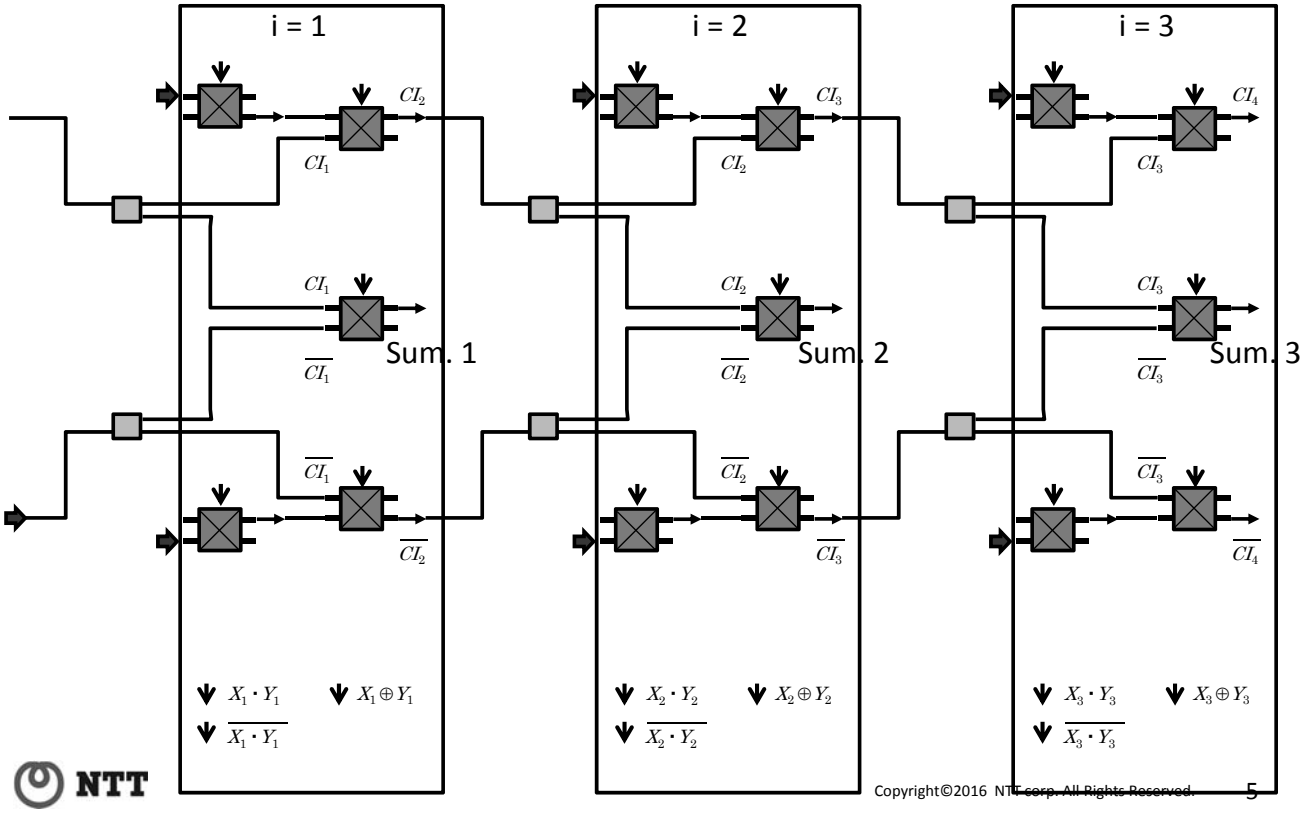
Serial tree connection

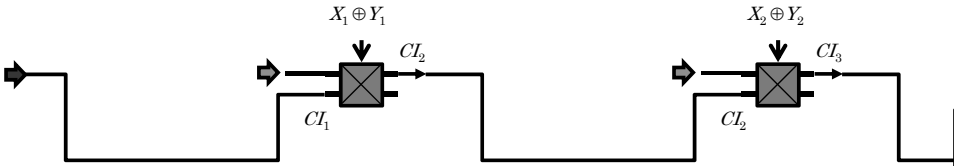


New optical adder (X+Y)

Proposed by Dr. Ishihara, Kyoto Univ.

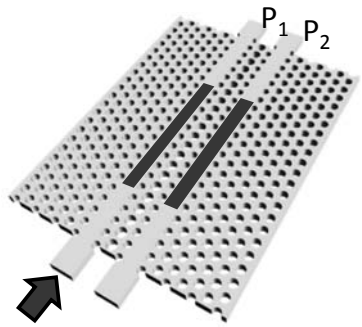


Calculation speed



Calculation time = signal propagation time in critical path

If we can realize 10 ~ 100 μm length optical pass gate,



Propagation speed
~ 100 μm/ps

τ_{path} = 0.1 ~ 1 ps

Latency of 32-bit adder
Optical pass gate
τ_{switch}= 10 ps τ_{path}= 0.1 x 32 = 3.2 ps τ_{total}= 13.2 ps
CMOS(normal type)
τ_{total}= 1400 ps (current) → 560 ps (future)
CMOS (advanced)
τ_{total}= 400 ps (current) → 160 ps (future)

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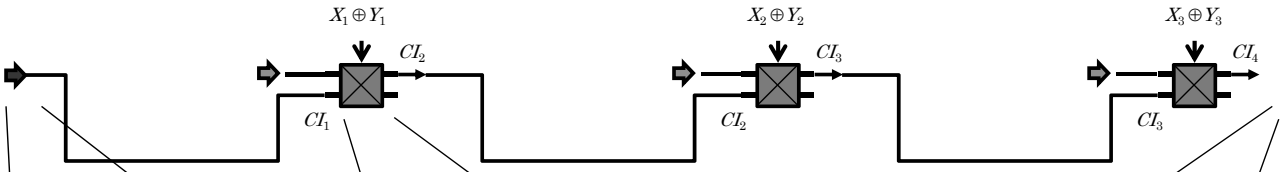
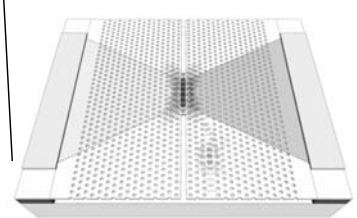
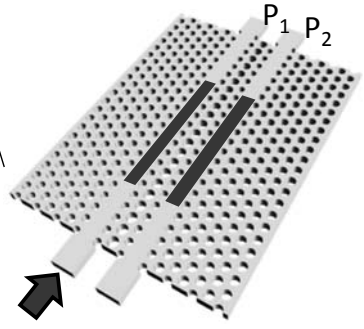
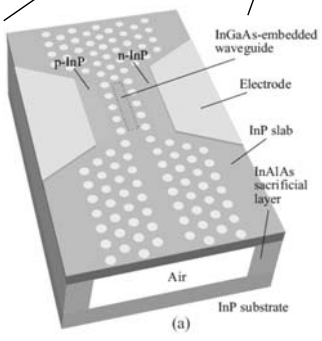
Building blocks for optical calculation



Calculation time = signal propagation time in Critical path







Ultralow-threshold laser

Electrically driven ultrashort 2x2 switch

High-efficiency O/E conversion w/o electrical amplifier

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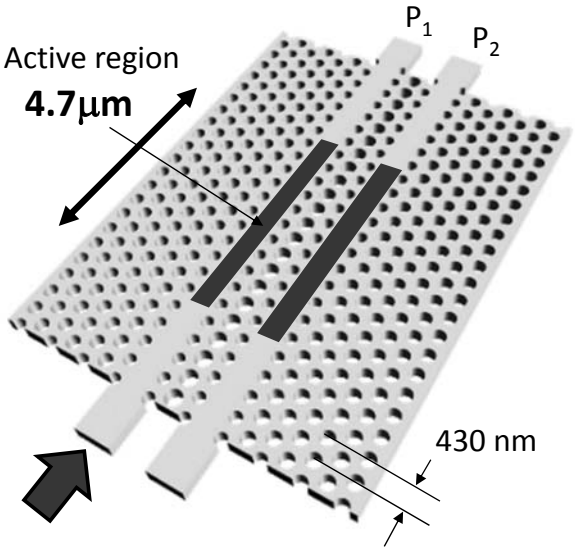
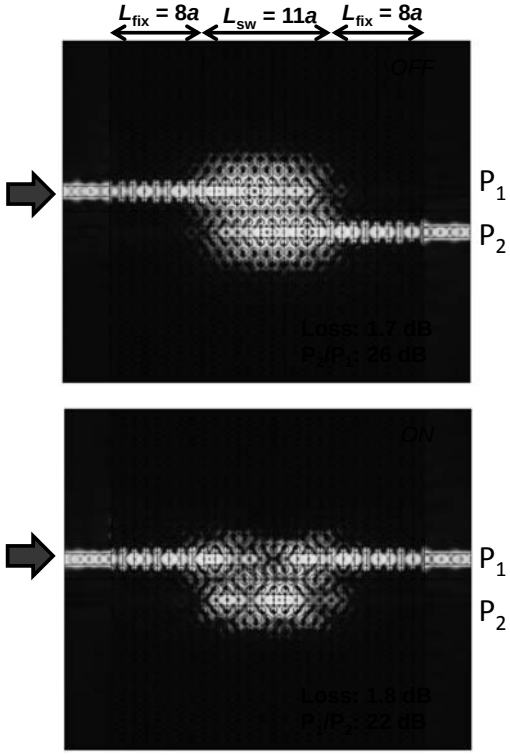
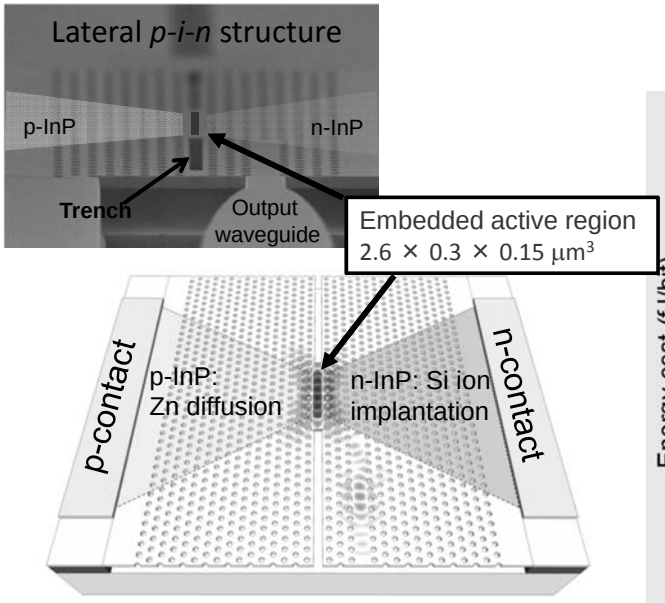
Electrically driven ultrashort 2x2 switch



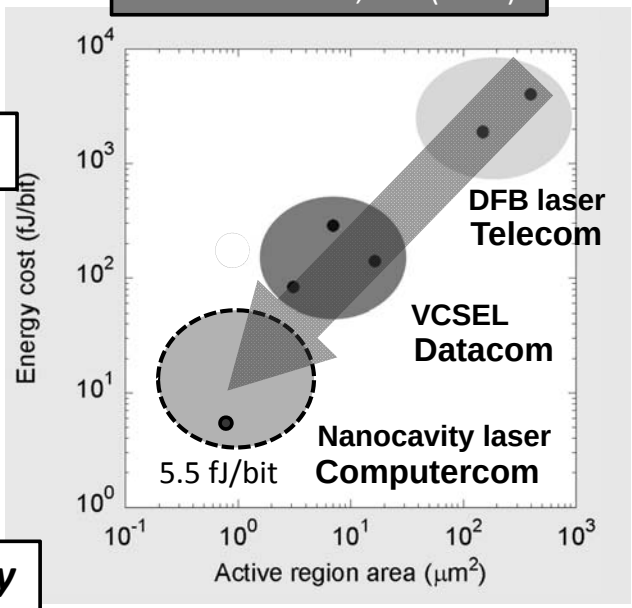


L_{tot} = 11.6 μm, τ_{path} ~ 0.44 ps

Ultralow-threshold laser



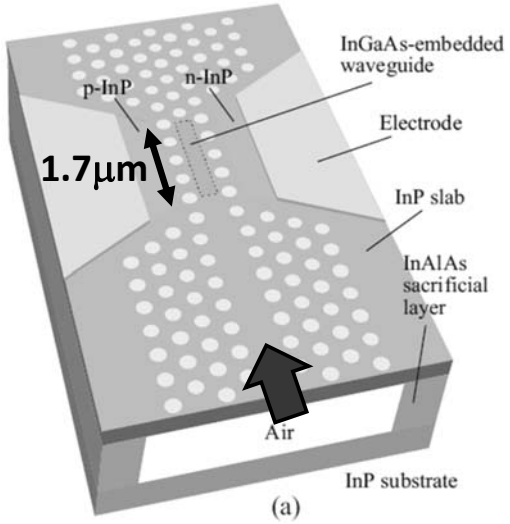
NTT, Takeda et al., Nature Photon. 7, 569 (2013)

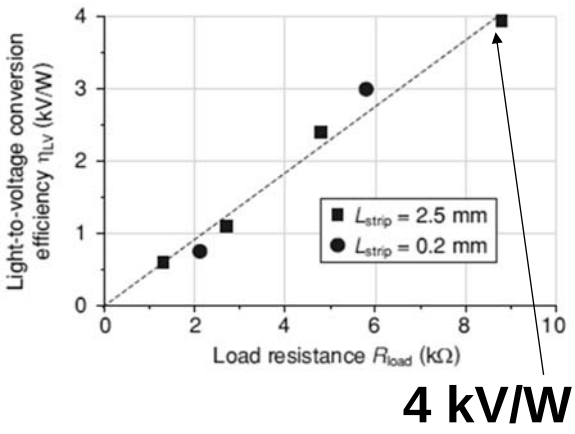


World's lowest threshold for any type of laser diode

High-efficiency light-to-voltage conversion w/o amplifier

Nozaki et al., Optica 3, 483 (2016)





4 kV/W

C_{theory} = 0.3~0.5 fF
28.5 GHz

Best candidate for receiver-less photodetector

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Summary

☐ Pass-transistor-based photonic logic circuit
- Only passes light through many gates.
- Creates complex logic functionalities.
- Enables light-speed computation!

☐ Requirements for photonic device
- Short gates
  Path delay is determined by light propagation speed.
- Highly effective E/O, O/E and O/E/O conversion

⇩

Nanophotonic device technology

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