ENERGY EFFICIENT SOCS
A REINFORCEMENT LEARNING APPROACH

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OVERVIEW

1. State-of-the-art and challenges
2. Reinforcement learning formulation of the energy minimisation problem
3. Some experimental results
4. Conclusions and perspectives
    - FDSOI: DFVS vs DBB

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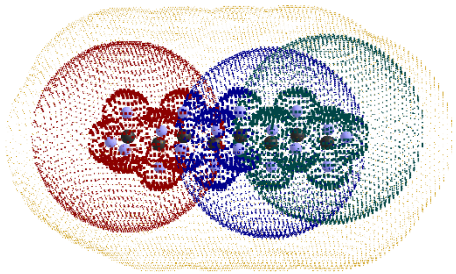
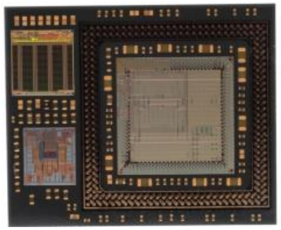
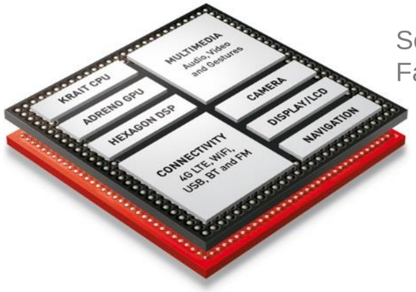
SOC ENERGY MANAGEMENT CONTEXT

Source: Urban Farming News





Source: NXP



Source: Fairphone

Source: HPE

- **Problem: design a *manager* (power governor, run-time,…) that:**
  - Minimise energy under performance constraints
  - Optimize energy efficiency under power and performance constraints
  - Mitigate heating
  - Maximise performance under power capping
  - …
- **Actuators**
  - Hardware units operating point (mode idle, mode sleep, DVFS, …)
  - Load balancing of the application software on the hardware units

STATE-OF-THE-ART: 2 MAIN VIEWS

Many-core/dark silicon	Heterogeneous processors (CPU/GPU)
Assumptions	
• One can compute the power • The exactly execution profile is known (start/end/execution/idle times, …)	• One can measure the power • Only the values of performance counters are known

$$E_i(V_i, V_{ti}) = R_i C_i V_i^2 + T_i k_i V_i e^{\left(-\frac{V_t}{S_t}\right)}$$

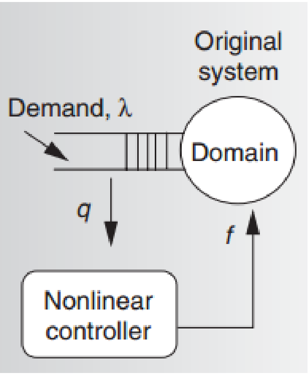
$$\overline{q}'_k = \bar{q}_{k-1} + \frac{T}{2}\left(\bar{\lambda}_{k-1} - \bar{\mu}_{k-1}\right)$$

$$\bar{q}_k = \bar{q}_{k-1} + \left(\bar{\lambda}_{k-1} - \bar{\mu}_{k-1}\right)T$$

$$e_k = \overline{q}'_k - q_{\mathrm{ref}}$$

$$\bar{\mu}_k = \bar{\mu}_{k-1} + K_I e_k + K_P\left(e_k - e_{k-1}\right)$$

$$f_k = \frac{\bar{C}_2 \bar{\mu}_k}{1 - \bar{t}_1 \bar{\mu}_k}$$



Counters	
CSBusy	HSALUTexRatio
CSTime	HSTexBusy
DepthStencilTestBusy	HSTexInstCount
DSBusy	HSPatches
DSTime	HSSALUBusy
GPUTime	HSSALUInstCount
GPUBusy	HSVALUBusy
GSBusy	HSVALUInstCount
GSTime	GSALUBusy
HSBusy	GSALUEfficiency
HSTime	GSALUInstCount
InterpBusy	GSALUTexRatio
PrimitiveAssemblyBusy	GSExportPct
PSBusy	GSPrimsIn
PSTime	GSSALUBusy
ShaderBusy	GSSALUInstCount
ShaderBusyCS	GSTexBusy
ShaderBusyDS	GSTexInstCount
ShaderBusyGS	GSVALUBusy
ShaderBusyHS	GSVALUInstCount
ShaderBusyPS	GSVerticesOut
ShaderBusyVS	ClippedPrims
TessellatorBusy	CulledPrims
TexUnitBusy	PAPixelsPerTriangle
VSBusy	PAStalledOnRasterizer
VSTime	PrimitivesIn

…

STATE-OF-THE-ART: 2 MAIN VIEWS

Many-core/dark silicon	**Heterogeneous processors (CPU/GPU)**
Assumptions	
• One can compute the power • The exactly execution profile is known (start/end/frame times, …)	• One can measure the power • Only the values of performance counters are known
Main challenges addressed	
• Models to fit application dynamics and methods to solve for, e.g., frequency	• Load balancing and metrics for application performance power ↔ consumption
Approaches	
• Control theory: simple/complex controllers [Wu04,Garg10,David12,Bartolini12, Bogdan13, Rahmani15 ..] • Learning [Tan09,Liu10,Jung10,Dhiman11,Wang11,Ye14, Das14,Triki14,Khan14,Chen15] • Theoretical proofs	• Power-performance prediction models [Dhiman09,Paul13,VRodriguez13,Pathania15] • Control theory • Simple controllers [Wang14,Dietrich14, Pathania14] • Experimental validation (large traces)
Evaluation	
• Simulation (no thorough cost investigation)	• Execution and measurements
• **Over-simplified view on software** • **Assume a too high observability of application and hardware**	• **Too low observability of application in relation to the hardware and power consumption**

CHALLENGES

- **Deal with "non-ideal" cases**
  - Application are too dynamic, exact models are hard to obtain
    - Dependent on the content of the input data
  - Application performance is not proportional to the operating point (e.g., core clock frequency)
    - Contention at shared resources, memory accesses
    - System software
      - Task scheduling, timers, interrupts
- **(Relatively) low computation cost of energy optimization**
    - No large matrix inversion
    - Small state space
    - No/limited costly functions (exponential, trigonometric)
    - No/limited least mean squares
    - …
- **Define hardware ↔ manager ↔ application interfaces for good application and power consumption visibility**
  - Power consumption should probably be the concern of the application and the operating system
  - In which parts of the application is the power consumed

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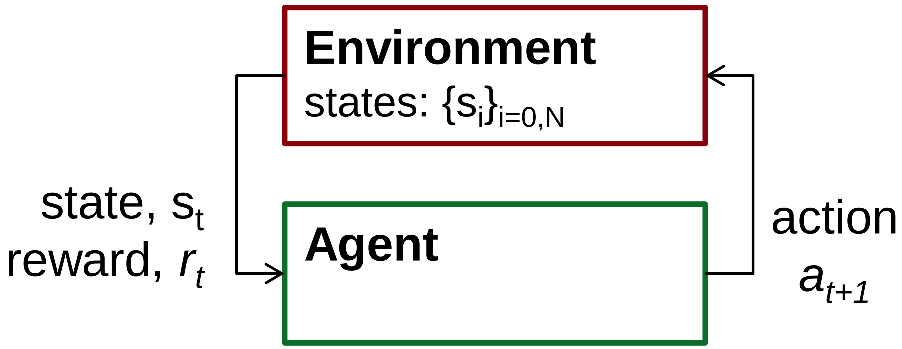
REINFORCEMENT LEARNING (RL) APPROACH

- **RL algorithm**
  - an *agent*, which aims to learn from the interaction with an *environment* (trial and error) to achieve a *goal (maximize reward)* [Sutton1998]
- **Adaptive (indirect) controller**

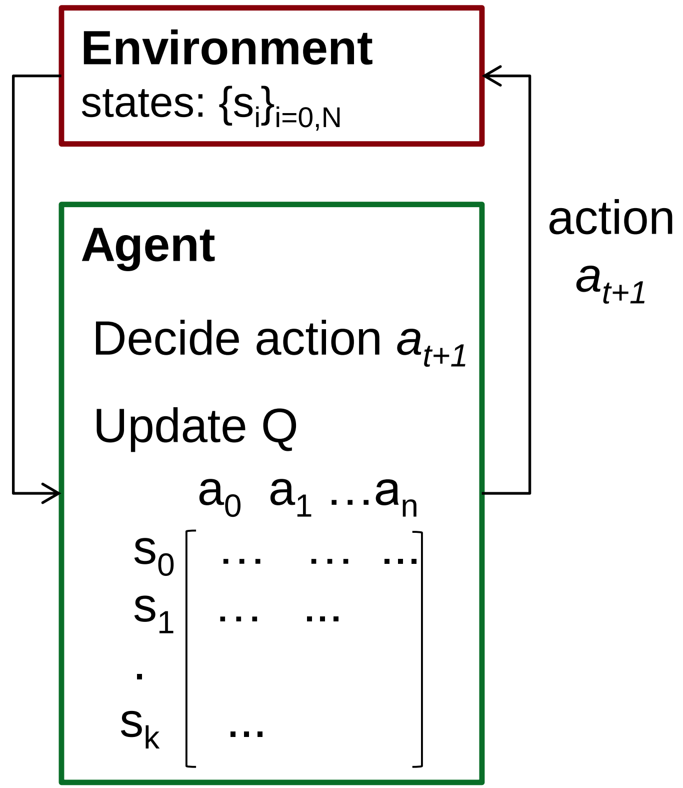


- **Advantages**
  - no model of the dynamics of the system
  - the learning is not (really) supervised
    - training happens in the same time with the optimization process (exploration/exploitation)
    - no need to know relevant use-cases
- **Disadvantages**
  - may take poor decisions during exploration
  - fully-fledged versions may have a large overhead
  - theoretical proofs (convergence speed, optimality) are valid only for discrete&finite state space, stationary, markovian systems (with some extension to semi-markovian cases)
    - however known to work ok in non-stationary, non-markovian, systems.

LOW COST Q-LEARNING

- Q-learning: the learned knowledge of the agent → a value table Q(states,actions)
  - Decided action, given s, Q → Ɛ-greedy
    - Exploitation: argmax(Q(s))
    - Exploration: some random value
  - Construct the Q table
    - Initial value of the Q table
    - Update formula:

$$Q_{t+1}(s,a) = Q_t(s,a) + \alpha \left[r_{t+1} + \gamma \max_{a'} Q_t(s',a') - Q_t(s,a) \right]$$



- Potential to learn complex behavior
  - No free lunch:
    - define the states
      - queues filling indicates application progress
    - set its parameters
      - experimental investigation
    - define a reward function
    - …

A.Molnos, S.Lesecq, J.Mottin, D.Puschini, "Investigation of Q-learning applied to DVFS management of a System-on-Chip". In 4th IFAC International Conference on Intelligent Control and Automation Sciences, ICONS (2016).

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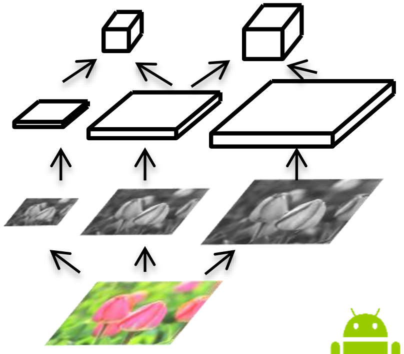
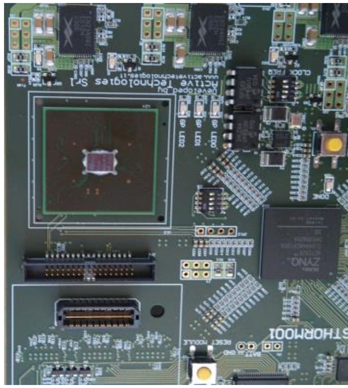
RESULTS

- Test board
  - ARM host processor and an SoC with 16 processors elements.
  - Android OS + in-house run-time
  - Application: a part of a HMAX object recognition
  - 15%-44% energy reduction wrt. state-of-the-art
  - similar number of throughput violations
  - lightweight manager: 0.7% of application time, 1KB footprint

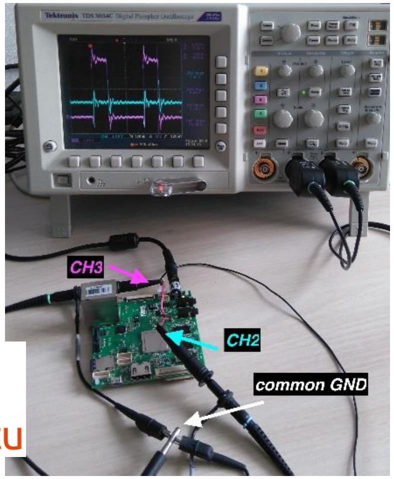




android

- Commercial board (on going work)
  - IMX6: dual-core ARM + GPU
  - Ubuntu OS, OpenCL
  - Application: obstacle detection

ubuntu



CONCLUSIONS

- **Challenges in managing energy consumption in SoCs**
  - Deal with “non-ideal” cases
  - (Relatively) low computation cost of energy optimization
  - Define hardware ↔ manager ↔ application interfaces
- **An adaptive Q-learning-based approach**
  - Model-free, potential to learn complex behaviour
- **Experiments with promising results**
  - Higher energy reductions than state-of-the-art methods addressing the same application domain.

PERSPECTIVES

- **More advanced RL methods that lead to quicker convergence and higher adaptability**
  - e.g., actor-critic, hierarchical, TD(λ), best-match → their applicability and costs should be evaluated.
  - multi-criteria optimization: temperature, aging
- **Better methods to deal with non-Markovian, non-stationary systems**
- **Deal with complex energy consumption models in future technologies**

FDSOI28 PARAMETRIC EXPLORATION

- **How to choose the best power/energy optimization strategy (DBB vs DVFS) to implement?**
- **Do we really need Dynamic Body Bias (DBB) mechanism in our future design?**

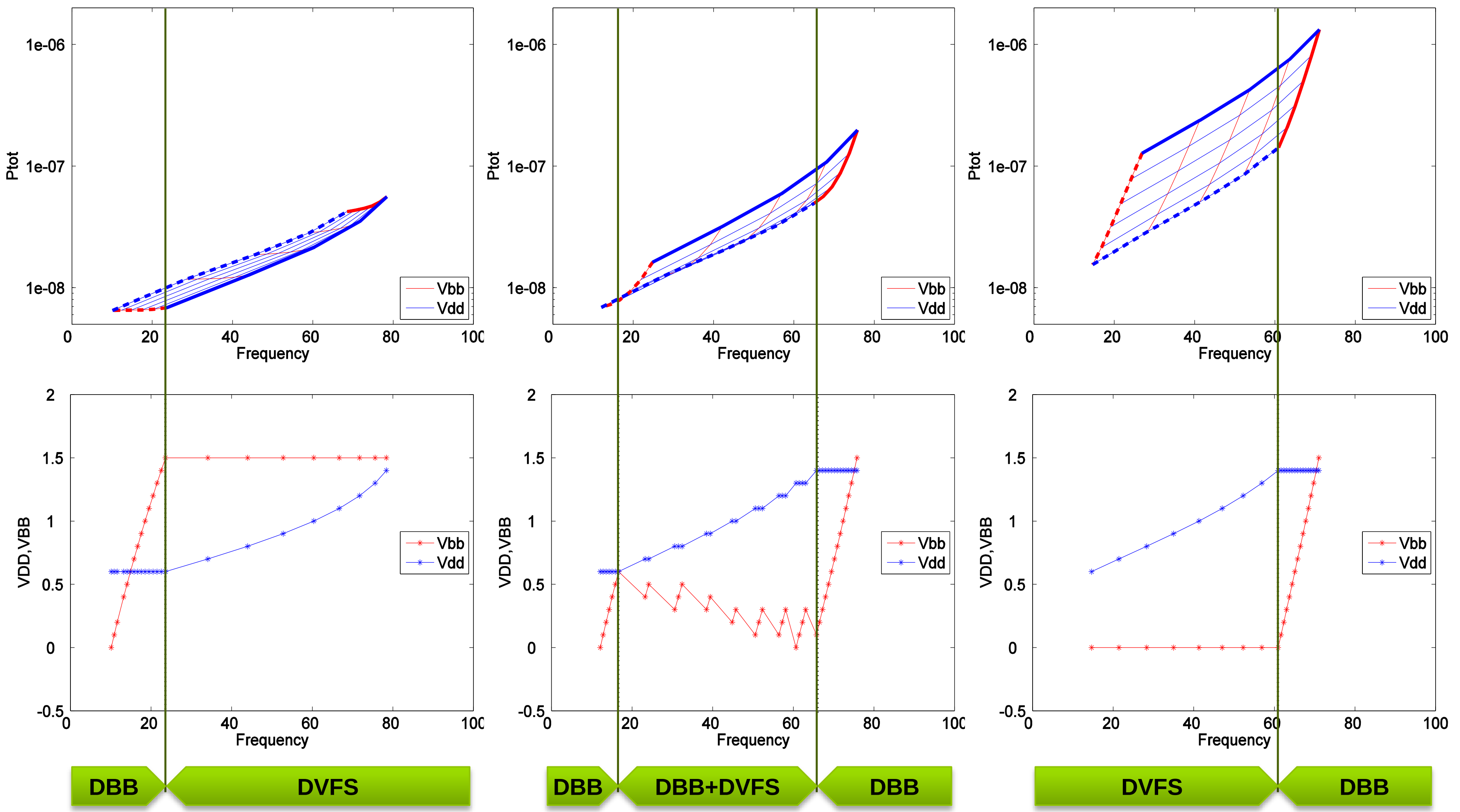
Inputs	Static Parameters		Substrate	RVT, LVT
			Poly Bias	0nm, 4nm, 10nm, 16nm
			Process Corner	SS, TT, FF
	Dynamic Parameters	User controlled	Vdd	[0.6V, 1.4V]
			Vbb in LVT	[0V, 1.5V]
			Vbb in RVT	[−1.5V, 0V]
		Operating Conditions	Temp	[−40°C, 125°C]
			Toggle Rate	[0.1%, 50%]
Measurements			Fmax	
			Iswitch	
			Ileak	

Electrical simulation of a ring oscillator

"Body Bias usage in UTBB FDSOI designs: A parametric exploration approach", D. Puschini, J. Rodas, E. Beigne, M. Altieri, S. Lesecq. Special Issue: Planar Fully-Depleted SOI technology, Solid-State Electronics Elsevier Journal, Volume 117, March 2016, Pages 138-145

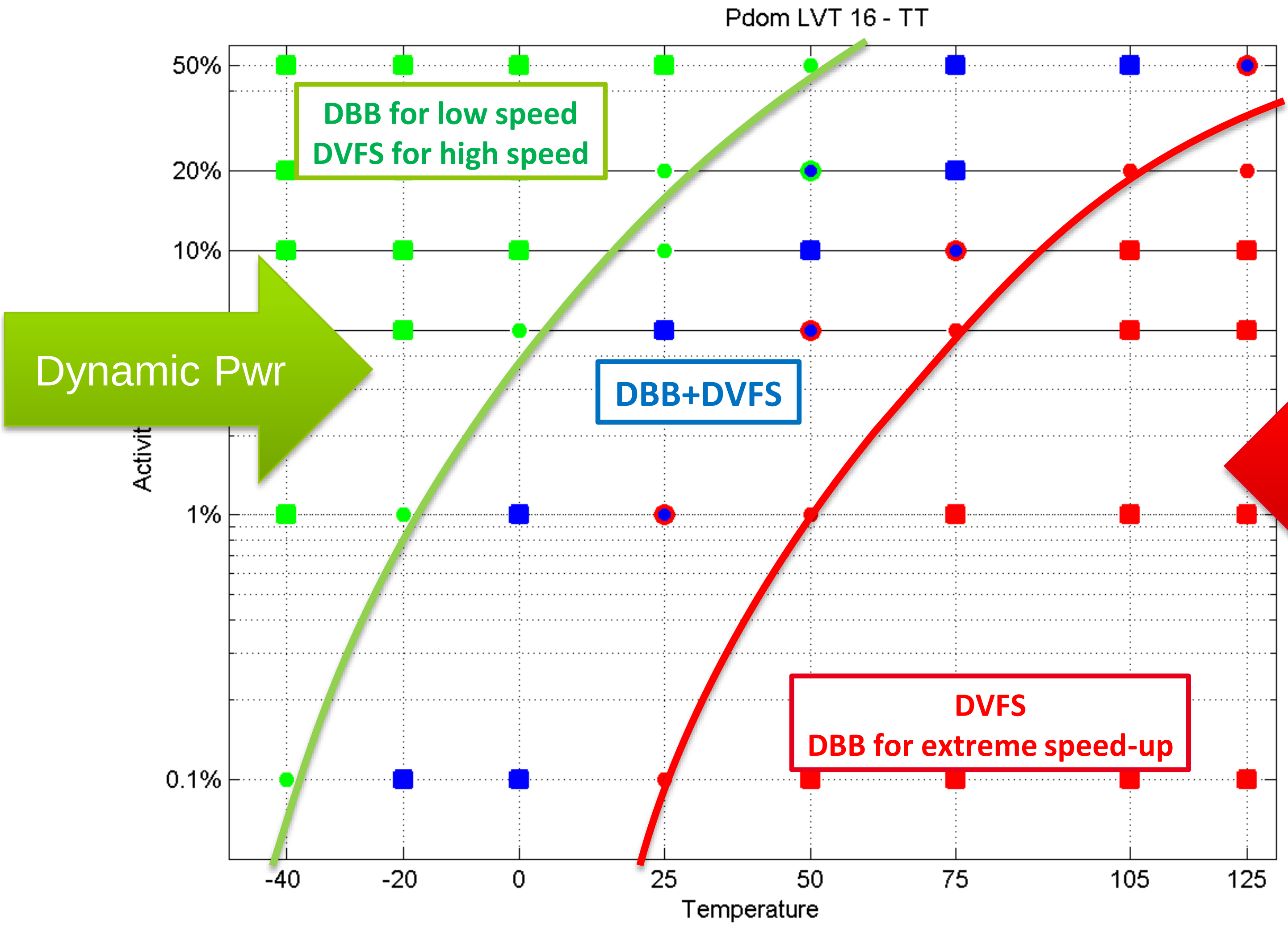
STATIC AND DYNAMIC POWER CONSUMPTION

Dynamic Power Dominates | Dynamic ≅ Static | Static Power Dominates



T= -20° | T= 50° | T= 125°

DBB VS. DVFS



Process TT
Vbb = -1.5V to 0V
Vdd = 0.6V to 1.4V

THANK YOU!

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