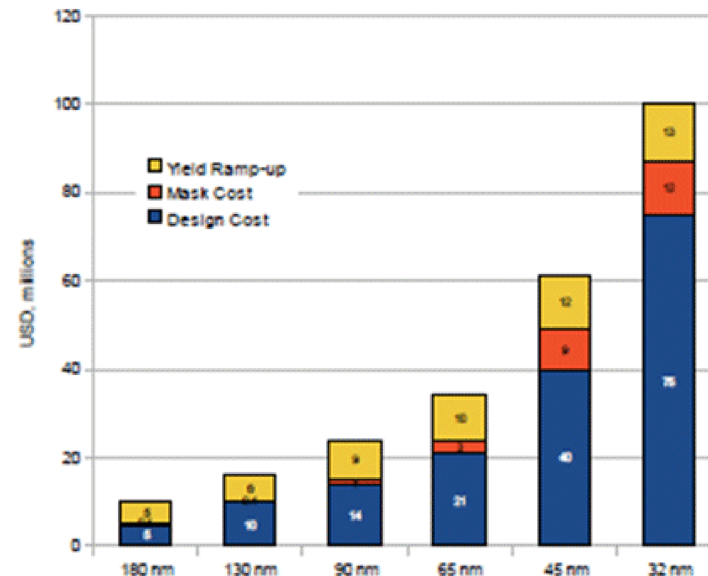
3D MULTICORE: FROM WIDEIO TO PHOTONIC INTERPOSERS

MPSOC | CLERMIDY Fabien | July 11, 2016

SOC DEVELOPMENT: IS THERE A FUTURE?

- **SoC development cost is exponentially increasing**
- **Limited to huge mass markets?**
- **But**
  - Power efficiency, new applications, big data, fragmented market of IoT…
- **New design solutions?**

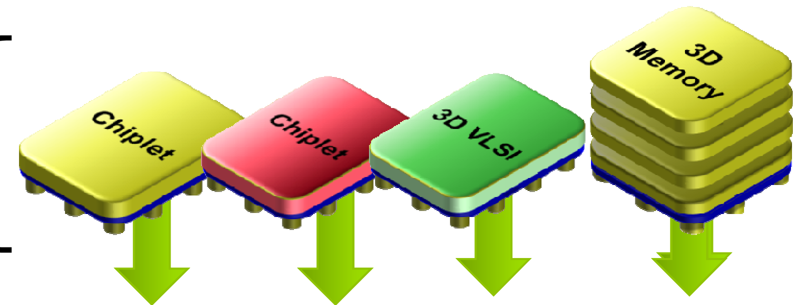


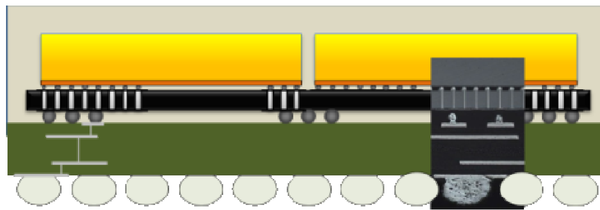
3D AS A SOLUTION TO DECREASE SOC DESIGN COMPLEXITY

- **3D technologies are now mature**
- **After 2D scaling, going 3D is a natural extension**
- **3D is multiform and can provide a full range of possibilities:**
  - Advanced packaging
  - Yield improvement
  - Performance (power/frequency) increase
  - Heterogeneous integration
  - Scalability and modularity

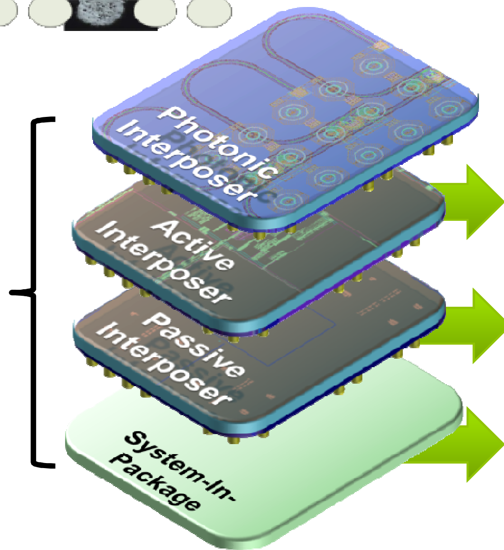
3D: FROM IP TO CHIPLET REUSE

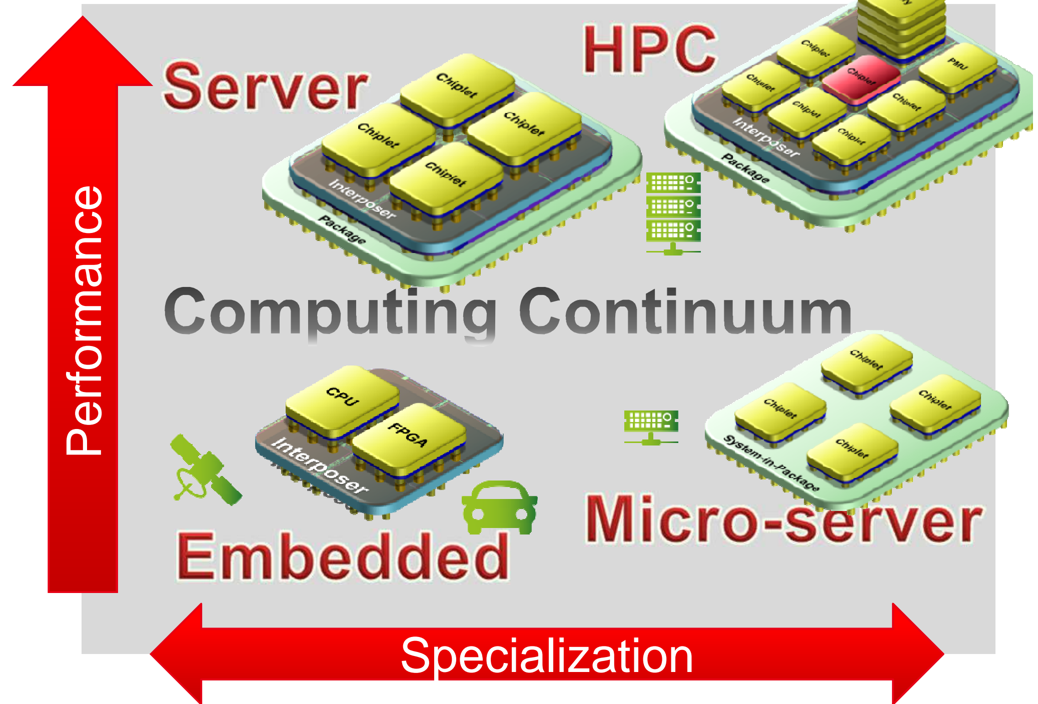
Compute, co-processor and memory *chiplets*



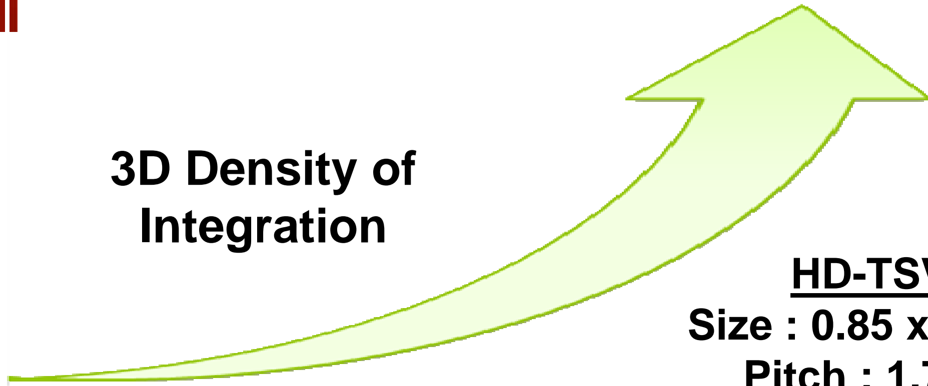


Interposer Integration





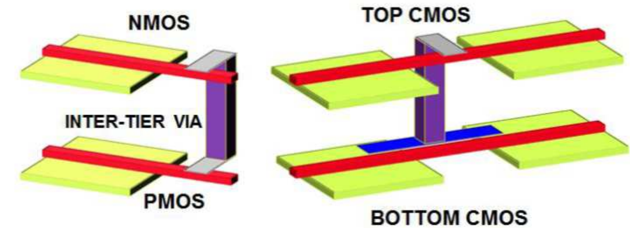
3D INTEGRATION TECHNOLOGIES



3D VLSI & CoolCube™ [3]
Size : 0.05 x 0.05 µm
Pitch : 0.11 µm

10^8 3D Contacts / mm²
=> Transistor Level Integration

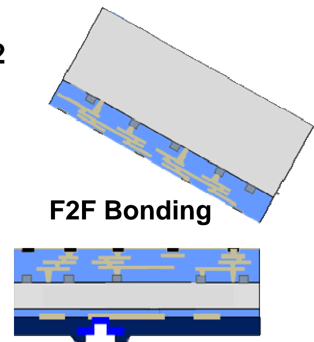
HD-TSV [2]
Size : 0.85 x 0.85 µm
Pitch : 1.75 µm



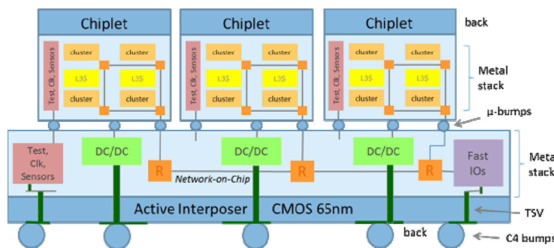
> 10^4 3D Contacts / mm²
=> Gate Level Integration

~10^3 3D Contacts / mm²
=> SoC Level Integration

Cu-Cu [2]
Size : 1.7x1.7 um²
Pitch : 3.4 µm



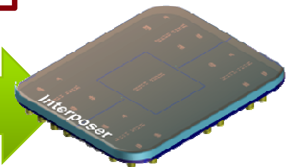
TSV + µBump[1]
Size : 10 x 10 µm
Pitch : 20 µm



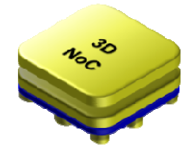
- 3D technologies available @ LETI
  - MD and HD TSV, µ pillars
  - Hybrid bonding (Cu-Cu)
  - Monolithic integration (CoolCube)

[1] Cheramy, S., et al. "Advanced Silicon Interposer", C2MI Workshop, 2015
[2] Patti, B., "Implementing 2.5D and 3D Devices", In AIDA workshop in Roma, 2013
[3] Batude, P., et al. "3DVLSI with CoolCube process: An alternative path to scaling ." VLSI technology symposium

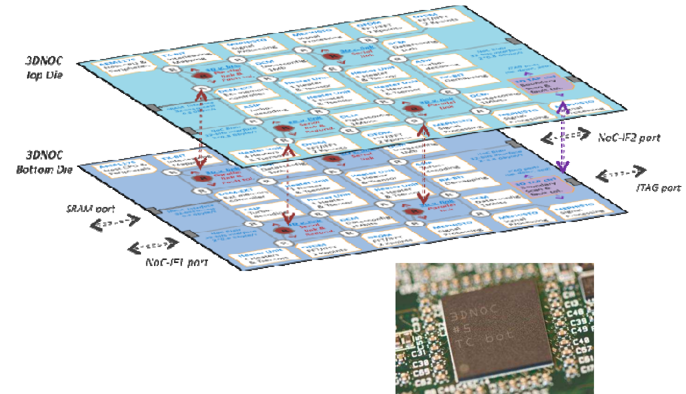
3D COMPUTING ROADMAP @ LETI



3DNOC: A LOGIC-ON-LOGIC MULTI-CORE



- **3D Network-on-Chip based multi-core**
  - Heterogeneous multi-core, MIMO 4G-Telecom application
  - Stack 2 similar dies on top of each others
  - No global clock, robust asynchronous 3D links
  - Serial link for throughput / #TSV trade-off
  - 3D-DFT & Fault Tolerance Scheme



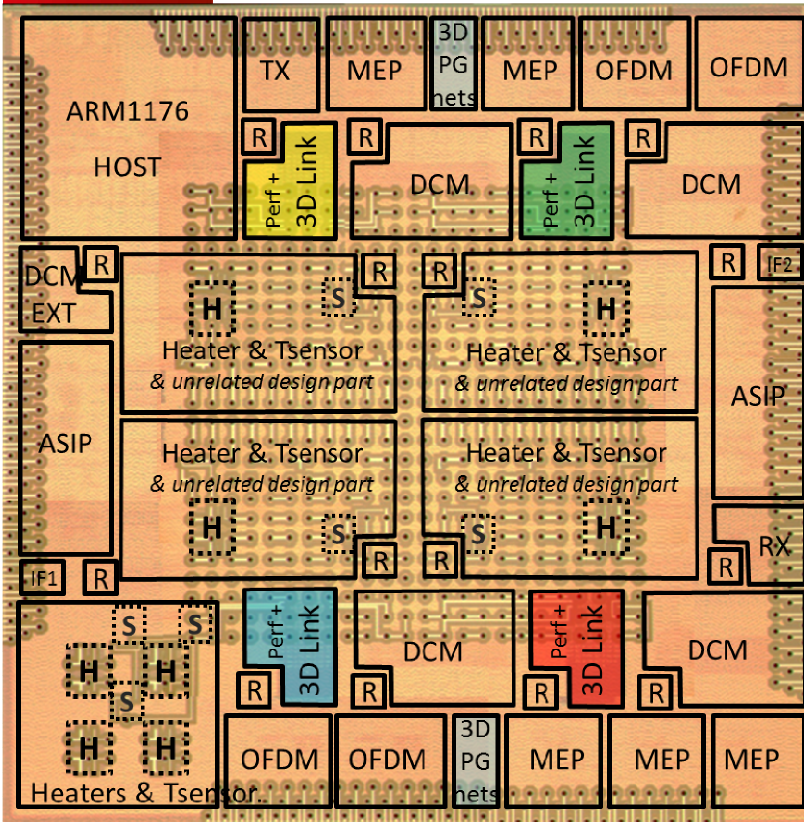
- **3D Link Performances**
  - Fastest link, +20% (326 Mflit/s)
  - Best Energy Efficiency, +40% (0.32 pJ/bit)
  - Self-Adaptation to Temperature, a strong 3D concern

	GeorgiaTech ISSCC'2012	*Kobe Univ. ISSCC'2013*	*This Work*
Architecture	Cache-on-CPU Manycore	Memory-on-Logic 1 layer DRAM	Logic-on-Logic 2 layers 3DNOC
Process & 3D technology	130nm F2F CuCu	90nm F2B TSV	65nm F2B TSV
3D Bandwidth	277 Mbps	200 Mbps	**326 Mbps**
3D I/O Power	-	0.56 pJ/bit	**0.32 pJ/bit**

[P. Vivet et al. ISSCC'16]

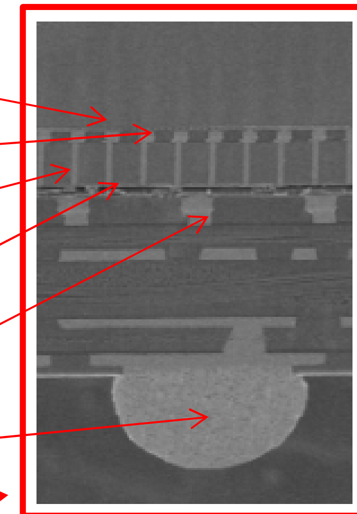
An efficient 3DPlug (asynchronous 3DNOC including test & fault tolerance**):**
a first step towards **3D-based computing architectures**

3D TECHNOLOGY & 3DNOC CIRCUIT

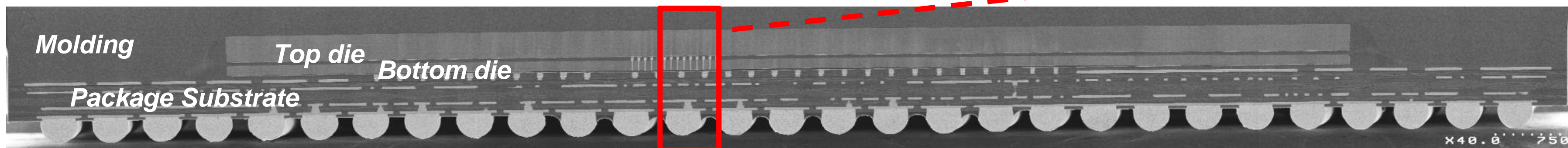


Bottom die photo (72 mm²)

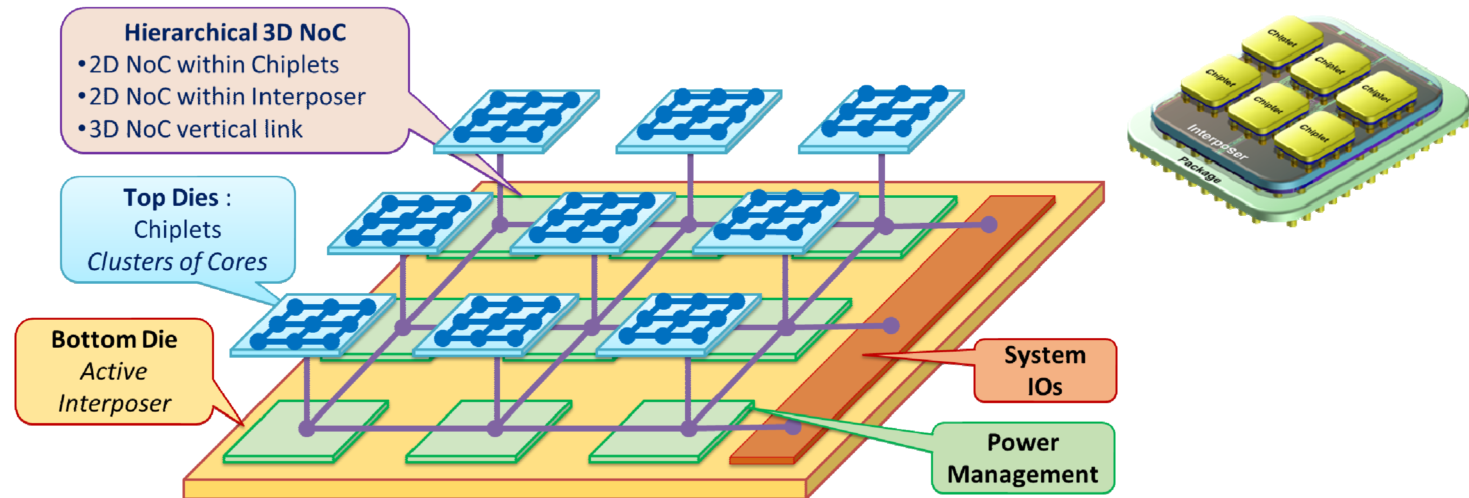
Cmos Process	65nm STMicroelectronics, Low-Power, Multi-VT
3D Tech.	TSV middle (AR 1:8) CEA-LETI µ-bumps, 50µm x 40µm pitch Face2Back stacking, Die2Die assembly
Package	12x12x1.2 flip-chip package, 4 layers substrate
Complexity	1.63 Mbyte SRAM, 228 Mtransistors, 276 IOs
Die Size	8.5mm x 8.5mm = 72.2 mm²
Power Supply	Core = 1.2 Volts, I/O pads = 2.5 Volts



3D cross section



ACTIVE INTERPOSER PARTITIONING FOR MANY-CORE



« Active » Interposer : which added value ?

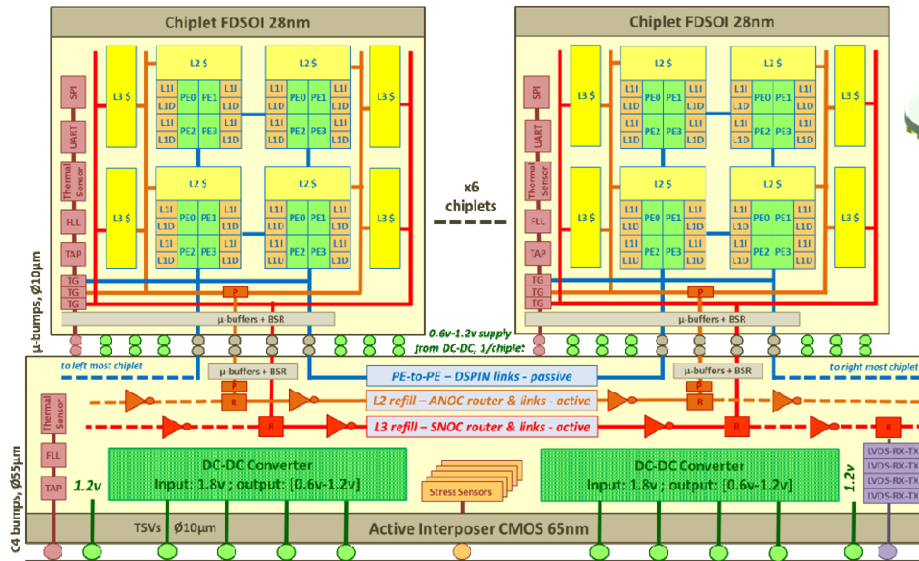
- **Heterogeneous 3D** - Advanced tech node for computation <u>within chiplets</u>
  - Mature tech node for communication/power/DFT/etc
- **Chip-to-Chip Interconnect** - Hierarchical NoC, for energy efficient communications
- **System IOs** - On Interposer, for off-chip memory accesses
- **Power Management** - Chiplet power supply, without any external passives

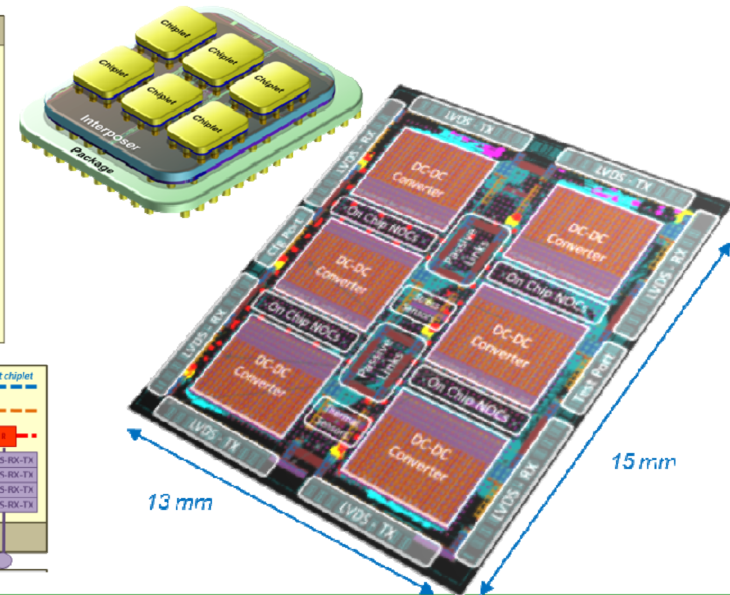
- **And most of all ... preserve (active) interposer cost with mature technology !**

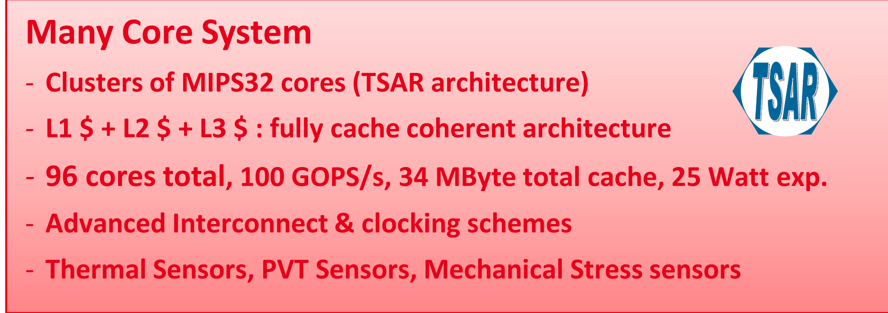
INTACT : AN ACTIVE INTERPOSER IN ADVANCED 3D TECHNOLOGY FOR CACHE COHERENT MANY CORE

*6 * Chiplets FDSOI 28nm*

Active Interposer CMOS 65nm







Many Core System

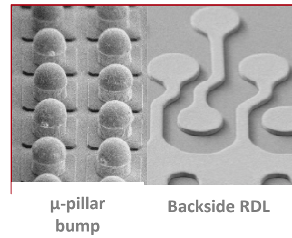
- Clusters of MIPS32 cores (TSAR architecture)
- L1 $ + L2 $ + L3 $: fully cache coherent architecture
- 96 cores total, 100 GOPS/s, 34 MByte total cache, 25 Watt exp.
- Advanced Interconnect & clocking schemes
- Thermal Sensors, PVT Sensors, Mechanical Stress sensors

3D Partitionning

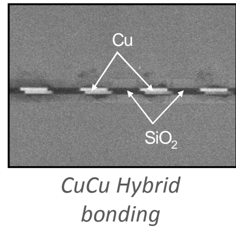
- 6 Chiplets in Advanced 28nm FDSOI technology, with Body biasing
- Active interposer in 65nm CMOS, with *« Smart features »*
  - Integrated Power Management (Switch cap DC/DC converter)
  - Pipelined NoC Interconnects + Fast IOs (LVDS links)
  - 3D DFT infrastructure

Advanced 3D technology

- µ-bumps (10µm diameter, 20µm pitch)
- CuCu Hybrid Bonding (7 – 20 µm pitch)
- TSV middle (1:10 AR, 40µm pitch)
- Back Side RDL (10µm pitch)
- Large size interposer (200 mm2, with 22mm2 chiplets)



µ-pillar bump   Backside RDL

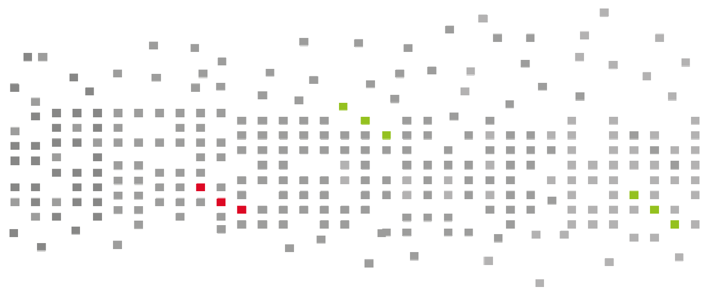


CuCu Hybrid bonding

IRT 3D Program

CONCLUSION

- **SoC complexity is currently limiting the innovation**
- **3D staking can give a new dynamic**
  - From IP reuse to chiplet reuse
- **3D technology basics are ready and technology is progressing quickly**
- **Full LETI's roadmap for exploring this new world of possibilities**



THANK YOU FOR YOUR ATTENTION

QUESTIONS?