Open ISA Core

More Freedom for Processor Architect

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Motivation

- **Old ISA** processors are **still dominant** in the market.
  - **X86**: since 1978 (8086), 1985 (IA-32), 2000 (x64)
  - **ARM**: since 1981 (ARM1), 1994 (v4, for ARM7, StrongARM, XScale)
- Because, ISA is **hard to change**.
  - Huge legacy software, Established ecosystem
- However, ISA **must be changed**
  - for **new applications** such as **AI**, **IoT**, ...,
  - for **multi-many cores**,
  - for **finer process**, and under power limitations.
  - Only highly efficient processor can achieve high performance.
- **Processor architects** must have **more freedom**.
  - We must find **a way to realize new ISA processor**.

What's General Purpose Processor (GPP) ?

- GPP is **pure general purpose**? – No!
  - **x86** is tuned for **PC/Server**.
  - **ARM** is tuned for cellular/smart **phones**.
  - GPP plays a role of a special purpose processor (**SPP**), too.
- Major GPPs are for **established big-market** application
  - GPP is the heart of its **ecosystem**, requiring **vast investments**.
  - All the established GPP ISAs are **proprietary**.
- For **New Application**
  - **GPP ecosystem** can be better than that made **from scratch**.
  - However, it may be **too far from ideal**. (GPP is tuned for others.)
  - **Significant "+α"** is necessary for efficiency and performance.
  - Further, proprietary GPP is **too expensive** for small start.

Current Open ISA Croe

- **Established ISA**
  - **GPP ecosystem** is already established.
  - **J-core** (**SuperH**), OpenSPARC (UltraSPARC T1/T2)
  - Please search with "J-core processor". (Just "J-core" is not enough.)
  - It hit to www.0pf.org, j-core.org, EE times article, etc.
  - Is it good enough for **new applications**? -- No, but it's **not a matter**.
- **New ISA**
  - ISA can be sophisticated regardless of compatibility.
  - RISC-V (riscv.org), OpenRISC (openrisc.io)
  - It has good potential, but it is difficult to establish its GPP ecosystem.
- **Open Established-ISA Simple Cores** are the best for **GPP**.
  - **J-core** (**SuperH**)

GPP: Open Established ISA + Simple Cores

- **Open Innovation Era**
  - Each vender do only the **expertised** part.
  - The key is to define **standard interfaces**, and to establish **ecosystem**.
  - **ISA** is the most important **interface**, and must be **standardized**.
  - **Established ISA** GPP can minimize **investment** and **time** for above.
- **Multi-Many-Core Era**
  - Each core on a SoC should do only the **fit jobs** to it.
  - **GPP** should concentrate on the role of the **heart of its ecosystem**.
  - The **simpler** is the **more efficient** for processor cores. (Pollack's rule)
  - GPP should be **pure GPP**, and highly efficient by **simple cores**.
  - **SPP** should **accelerate** the important parts of applications.
- **New-ISA Simple Cores** are the best for **SPP**.

SPP: New ISA + Simple Cores

- **Open ISA GPP for New ISA SPP**
  - **New ISA processor** can be an **SPP** easier than ever **with open GPP**.
  - The **SPP** can be **free** from various **ecosystem** issues.
- **GPP vs. SPP**
  - **GPP** must treat **huge past/future** software correctly.
  - **GPP** must be verified by established/proven **verification suits**.
  - **GPP** must have established **ecosystem** including tools and runtime.
  - **SPP** software can be **limited** for library, written by specialists, and so on.
- **New ISA** is acceptable and the best for SPP.
- **Simple cores** are always the best choice under **power limitation**.

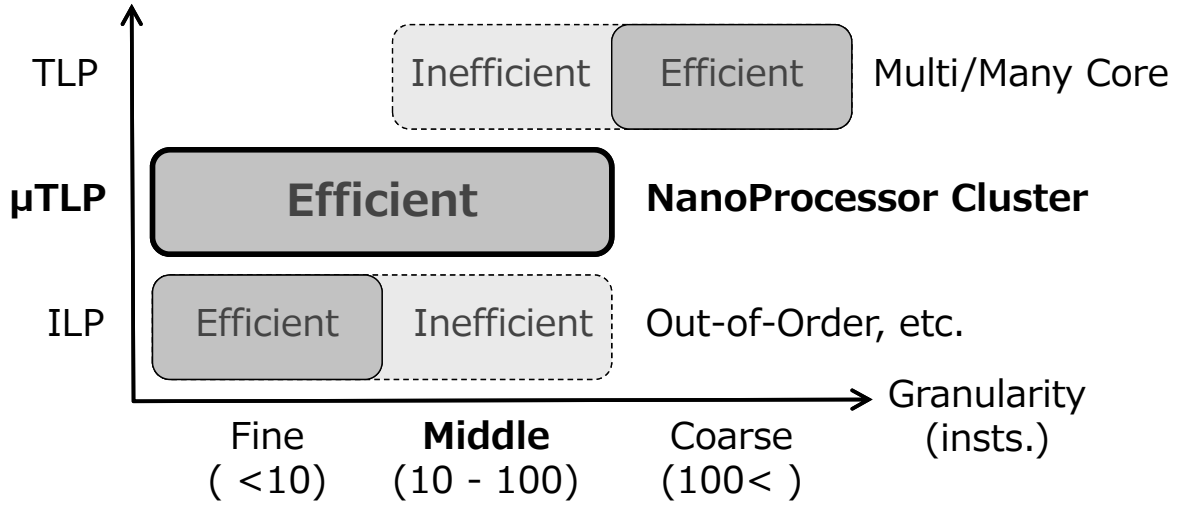
- **NanoProcessor Cluster**: An **SPP** to offload **GPP** jobs **unfit** to it.

NanoProcessor Cluster

- NanoProcessor Cluster Topic in **MPSoC**
  - Conversion from **ILP** to **μTLP** (2014)
  - Naturally Minimizing Active Portion for **Dark-Silicon** Era (2015)
  - Approach from **Special** to **General** Purpose Processor (2016)
- **Approach from SPP to GPP**
  - Technically, NanoProcessor Cluster can be **a highly efficient GPP**.
  - However, GPP should use established ISA as explained above.
  - As an SPP, it fits to important **middle-grain** parts of codes.
  - Starting as an SPP, it can establish **ecosystem for GPP gradually**.
- Past example
  - GPU has become **GPGPU** with its **ecosystem**, but it took long time.
  - It is still SPP because it does not fit to basic GPP's processing.

Conversion from ILP to μTLP

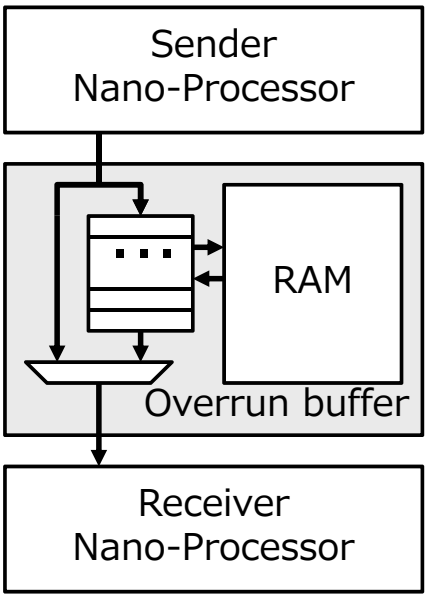
- Fine/Coarse Grain: fit to ILP/TLP *), respectively
- **Middle Grain: Bad for conventional Arch.**
- **μTLP** of **NanoProcessor Cluster** fits to Middle Grain



*) ILP / TLP : instruction/thread level parallelism

Overrun buffer for Dark Silicon

- In order to absorb write/read timing gap of NanoProcessors
  - While sender and receiver paces are well **synchronized**, overrun buffer is **idle**.
  - Once receiver **stalls**, it requests to stop data sending and **keeps all the on-the-fly data** in overrun buffer.
  - On-the-fly data can be huge in a high-throughput long-latency case, and a **RAM** is useful.
  - Either the sender/receiver or overrun buffer is active.
    => fit to **Dark silicon era**



Trends for Processor Architecture

Trend	Issue	from	to
Open Innovation	R&D	Closed	Open
	ISA, Architecture	Proprietary	**Open**
	Interface	Proprietary	Open Standard
	Competitive design	Full custom	**Expertised** part
Multi-many cores (Distributed Processing)	Processing style	Master/Slave	**Distributed**
	Operation start	Code driven	**Data** driven
	Data/Code transfer	Pull	**Push**
Time to Space	Optimizations	Order	Place
	Process switch	Interrupt	**Sleep/Wake**
Finer process	Major cost	Processing	Transfer
	The Same data	Copy	Regenerate
Power limitation	Activity	Full utilization	**Dark Silicon**
	Core micro-arch.	Complex	**Simple**

Summary

- **Old ISA** processors are **still dominant** in the market.
- **Processor architects** must have **more freedom**.
- **New ISA processor** can be **SPP** easier than ever **with Open GPP**.

- In **Open Innovation** & **Multi-Many-Core** Era:
- **Established-ISA Simple Cores** are the best for **GPP**.
- **New- ISA Simple Cores** are the best for **SPP**.

- **J-core** (**SuperH**): **Open-Established-ISA Simple Core** for **GPP**
- **NanoProcessor Cluster**: An **SPP** to offload **GPP** jobs **unfit** to it.

Dear Computer Architect,

Enjoy Open ISA Cores, and get more FREEDOM.

Thank you