JADE Heterogeneous Multiprocessor Design & Simulation Environment

Jiang Xu

BIG DATA SYSTEM LAB

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

OPTICS Lab

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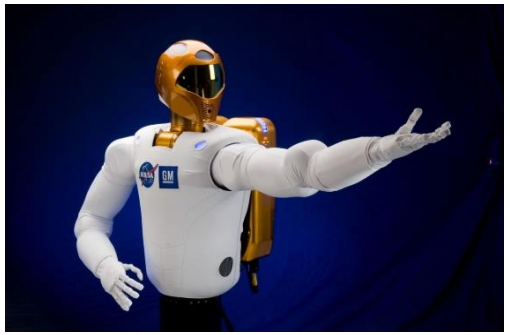
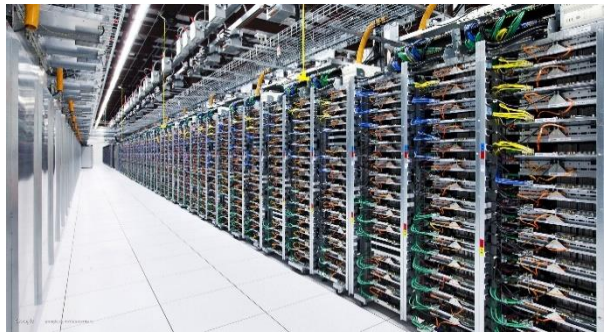
PERFECT Computing Systems

- Design targets
  - Performance
  - Energy efficiency
  - Reliability
  - Functionality
  - Extensibility
  - Cost
  - Testability
- More cores and memory on a chip and in a system
- Heterogeneous



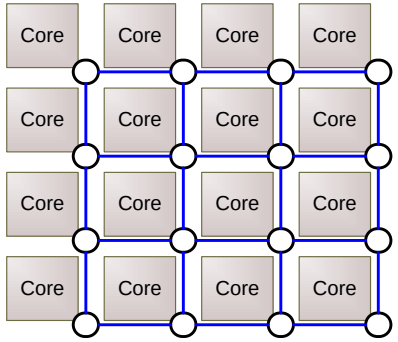


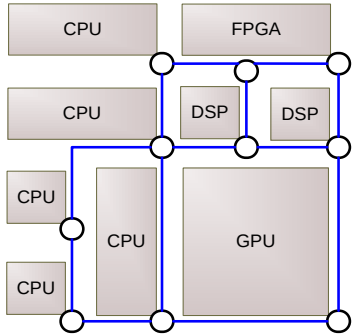


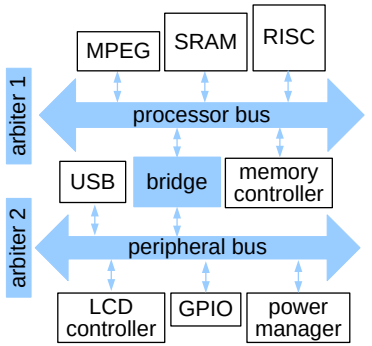


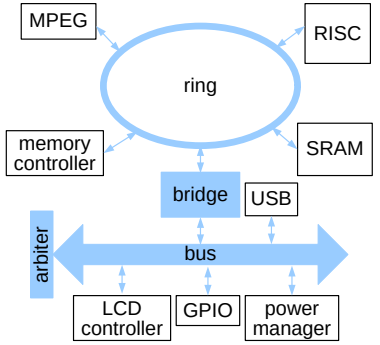

Huge Design Space to Explore

- Application
  - IoT/IoE, mobile, data center, HPC, mainframe …
  - Wireless communication, multimedia processing, machine learning, database …
- Processor
  - CPU, GPU, FPGA, DSP, ASIP, ASIC …
  - Homogenous vs. heterogeneous multiprocessor
  - FinFET, FD-SOI, GAA, CNT FET …
- Memory and storage
  - Hierarchy
  - Cache coherence
  - DRAM, SRAM, flash, STT-RAM …
- Interconnect
  - Ad-hoc, bus, NoC, hybrid …
  - Regular vs. irregular topology
  - Protocol: routing, flow control, congestion control …
  - Switch/router architecture
  - Electrical, optical, RF …
- Support
  - Power delivery and management
  - Clock distribution and management
  - Thermal, aging, noise …
- Peripherals
  - Network interface, user interface, management …



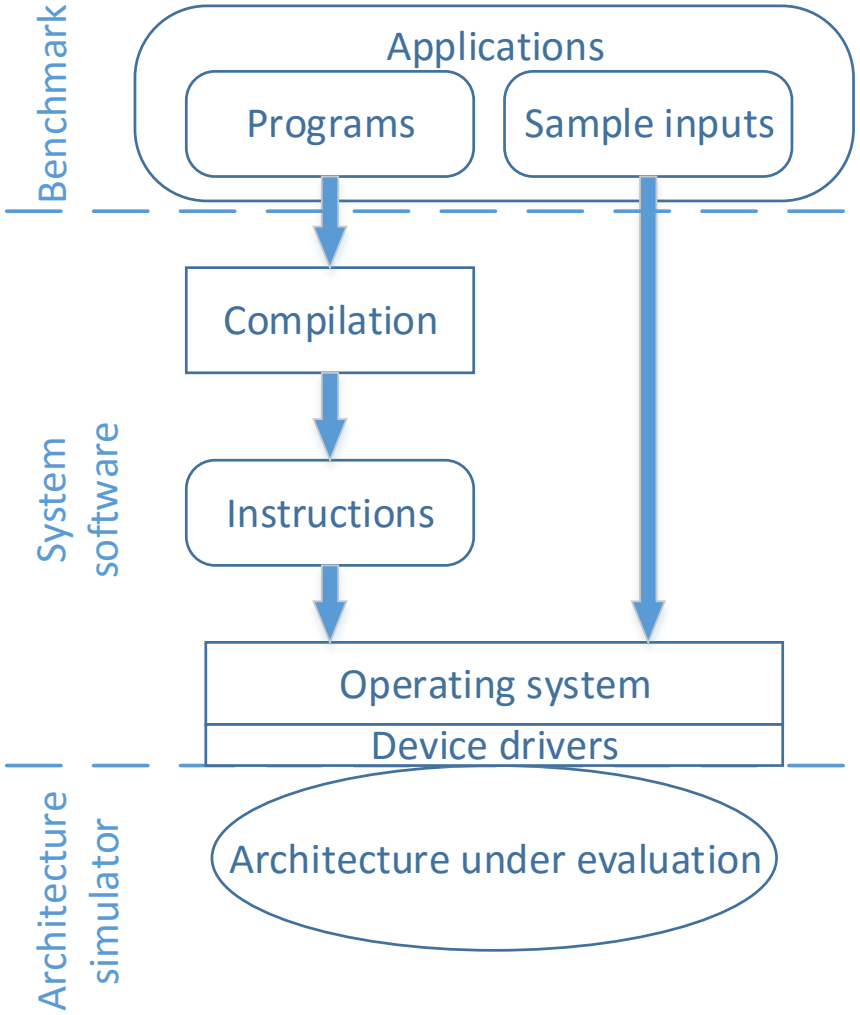






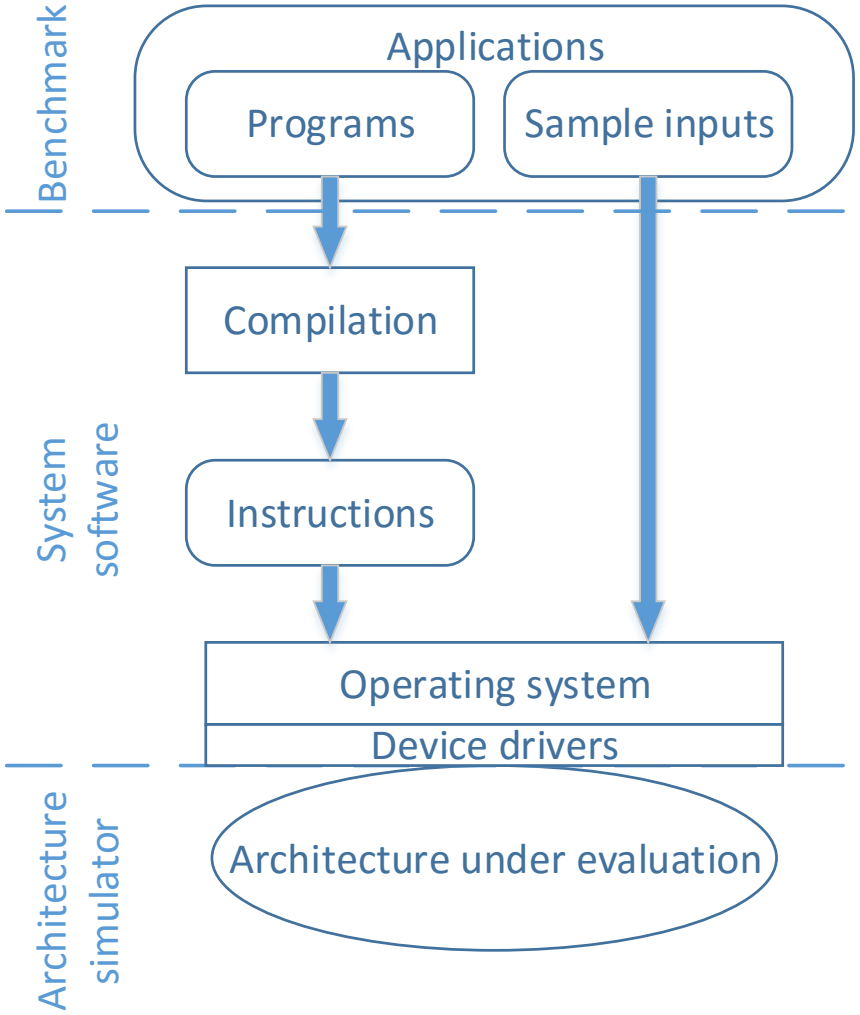
Simulation-based Architecture Exploration

- Benchmark applications with sample input data sets
- System software
- Cycle-accurate "full-system" architecture simulator
- Speed-up techniques
  - Simplify interconnect, memory, processor, OS, *etc.*
  - Sampling application executions
  - Sampling inputs
  - Break causality to better parallelize simulations
  - Hybrid the above techniques



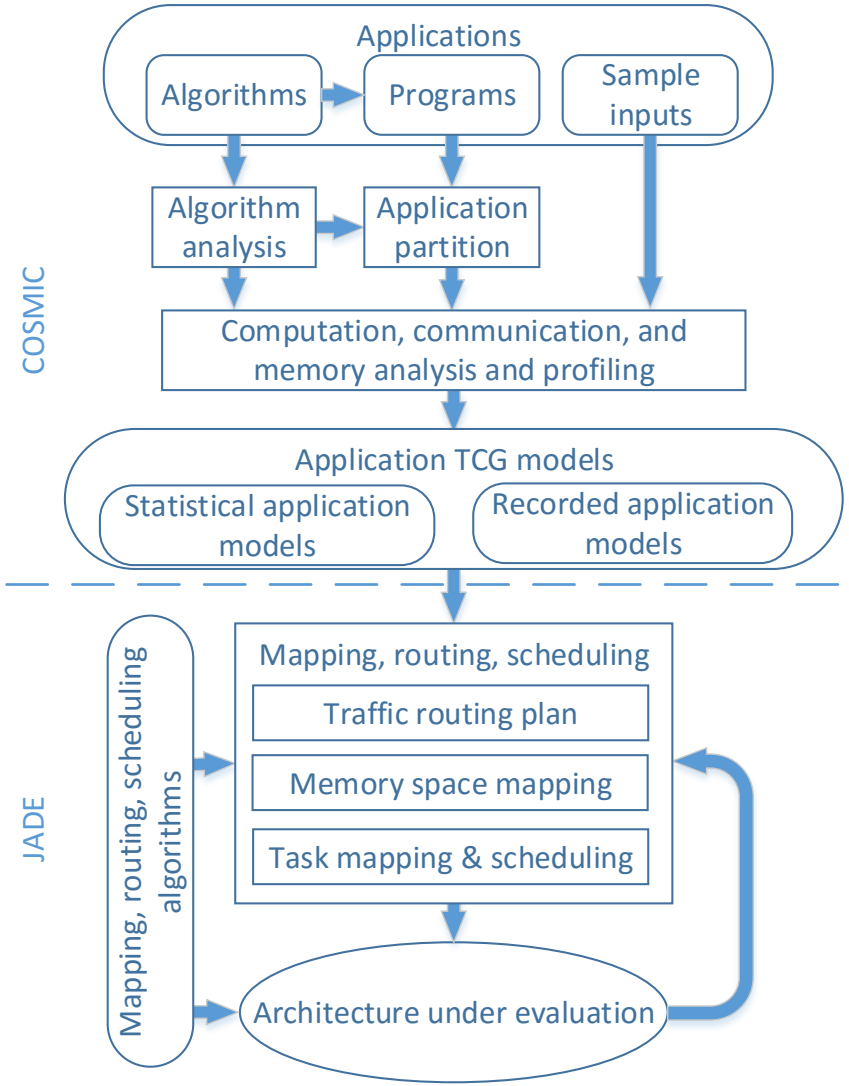
The Good, the Bad and the Ugly

- Good for detailed/late-stage design
  - Tweaking, testing, debugging …
- Bad for early design space exploration
  - Too slow to provide essential system statistics such as average and worst-case performance, energy efficiency, cost …
- Ugly for heterogeneous systems
  - Compilation for heterogeneous ISAs, hardware accelerator, FPGA …
  - OS support of new large-scale heterogeneous systems without drivers



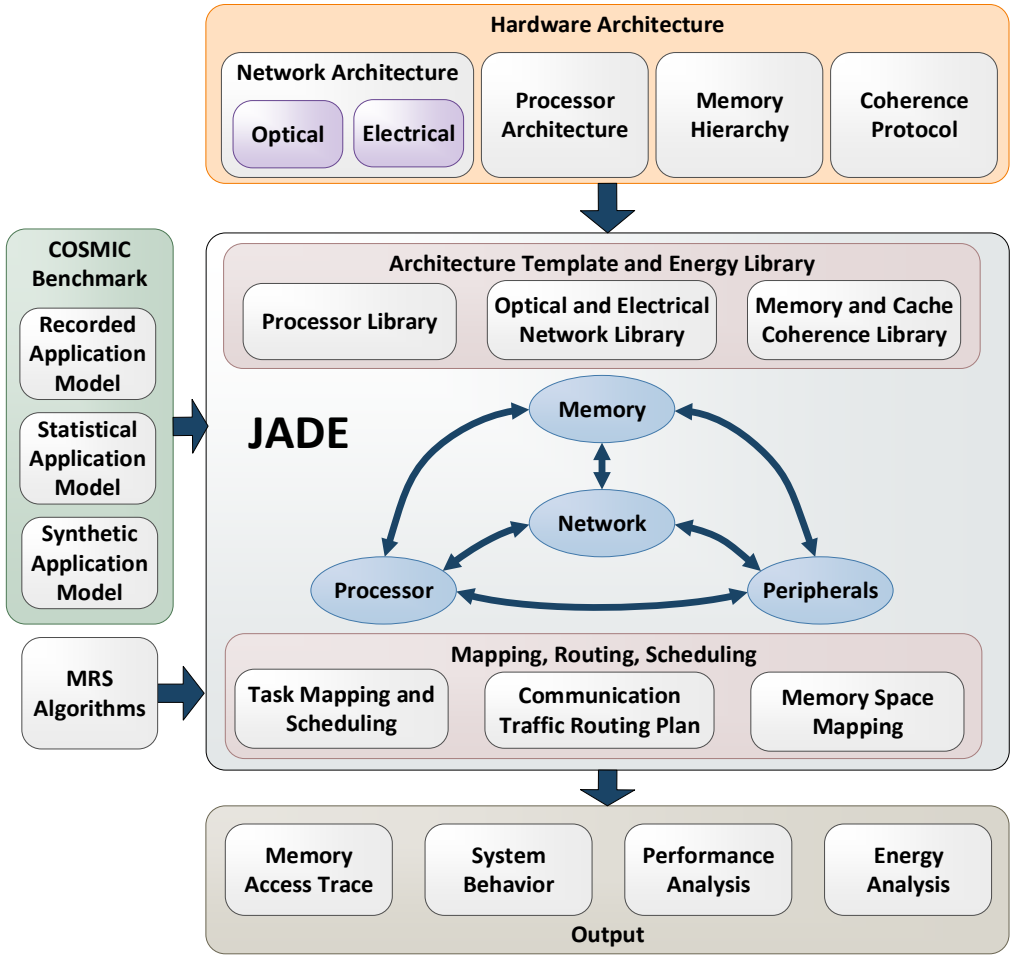
Joint Application/Architecture Design Exploration

- Application models for heterogeneous multiprocessor system explorations
  - COSMIC
- Heterogeneous multiprocessor system design and simulation platform
  - JADE



JADE
Heterogeneous Multiprocessor Simulation Environment

- JADE (Joint Application/Architecture Design Exploration)
  - Heterogeneous system designs
  - Early design space exploration
  - Systematic system evaluation
- Highlights
  - Statistical, recorded and synthetic application models
  - Network-on-chip and off-chip networks
  - Optical and electrical interconnects
  - Memory subsystem
  - Built-in power analysis



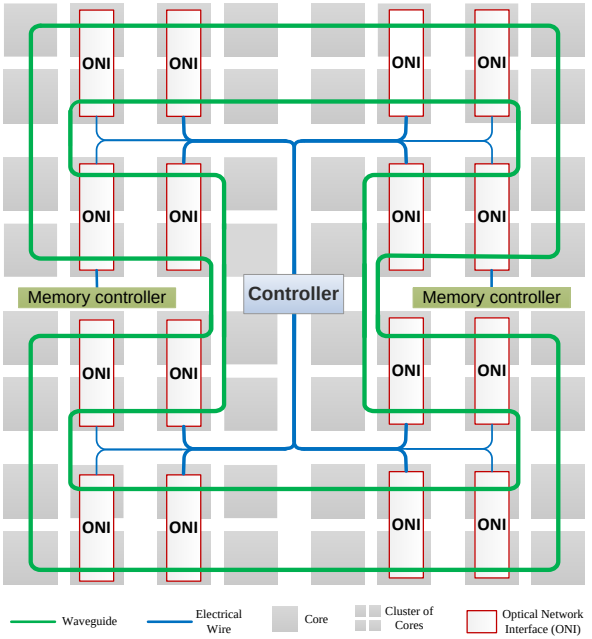
COSMIC Heterogeneous Multiprocessor Benchmark

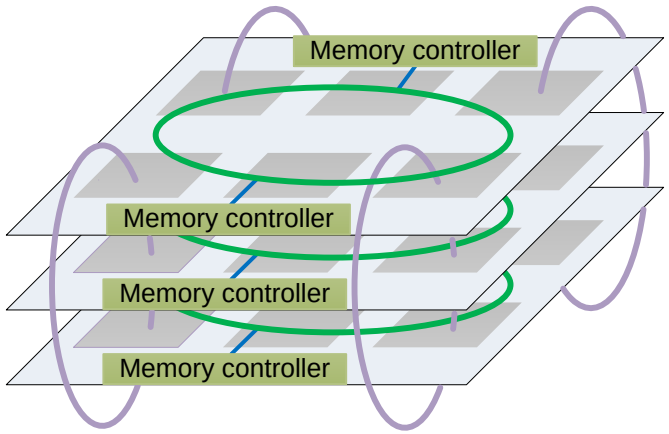
Application	Description
Machine Learning - FMP	Financial market prediction using machine learning
Machine Learning - ALIP	Machine learning based image indexing
Molecular Dynamics	Simulating molecular dynamics when molecules hit surfaces of solid atoms
Ray Tracing	3D scenes rendering
Ultrasound	Medical diagnostics using 2D/3D ultrasound imaging
Fast Fourier Transform	Fast Fourier Transform with complex number inputs
LDPC Encoder	Low-density parity-check code encoder
TURBO Decoder	Turbo code decoder
Reed-Solomon	Reed-Solomon code encoder and decoder

- Collaborating with application experts
- More applications are under development

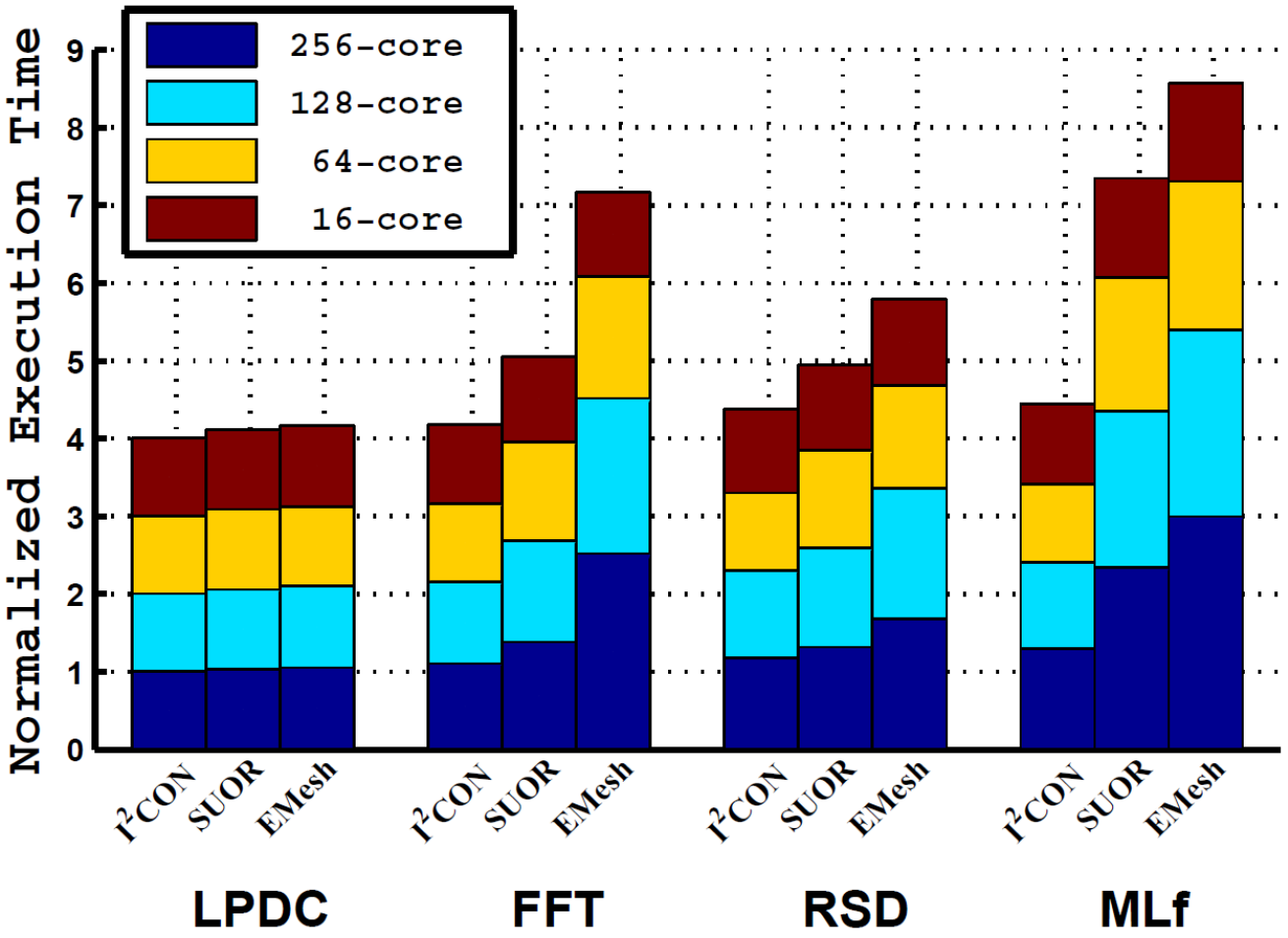
Exploration Cases

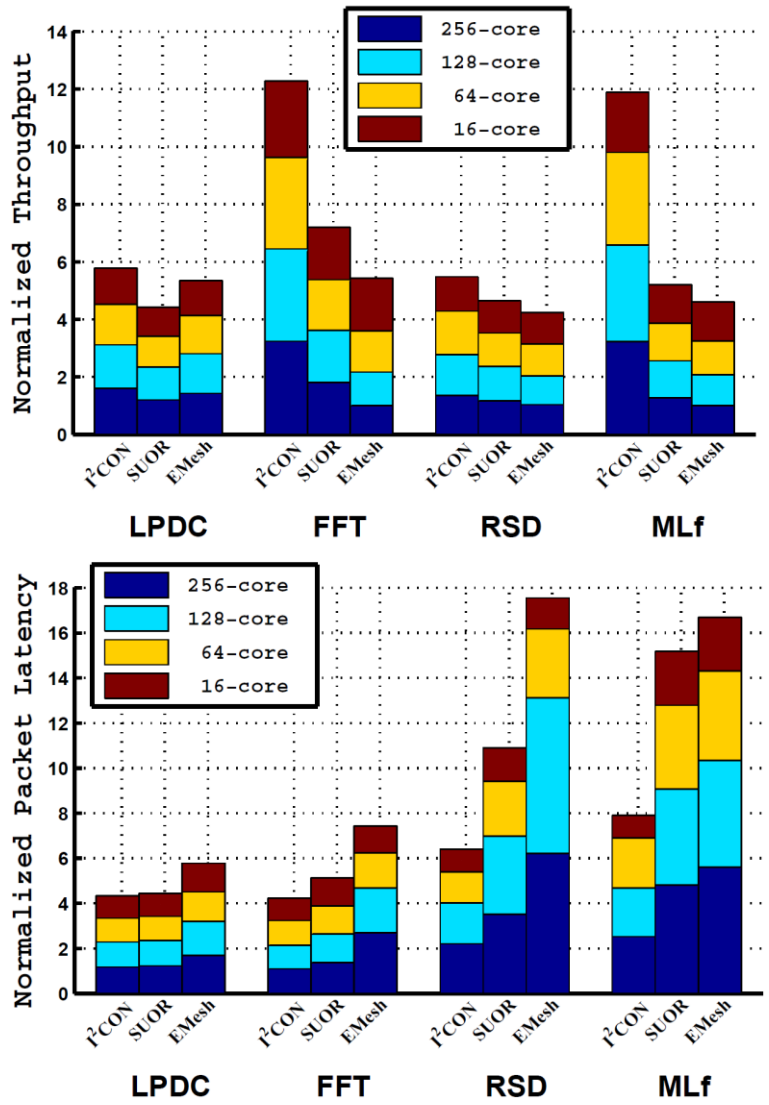
- I²CON inter/intra-chip optical network
- SUOR optical NoC
- Electrical mesh-based NoC
- Memory hierarchy
  - Private L1 caches
  - Shared L2 cache – 16 banks
  - 16 memory controllers
- Processor core
  - ARM-v7a
  - 7nm, 1GHz, 0.6V



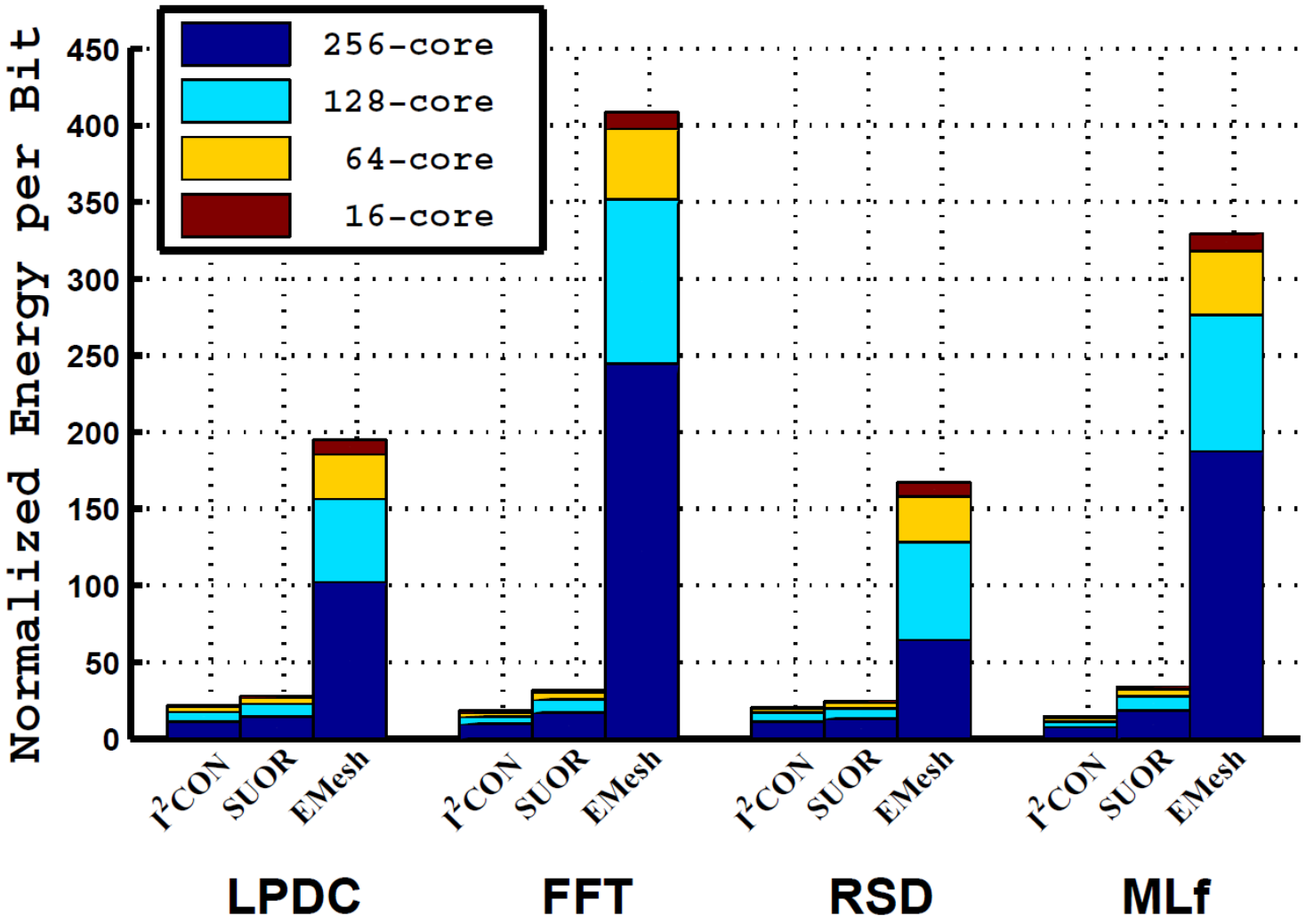


Performance and Scalability





Energy Efficiency and Scalability



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