Edge Computing System for Small Sensing Nodes

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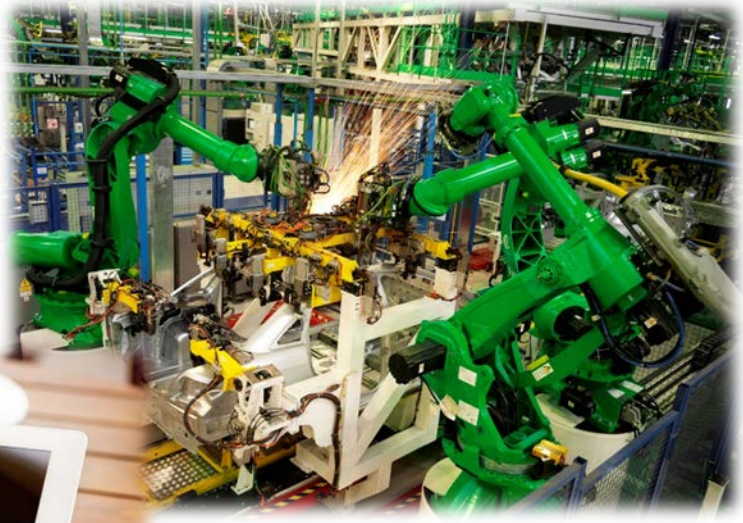
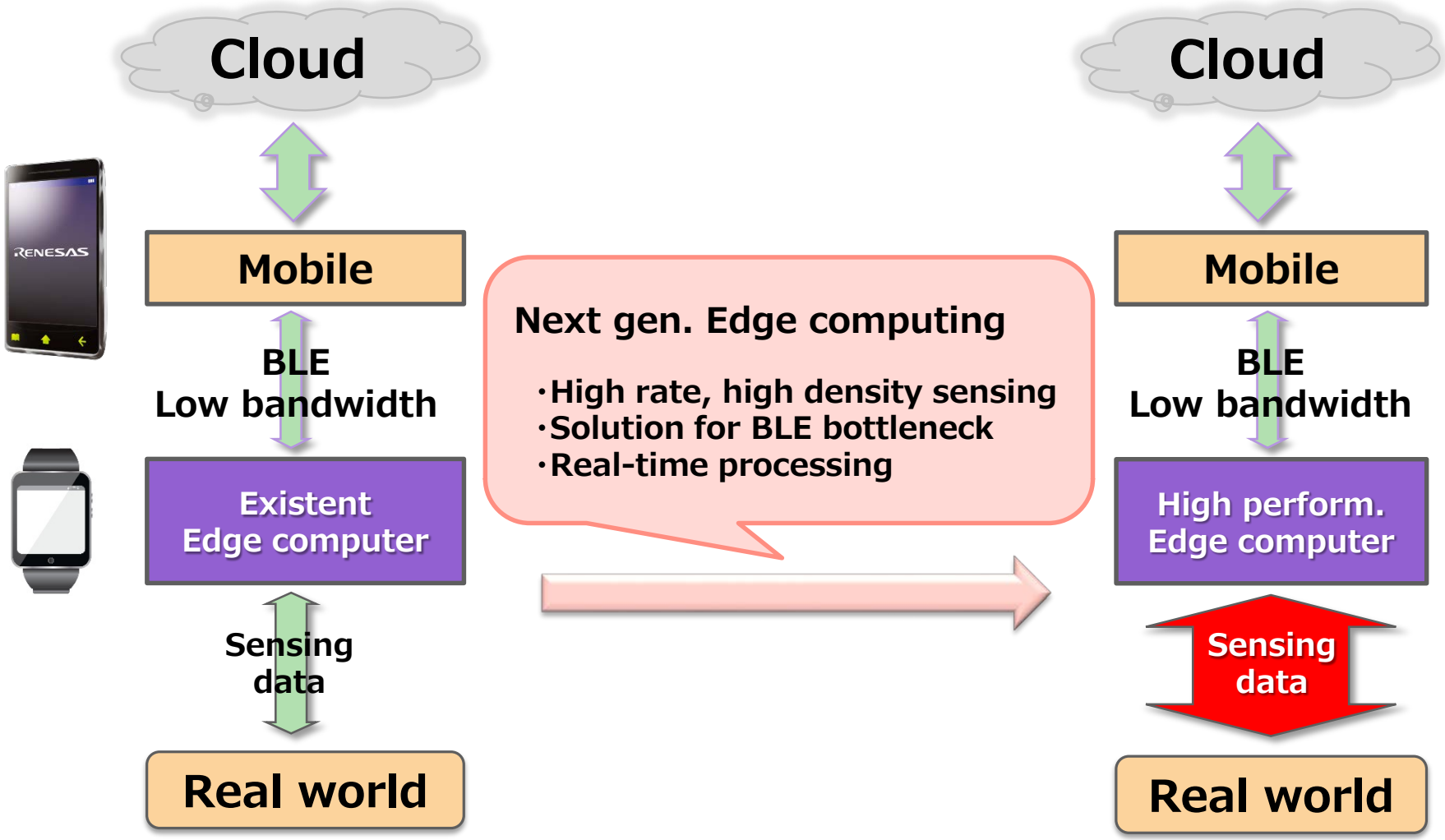
Sensing Applications

Sensors everywhere: and they are invisible

Smaller size and Lighter weight -> Low Power is necessary.



Requirement of high performance “Edge computing”



Example of high-performance edge computing

- **Question? Which sports is the fastest initial ball speed?**

1: Baseball

2: Soccer

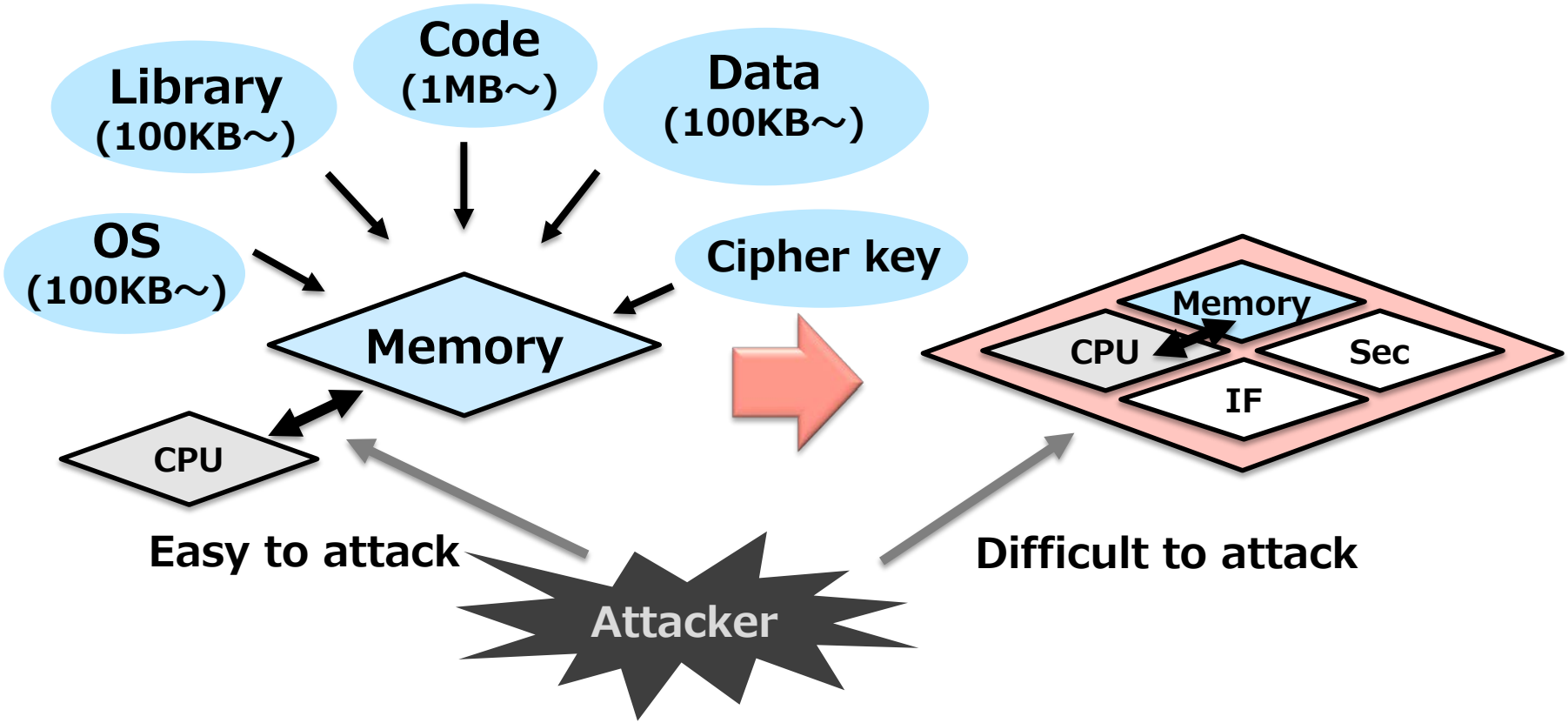
3: Golf

4: Badminton

	150km/h	**195km/h**	**267km/h**	**322km/h**
0.5K/s Sampling	**27cm**	**35cm**	**47cm**	**57cm**
5K/s Sampling	**3cm**	**4cm**	**5cm**	**6cm**

Requirement of large capacity on-chip memory

- **Increasing data to protect**
  - Library and code : Original algorithm
  - Sensing data : Privacy and security information

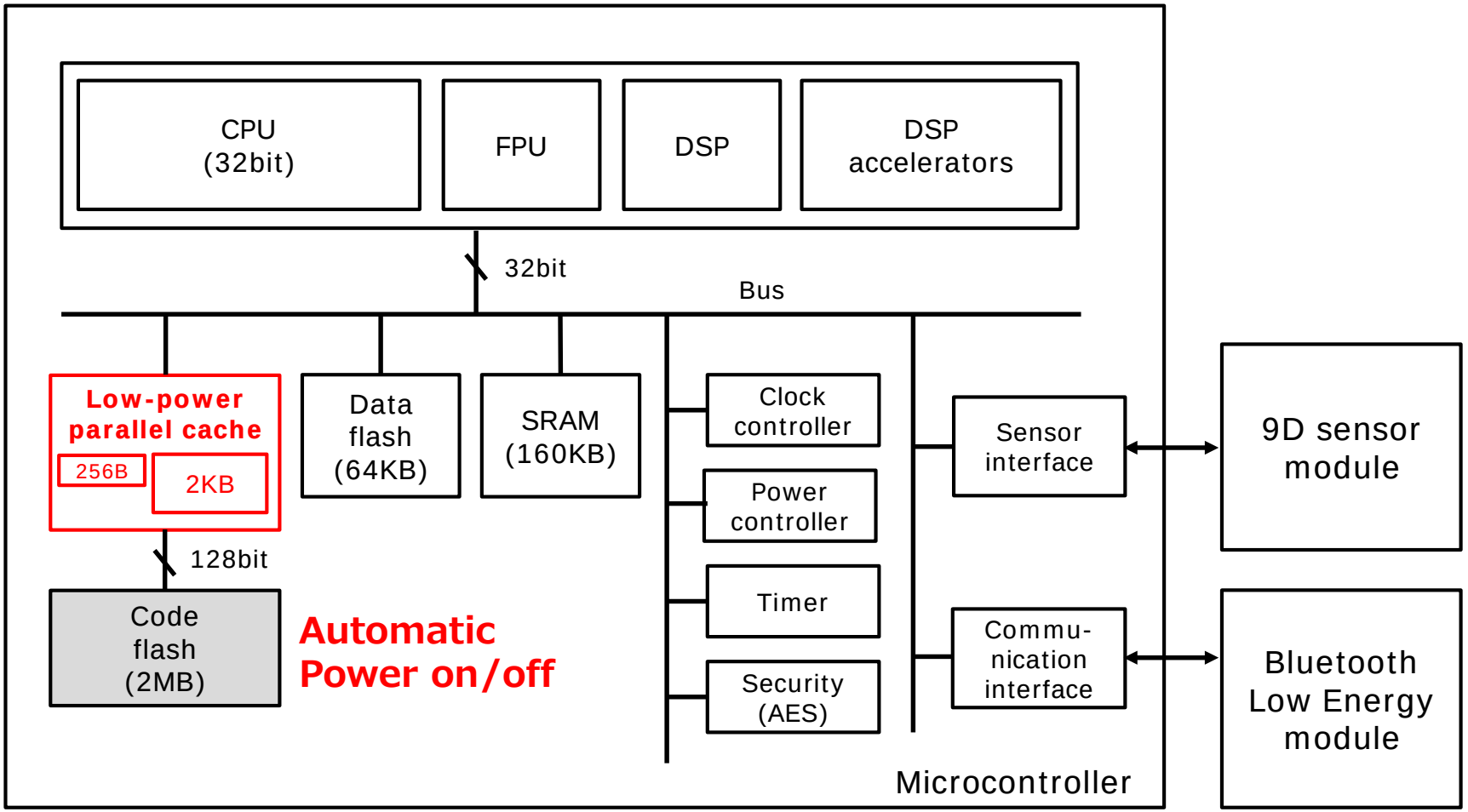


Next generation sensing application requirement

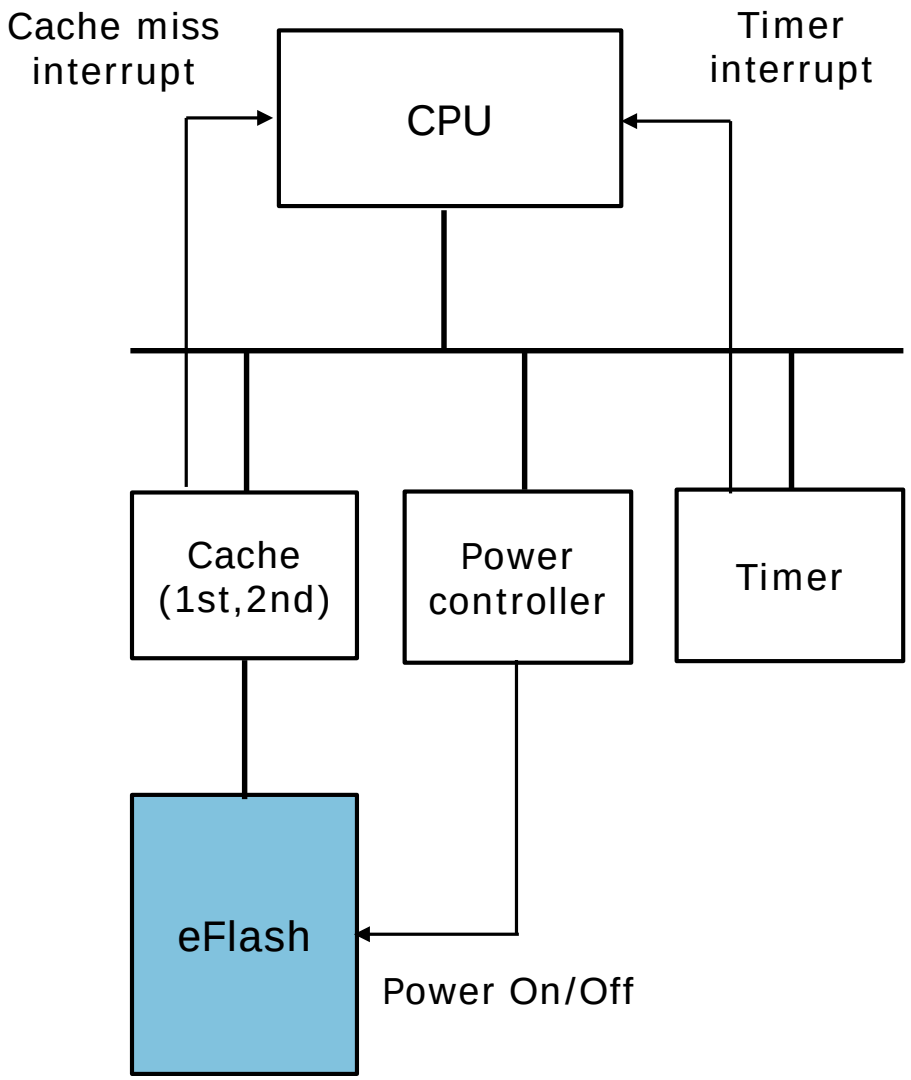
- **Autonomous processing : Edge computing**
  - Higher sampling rate
  - Higher computation power
    -> From data to information or knowledge
- **Expansion of use scene**
  - Smaller size and Lighter weight
    -> Smaller battery size
  - Large memory
- **Strong security**
  - On-chip memory

Low Power Memory Access Scheme

Block diagram of the chip and system



Operation of automatic power on/off scheme



Power On -> Off

- Timer interrupt
- eFlash power off

Power Off state

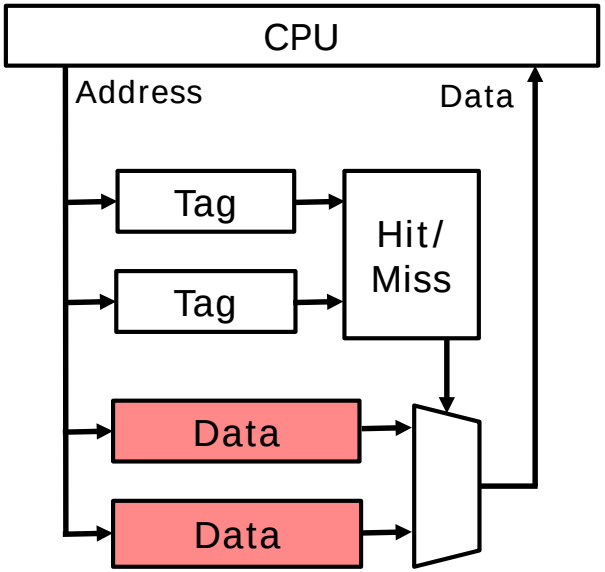
- 1st or 2nd cache hit

Power Off -> On

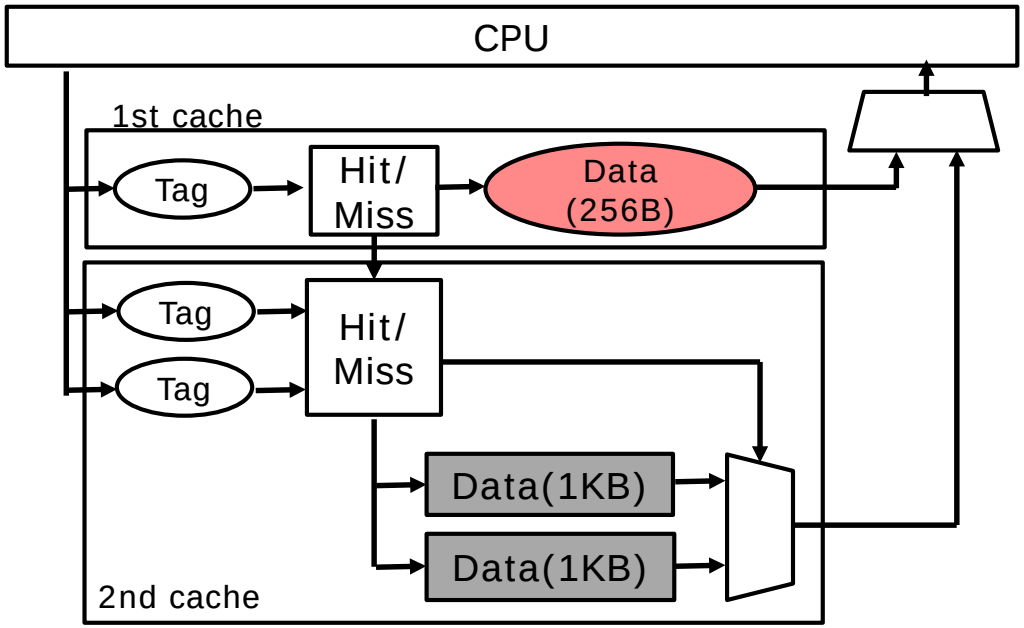
- 1st and 2nd cache miss
- Cache miss interrupt
- eFlash power on
- Read from eFlash

Block diagram of low-power parallel cache

Conventional cache



Proposed cache



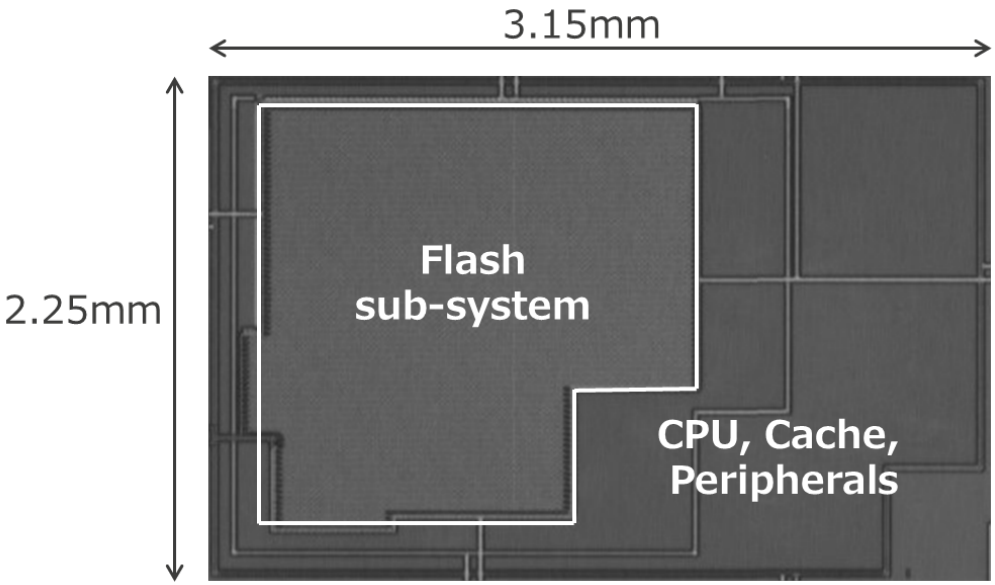
Developed Chip

Chip features

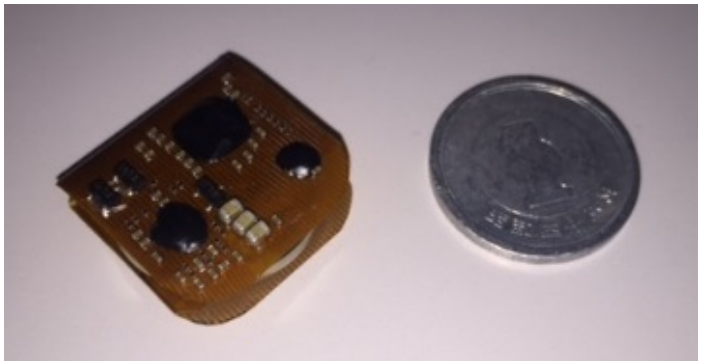
Process technology	40nm low power process with embedded flash
Chip size	3.15mm x 2.25mm
Operation frequency	200MHz (Max)
Current consumption	4mA @ 1.1V (Sensing processing)
Energy efficiency	20uA/MHz
Memory	Code flash : 2MB Data flash : 64KB Cache memory : 256B(FF) + 2KB(SRAM) Code SRAM : 128KB Data SRAM : 32KB

Chip utilizing 40nm eFlash and small sensing module

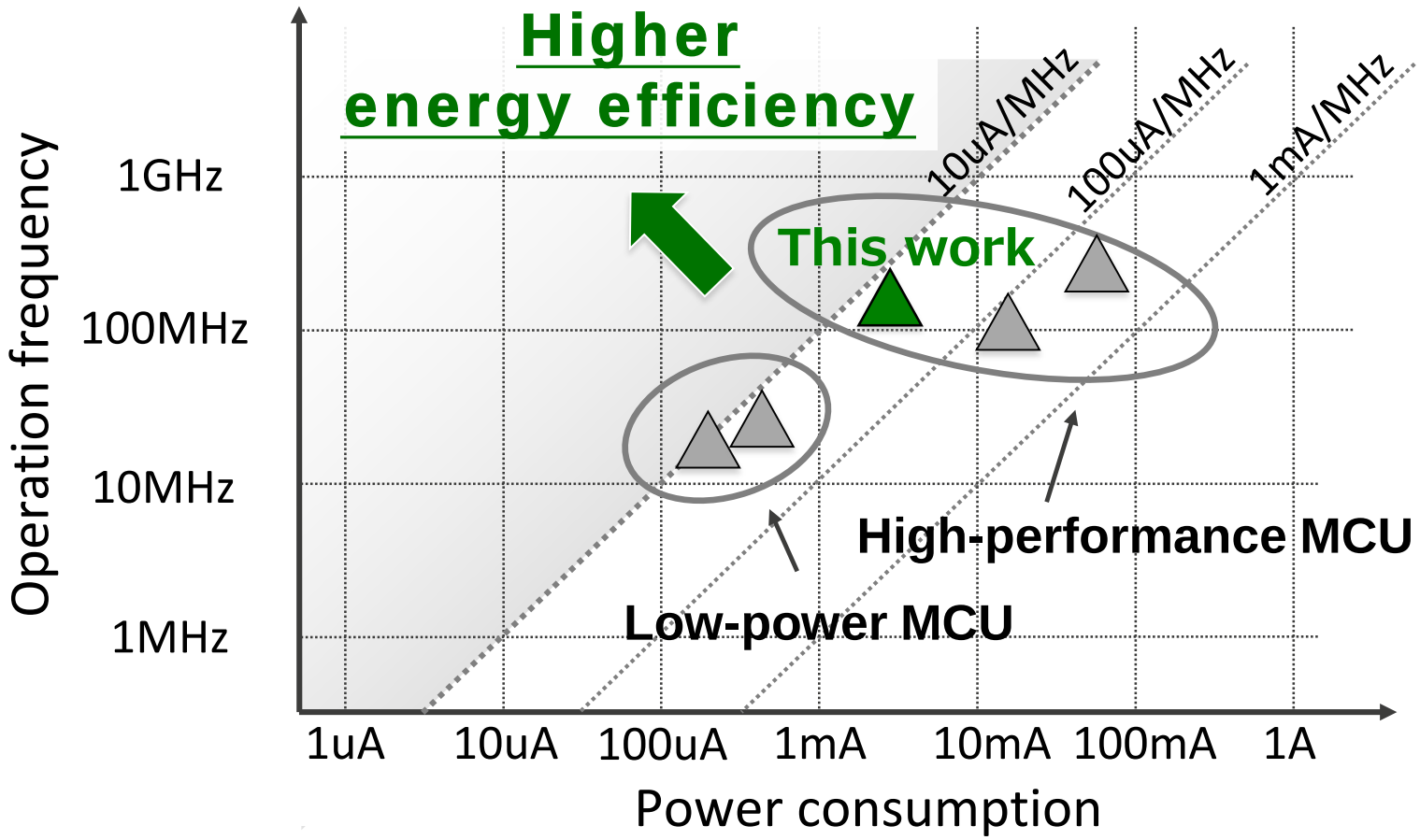
- **Chip micrograph**



- **Small sensing module**



Comparison with previous work



Conclusion

- We showed requirements of the next generation sensing application.
- We have succeeded in reducing power consumption during sensing application operation at 20uA/MHz at 200MHz by using 40nm low power process with embedded flash and Low Power Memory Access Scheme.
- We will enable the next generation sensing application by using small sensor nodes.

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