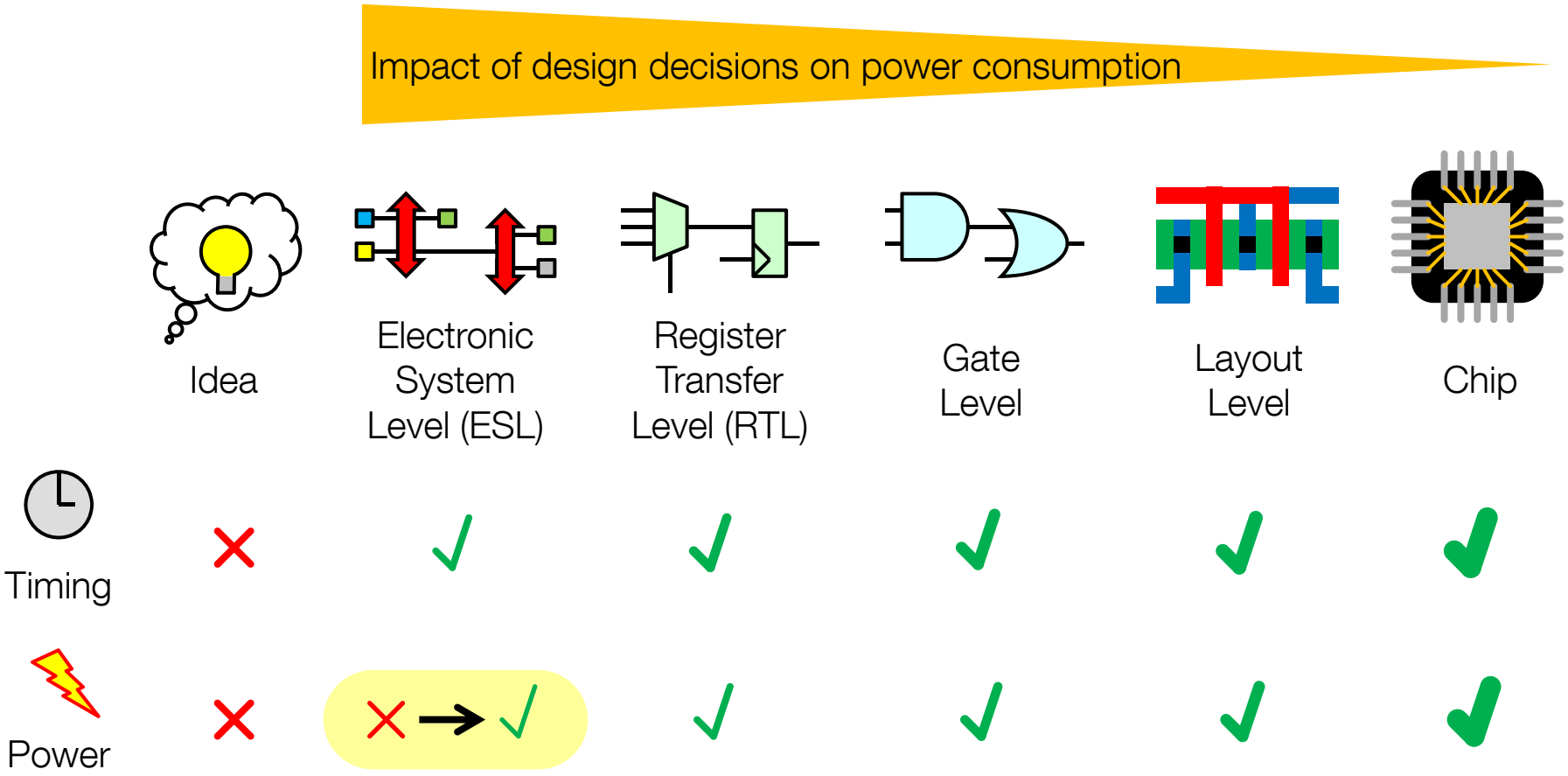
Fast and Accurate MPSoC Power Estimation

Rainer Leupers

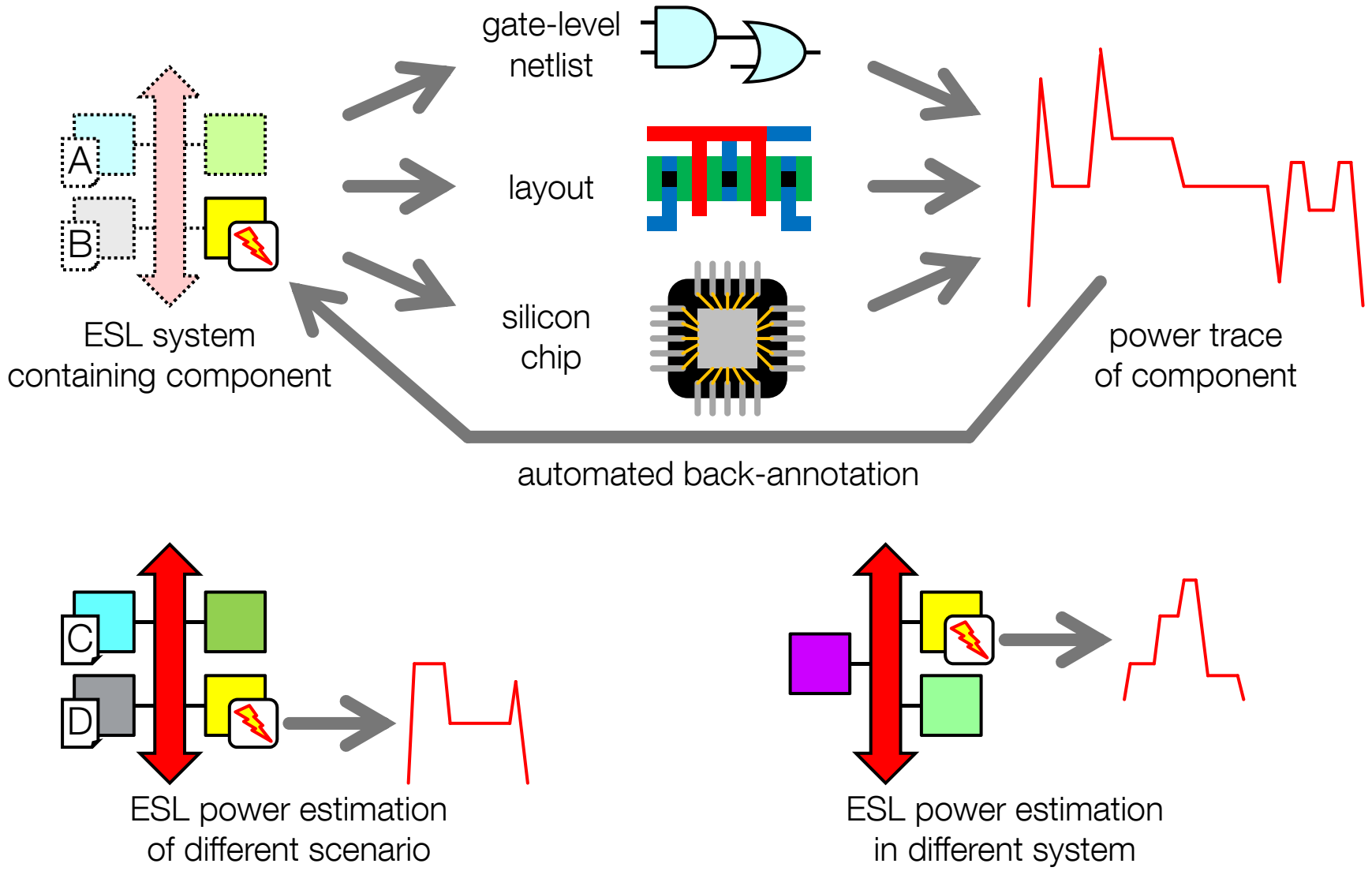
ICE | RWTH AACHEN UNIVERSITY

Motivation



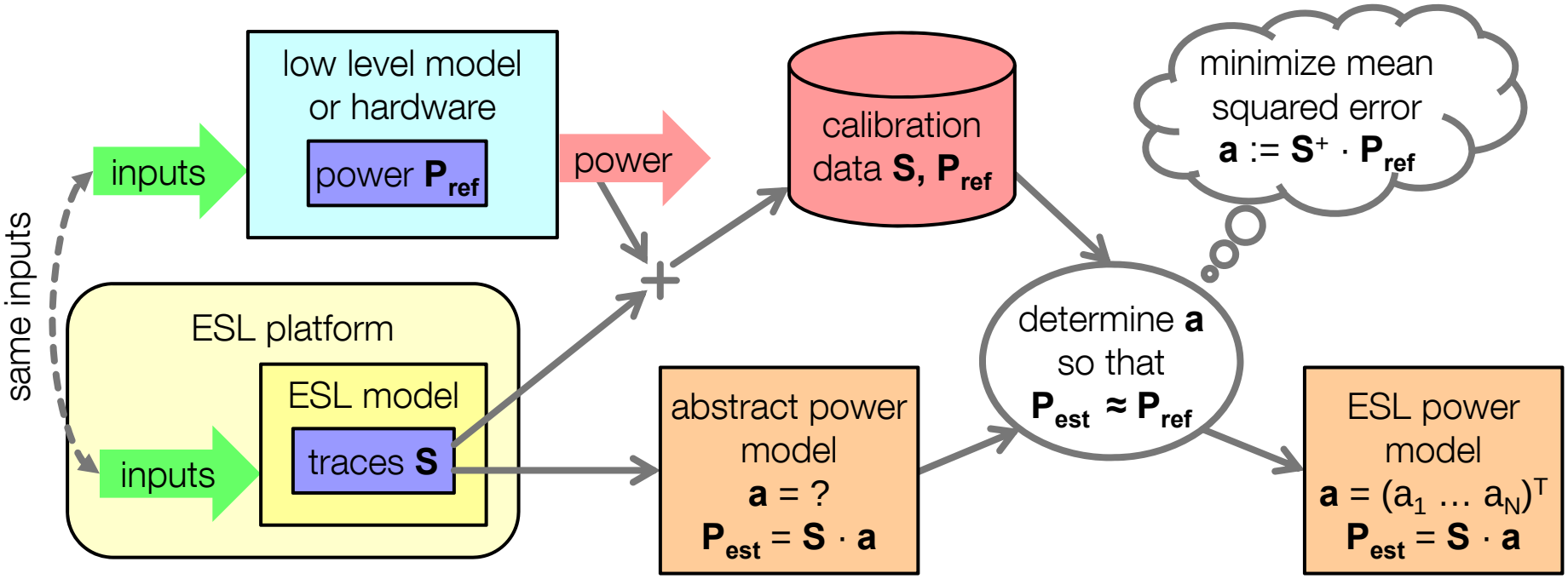
➔ Make fast, early power estimates available for architecture and SW mapping exploration

ESL Power Estimation Methodology



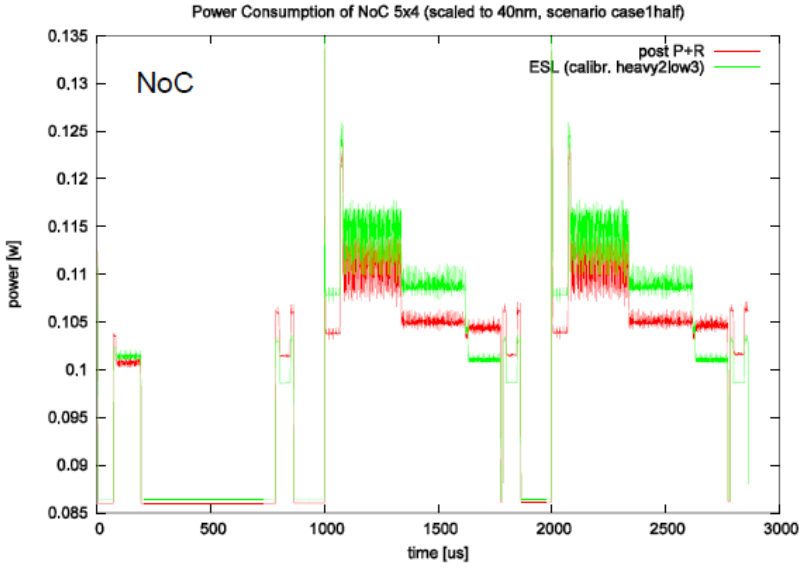
Basic Power Model Calibration Flow

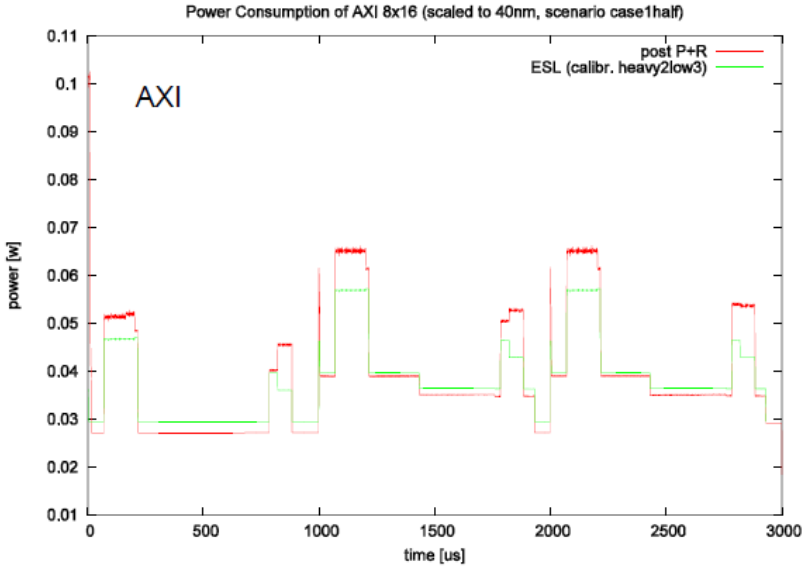
- Run low level model and ESL model with same inputs/benchmarks
- Record ESL states and reference power as calibration data
- Assume linear power model
  - Determine power model factors **a** with best fit



NoC power estimation [MPSoC 2013]

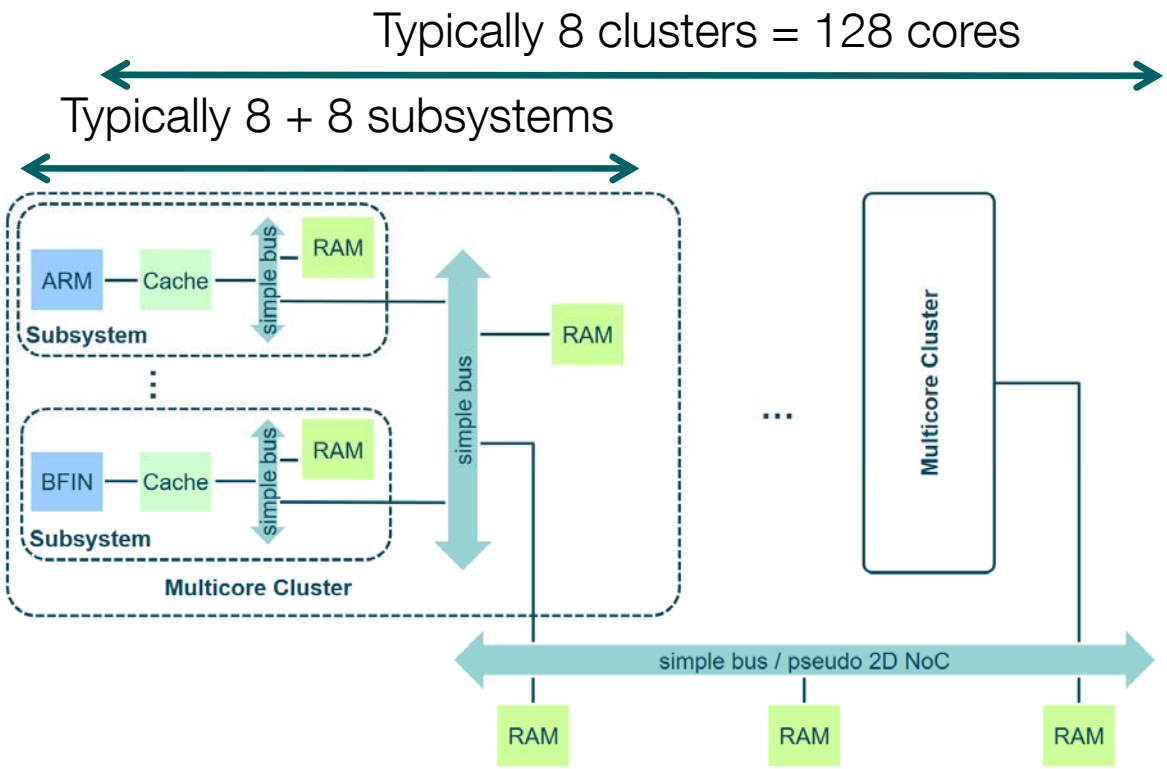
- ESL power estimation methodology initially for AMBA AXI and complex custom NoC at VLSI layout level (post P&R)
- Estimation error < 22%
- Can predict different „power phases“ correctly
- 900x faster than low-level power simulation





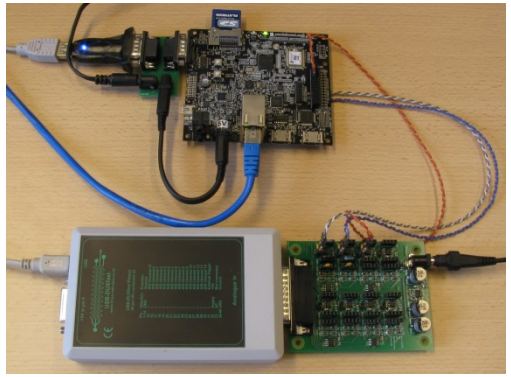
Power estimation for clustered multicore system

- Need fast and accurate processor core power estimation
- ARM A9:
  - White box approach using instrumented simulator, e.g. gem5
  - Black box approach using OVP simulator and TLM traces
- Blackfin 609 DSP:
  - Black box approach

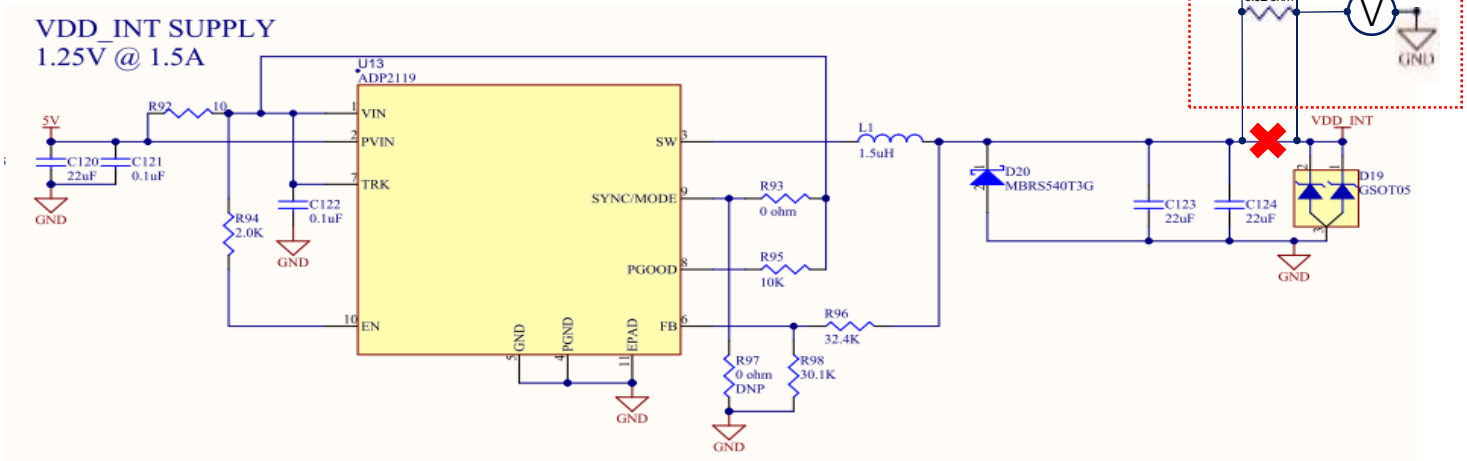


Reference systems for calibration/measurement

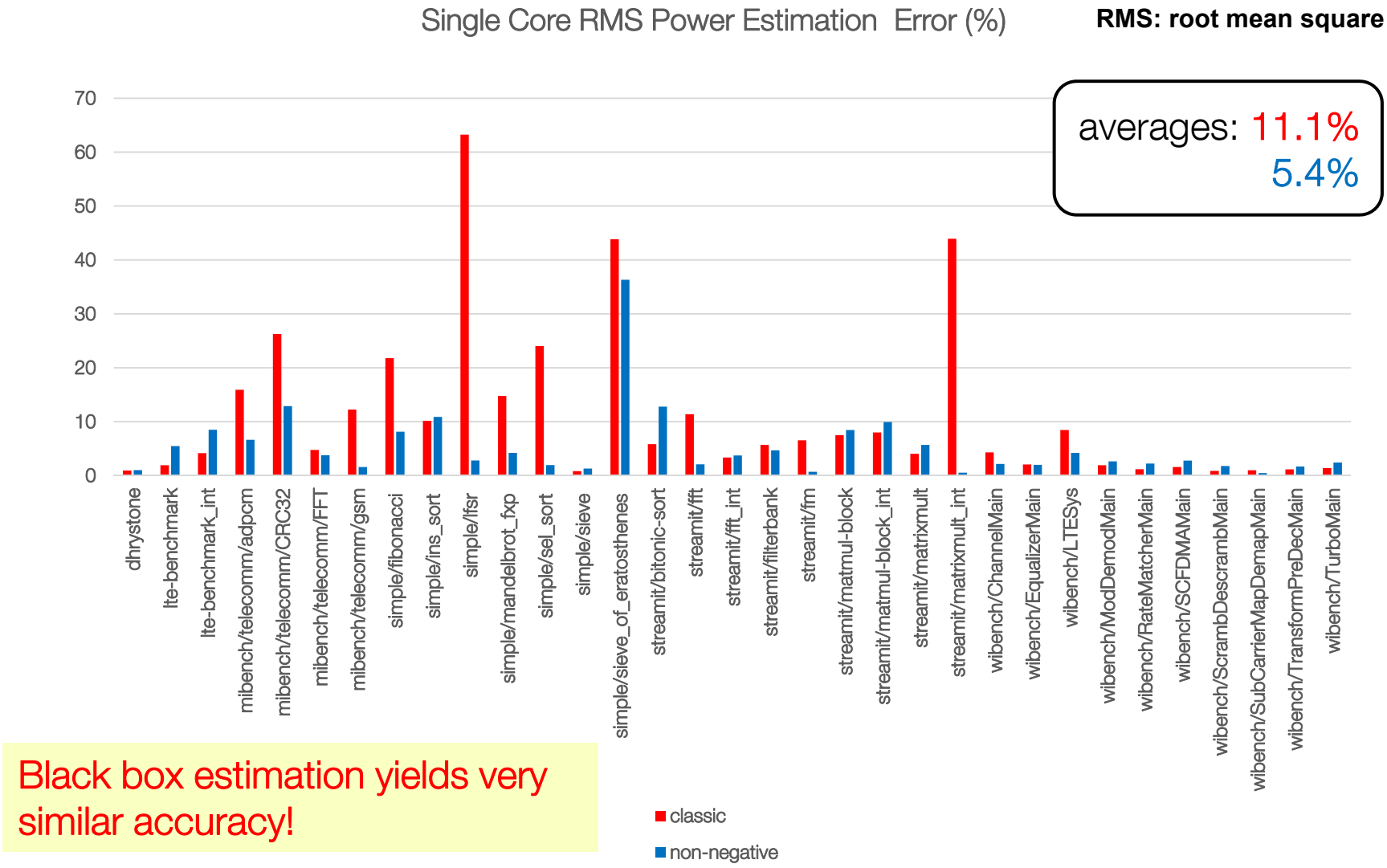
- PandaBoard ES
  - TI OMAP4430
    - ARM Cortex-A9 dual-core (one active)
- FinBoard
  - Analog Devices Blackfin 609 processor
    - 500 MHz dual-core DSP (one active)
- Power Measurement (FinBoard)



modifications for power measurement

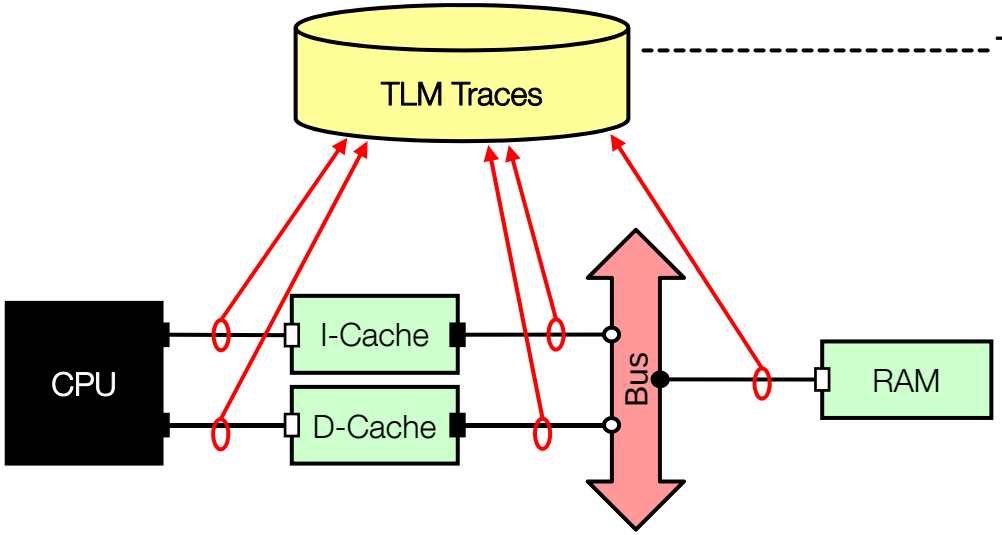


ARM white box estimation results



Black box estimation yields very similar accuracy!

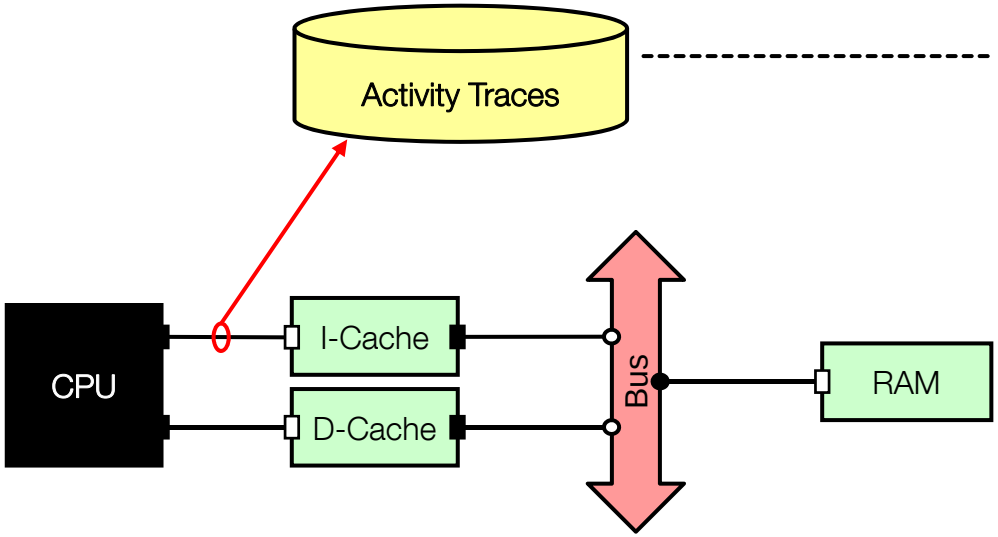
Tracing for Black Box estimation



Traced TLM transactions

- Core running state
- Number of read words
- Number of written words

~10% sim. time overhead



Traced activity

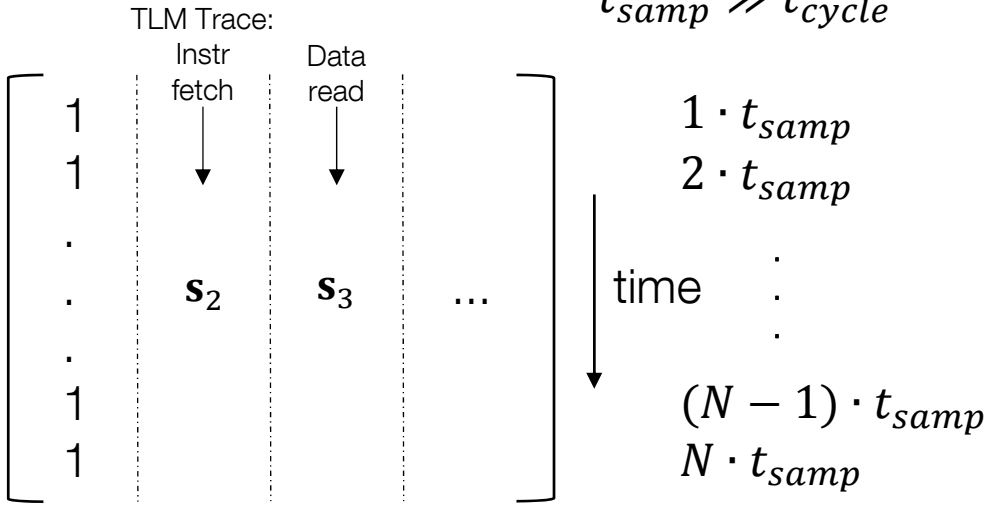
- Look at fetches
- Sleep on IDLE
- Wakeup on every other instruction

< 1% sim. time overhead

Linear Power Model

e.g. 200µs e.g. 2ns

$t_{samp} \gg t_{cycle}$



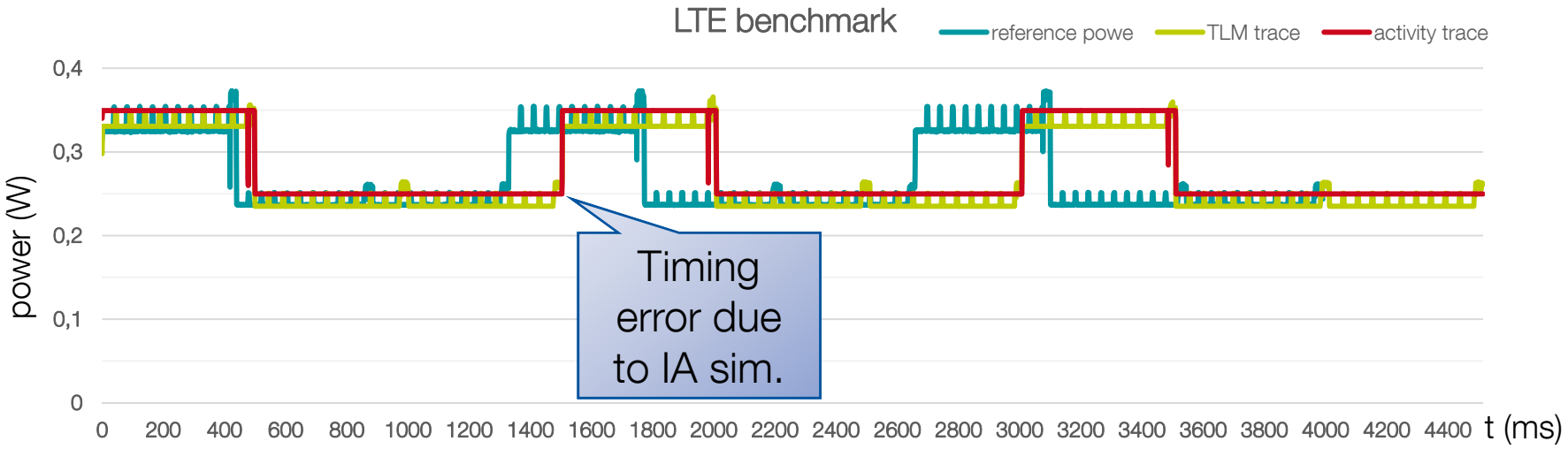
Power factors $\mathbf{a}$ = $\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ . \\ . \end{bmatrix}$

$$\mathbf{P}_{est} = \mathrm{a}_1 + \mathbf{s}_2 \cdot a_2 + \mathbf{s}_3 \cdot a_3 + \cdots$$

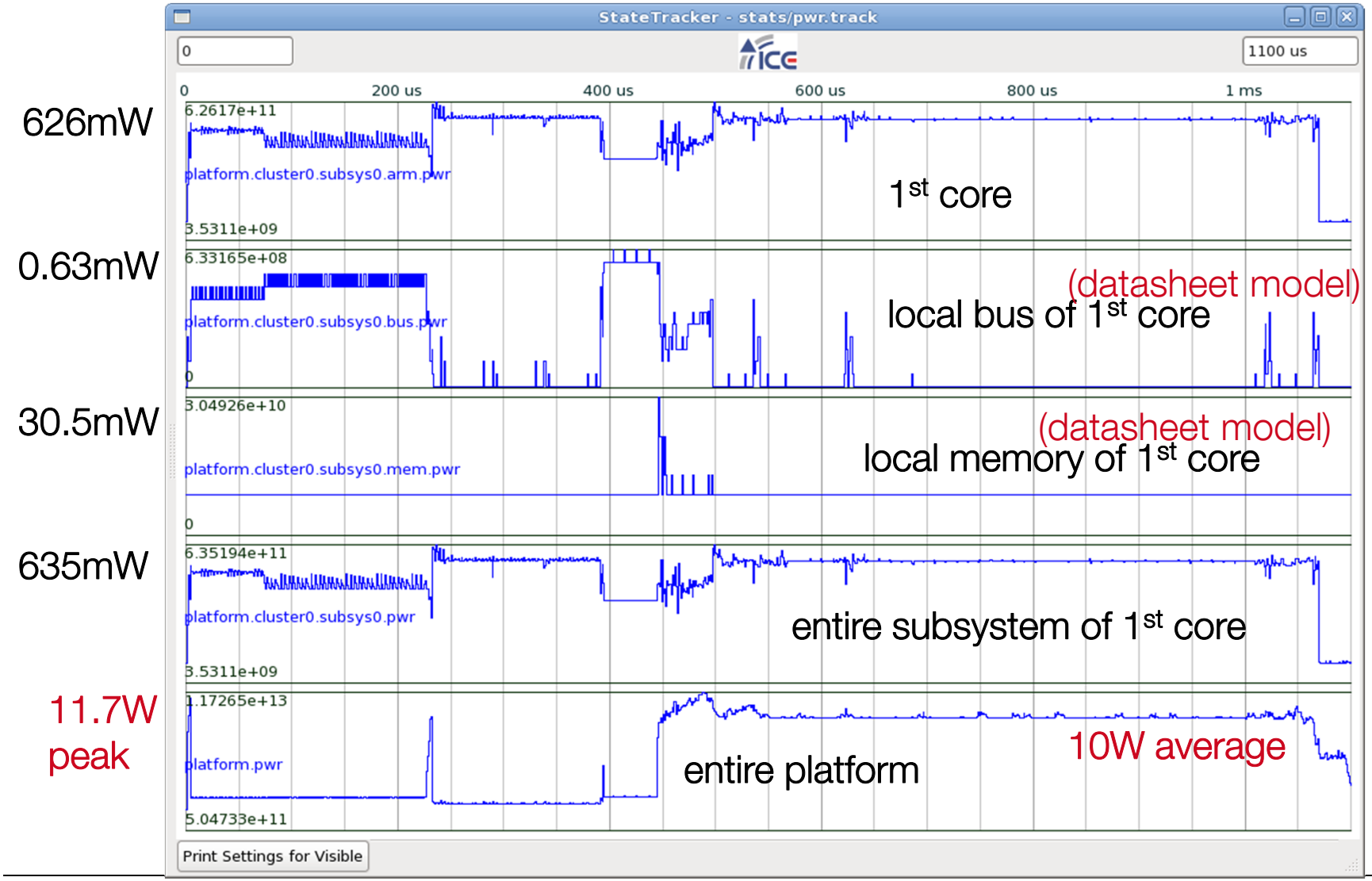
– $\mathbf{P}_{est} = \mathbf{S} \cdot \mathbf{a}$; $\mathbf{a} = \underset{\mathbf{x}}{\operatorname{argmin}} \|\mathbf{S} \cdot \mathbf{x} - \mathbf{P}_{ref}\|_2$

Dual-core Blackfin 609 DSP case study

- ESL: SystemC virtual platform with instruction-accurate processor model from gdb-utils
- TLM trace estimation error: 0.2 – 16%, on average: 2.4%
- Activity trace estimation error: 0.5 – 19%, on average: 4.1%

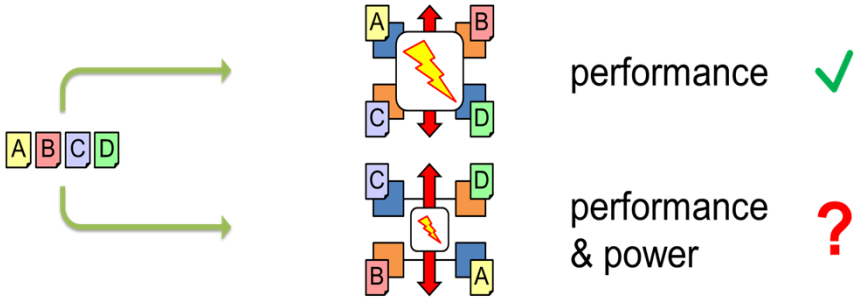


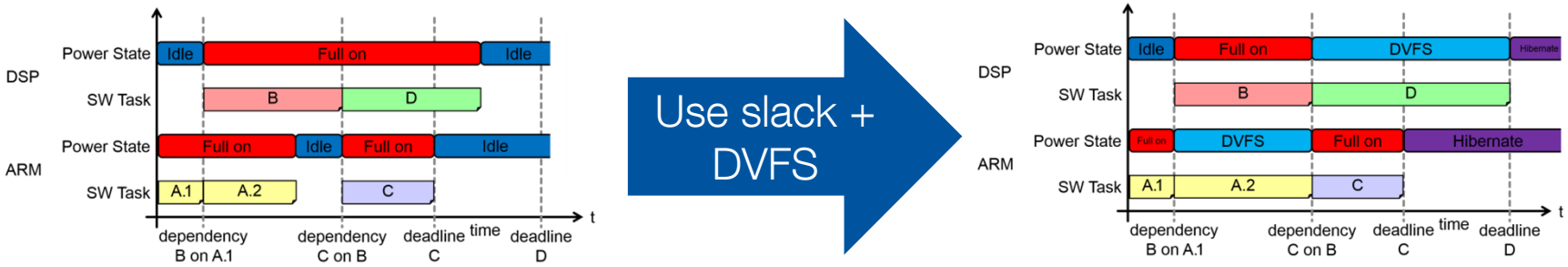
ESL power estimation for multicore cluster



Towards SW-in-the-loop power optimization

- Explore different spatial task mappings
- Optimize temporal task mapping





- Integration into Silexica´s SLX multicore programming tool suite
- See presentation by W. Sheng

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multicore meets simplicity

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Thank you!

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