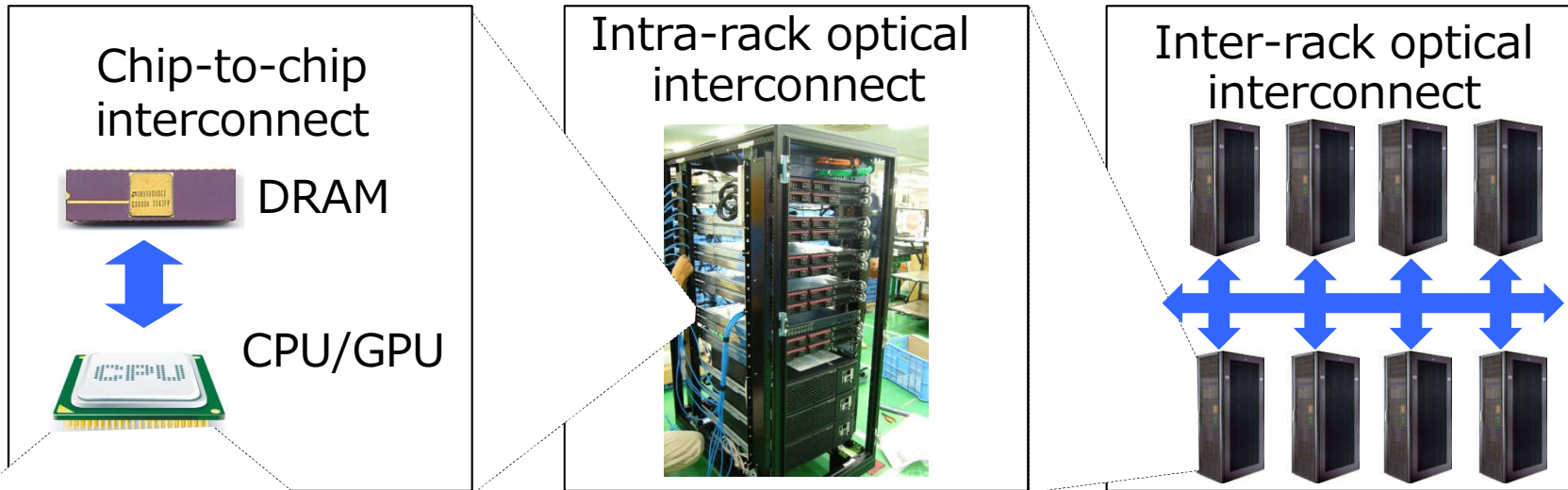# An Integrated Optical Parallel Adder: A First Step towards Light-Speed Data Path Operation
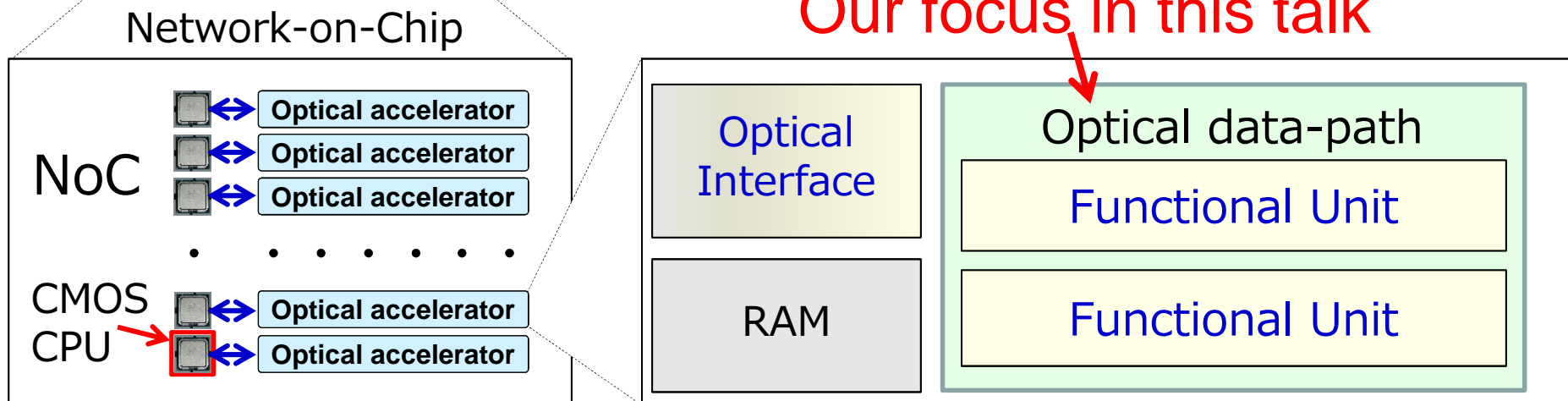
Tohru ISHIHARA

Kyoto University

This work is done in collaboration with NTT Nanophotonics center and Kyushu University
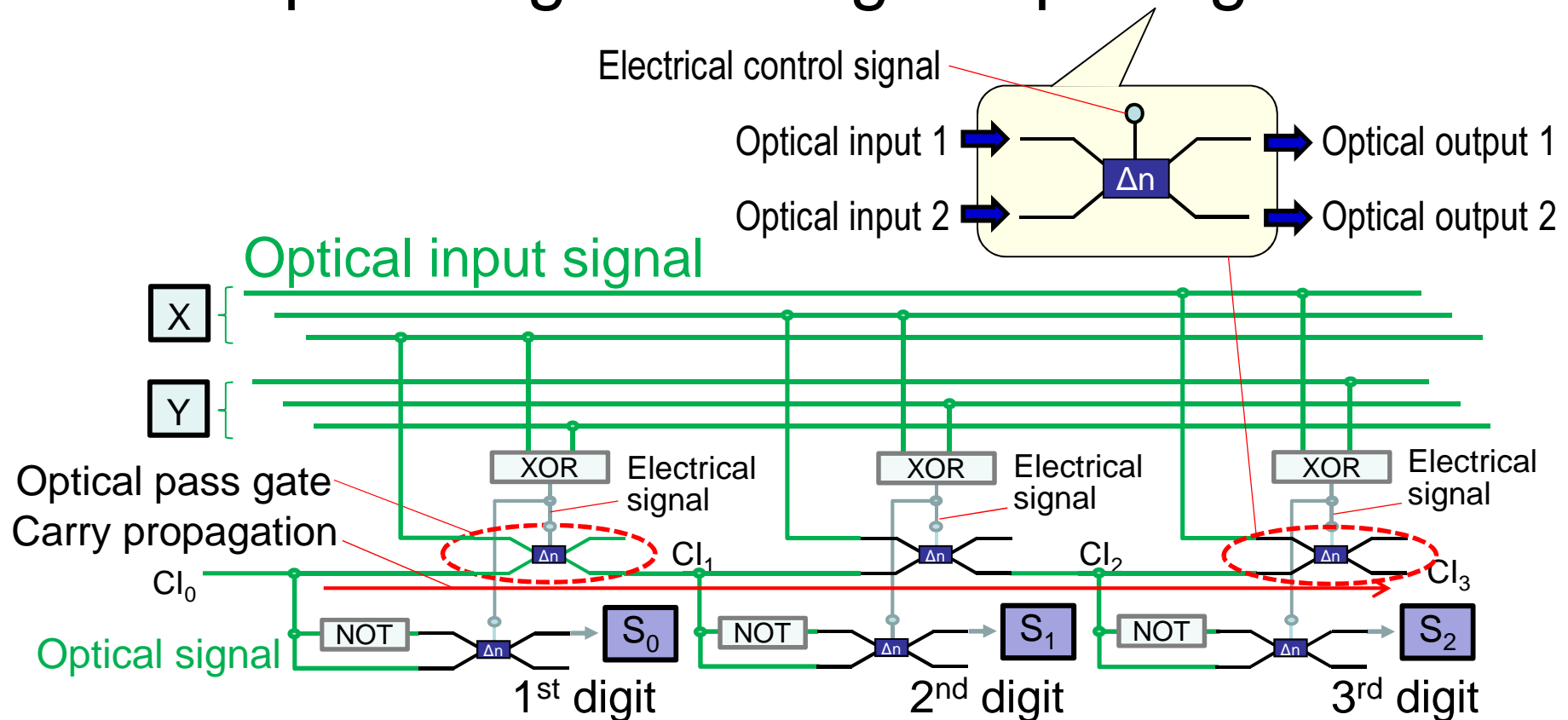
Beyond Optical Communication

Chip-to-chip interconnect

DRAM

CPU/GPU

Intra-rack optical interconnect

Inter-rack optical interconnect

Network-on-Chip

NoC

Optical accelerator
Optical accelerator
Optical accelerator

CMOS
CPU

Optical accelerator
Optical accelerator

Our focus in this talk

Optical Interface

RAM
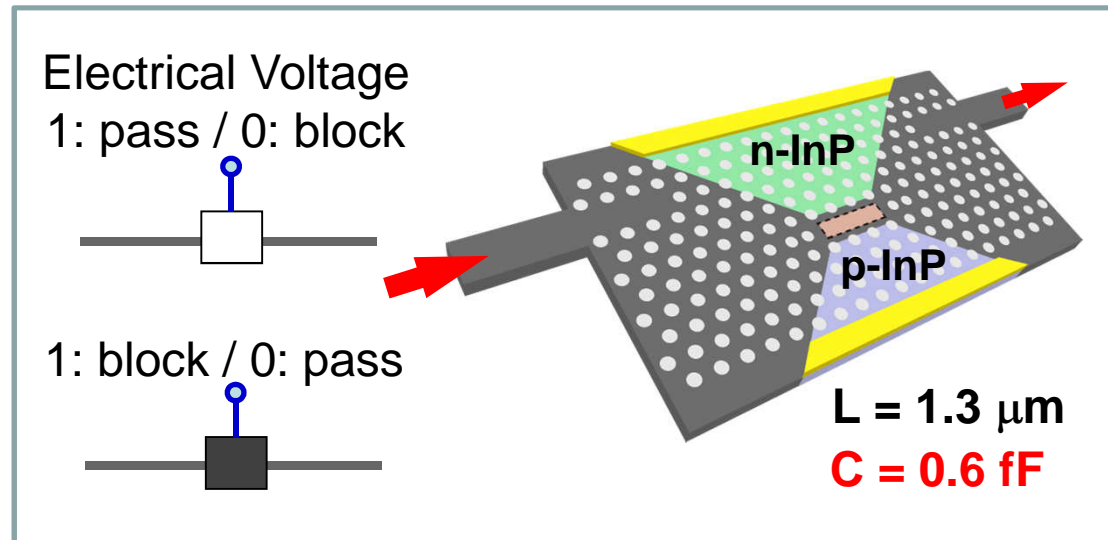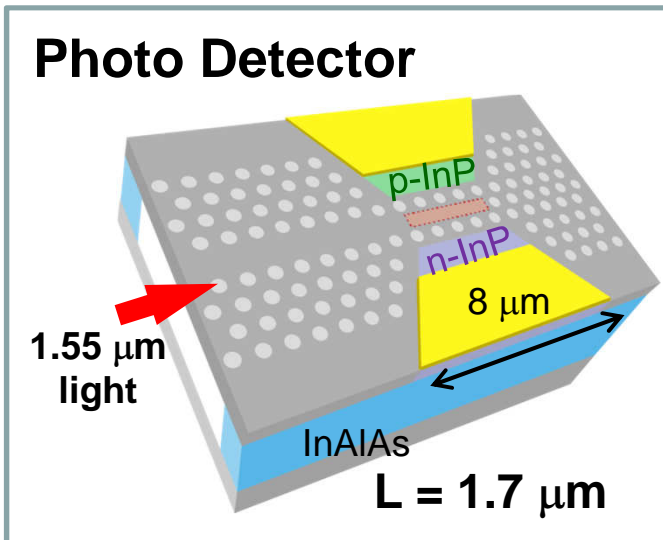
Optical data-path

Functional Unit

Functional Unit

2

Why Optical Data Path?

- Computation can be done by just passing the optical signal through a "pass gate"

Electrical control signal

Optical input 1 → → Optical output 1

Δn

Optical input 2 → → Optical output 2

Optical input signal

X

Y

Optical pass gate
Carry propagation

XOR   Electrical signal
XOR   Electrical signal
XOR   Electrical signal

CI_0 CI_1 CI_2 CI_3

Δn Δn Δn

Optical signal

NOT Δn S_0
NOT Δn S_1
NOT Δn S_2

1st digit 2nd digit 3rd digit

Optical Pass Gate

Electrical Voltage Control
1: pass / 0: cross

Optical signal → Δn → Optical signal

Directional Coupler

Targeting
100 μm or less

Photo Detector

p-InP

n-InP

8 μm

1.55 μm
light

InAlAs

L = 1.7 μm

Electrical Voltage
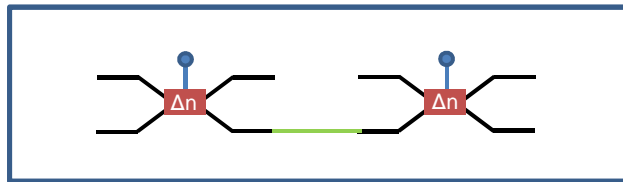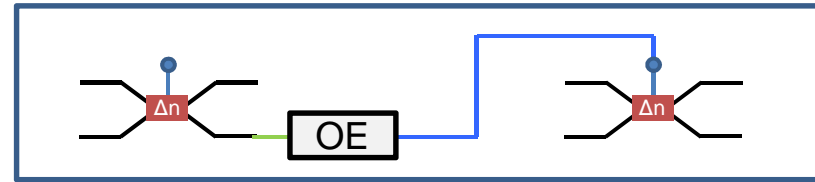1: pass / 0: block

1: block / 0: pass

n-InP

p-InP

L = 1.3 μm
C = 0.6 fF

4

Why Optical PG for Data Path?

- Good at data path operation

  ✓ Light speed operation
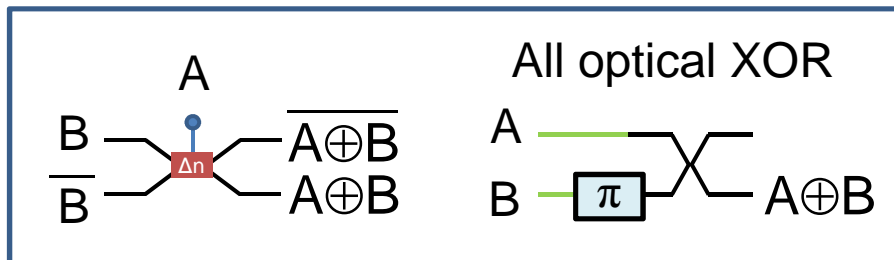

Good at serial connection (light speed)

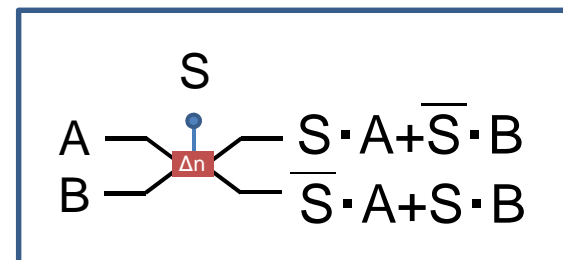NOT good at cascade connection (OE & switching delay involved)
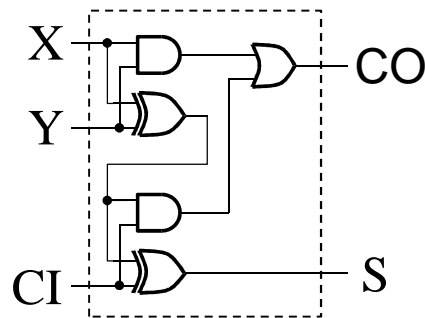
  ✓ Good at pass/cross propagations (XOR and MUX)

XOR

MUX

All optical XOR

$$\overline{A \oplus B}$$
$$A \oplus B$$

$$B \xrightarrow{\pi} A \oplus B$$

$$S \cdot A + \overline{S} \cdot B$$
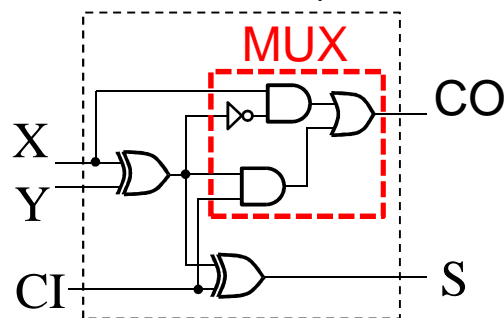$$\overline{S \cdot A + S \cdot B}$$

Arithmetic Operation with OPG

- ## XOR/MUX-dominant data-path operation

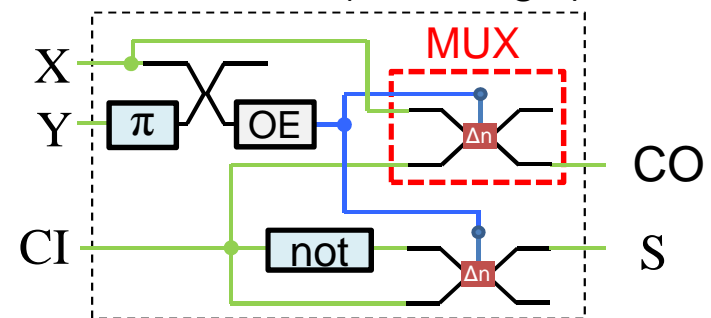 ✓ Parallel Adder, Multiplier, and Barrel Shifter etc.

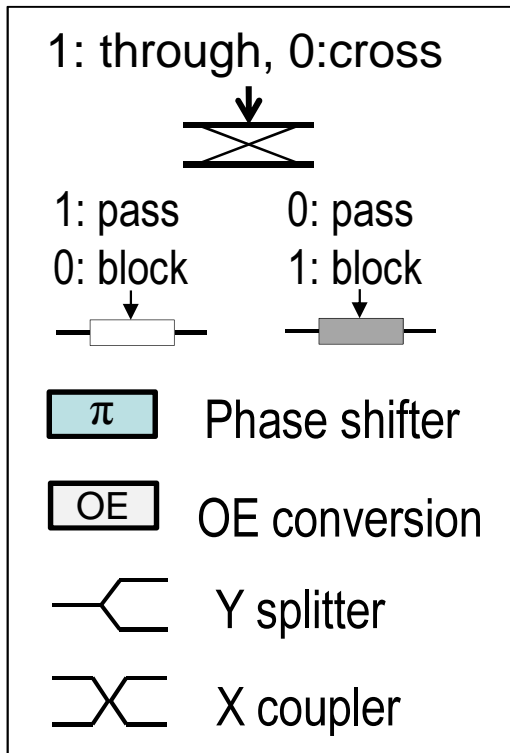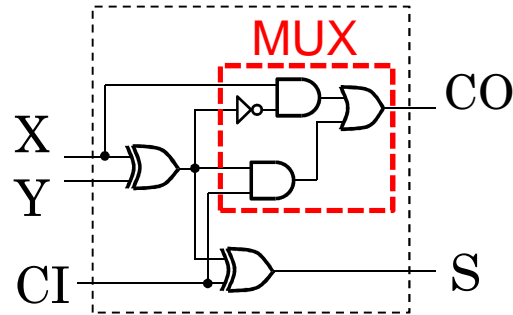Full Adder (AOI logic)   Full Adder (modified)   Full Adder (OPG logic)

  ✓ Parallel adder as a first step

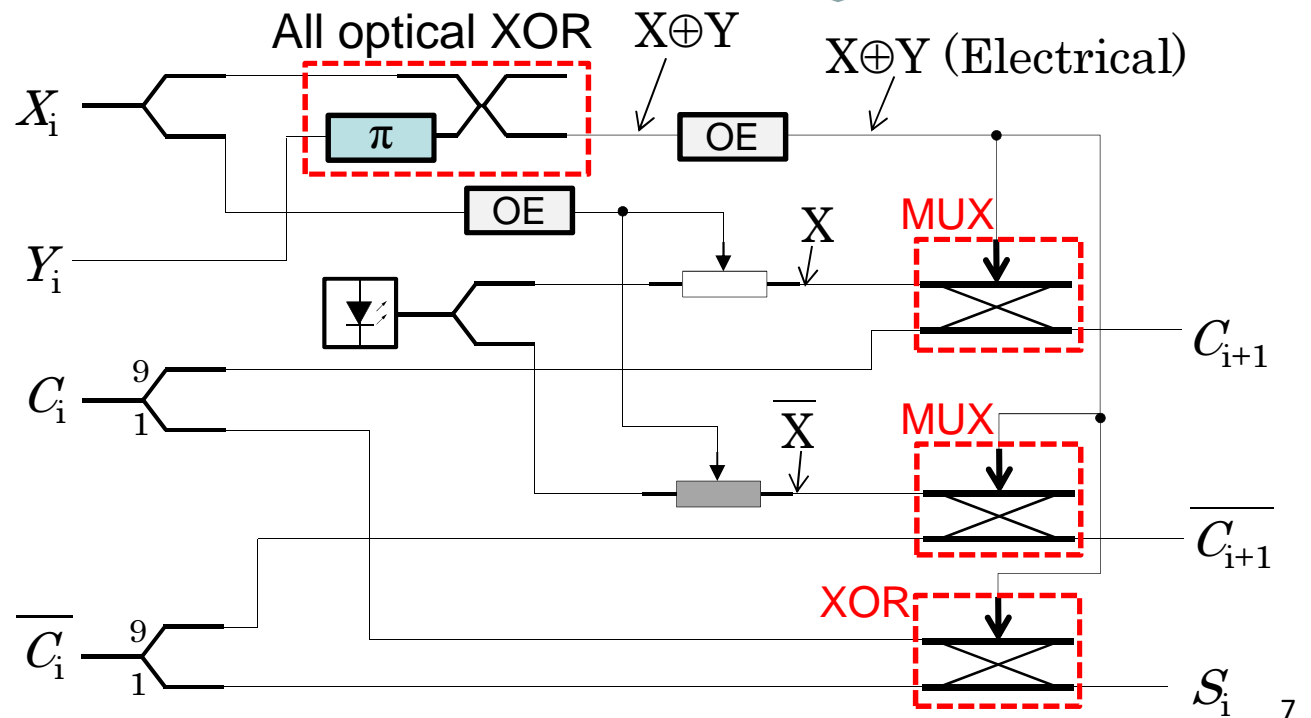 ➢ Can be constructed with serial connections only

Optical Full Adder
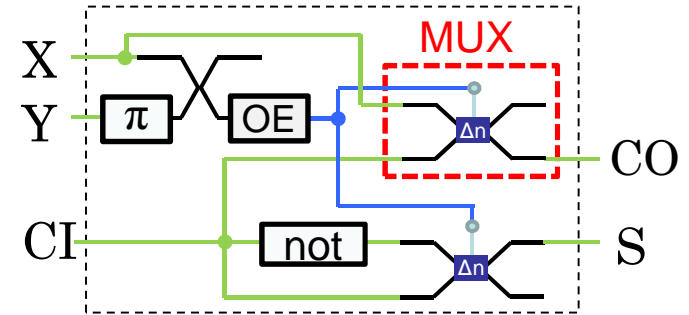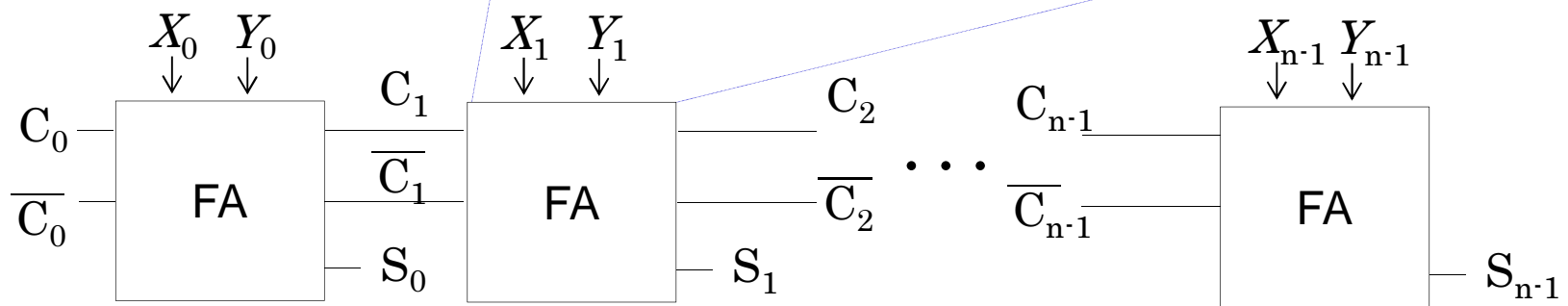

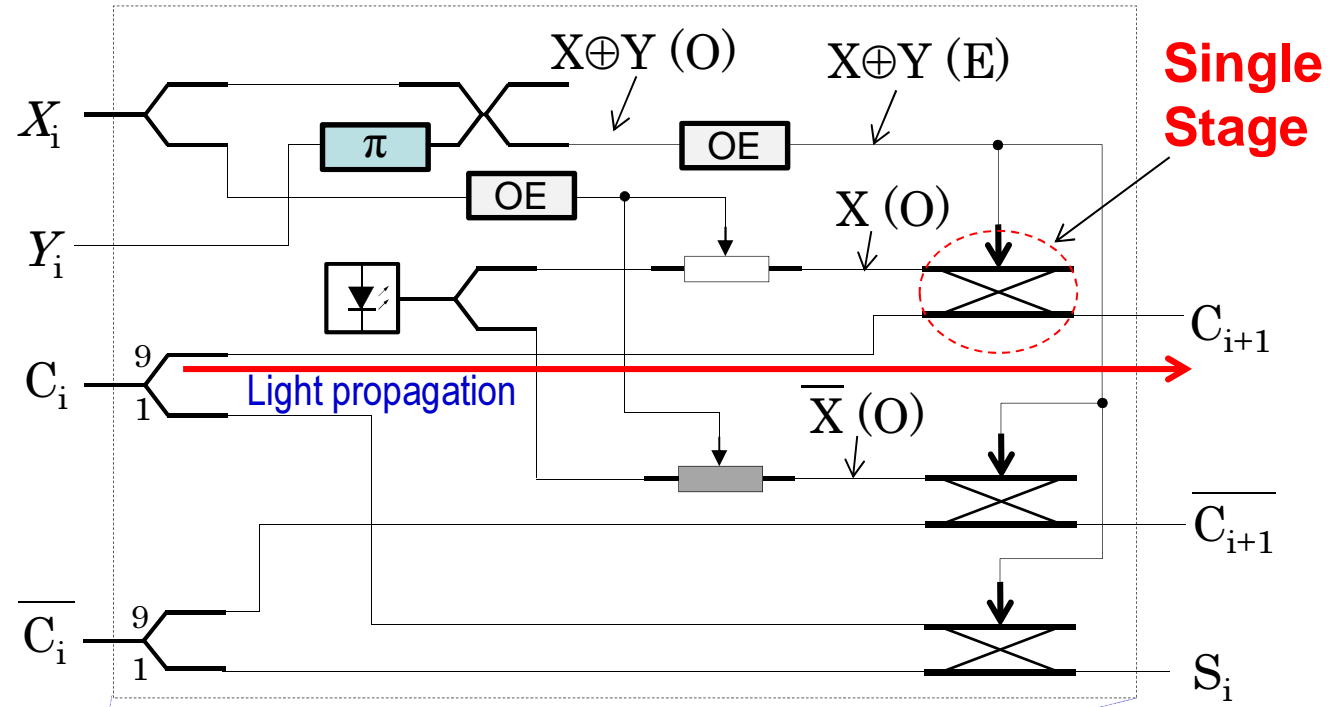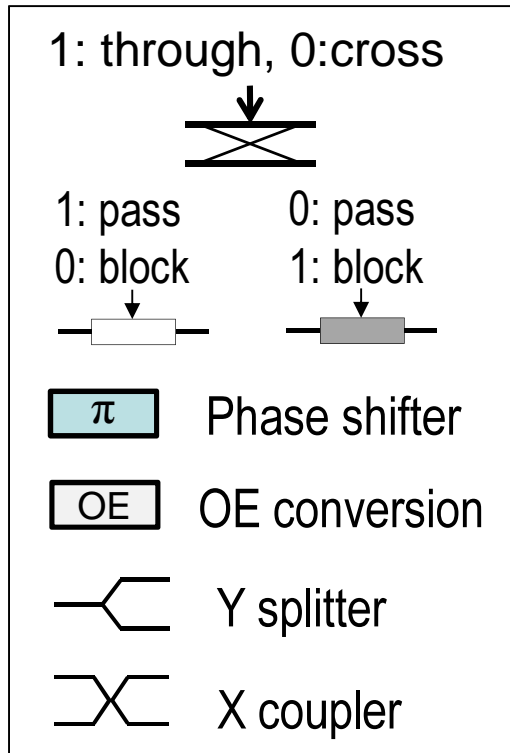Library Cells in OptiSPICE simulator (Optoelectronic circuit simulator)

Full Adder (AOI logic)

Full Adder (OPG logic)

1: through, 0:cross

1: pass   0: pass
0: block   1: block

π Phase shifter

OE   OE conversion

Y splitter

X coupler

All optical XOR

X⊕Y

X⊕Y (Electrical)

MUX

XOR

Design and Evaluation: 8-bit Adder

1: through, 0:cross

1: pass   0: pass
0: block   1: block

π Phase shifter

OE   OE conversion

Y splitter

X coupler

X_i

Y_i

C_i

$\overline{C_i}$

$X \oplus Y$ (O) $X \oplus Y$ (E)

X (O)

$\overline{X}$ (O)

Single Stage

Light propagation

C_{i+1}

$\overline{C_{i+1}}$

S_i

X_0 Y_0 X_1 Y_1 X_{n-1} Y_{n-1}

C_0 ── FA ── C_1 ── FA ── C_2 · · · C_{n-1} ── FA

$\overline{C_0}$ ──── $\overline{C_1}$ ──── $\overline{C_2}$ $\overline{C_{n-1}}$

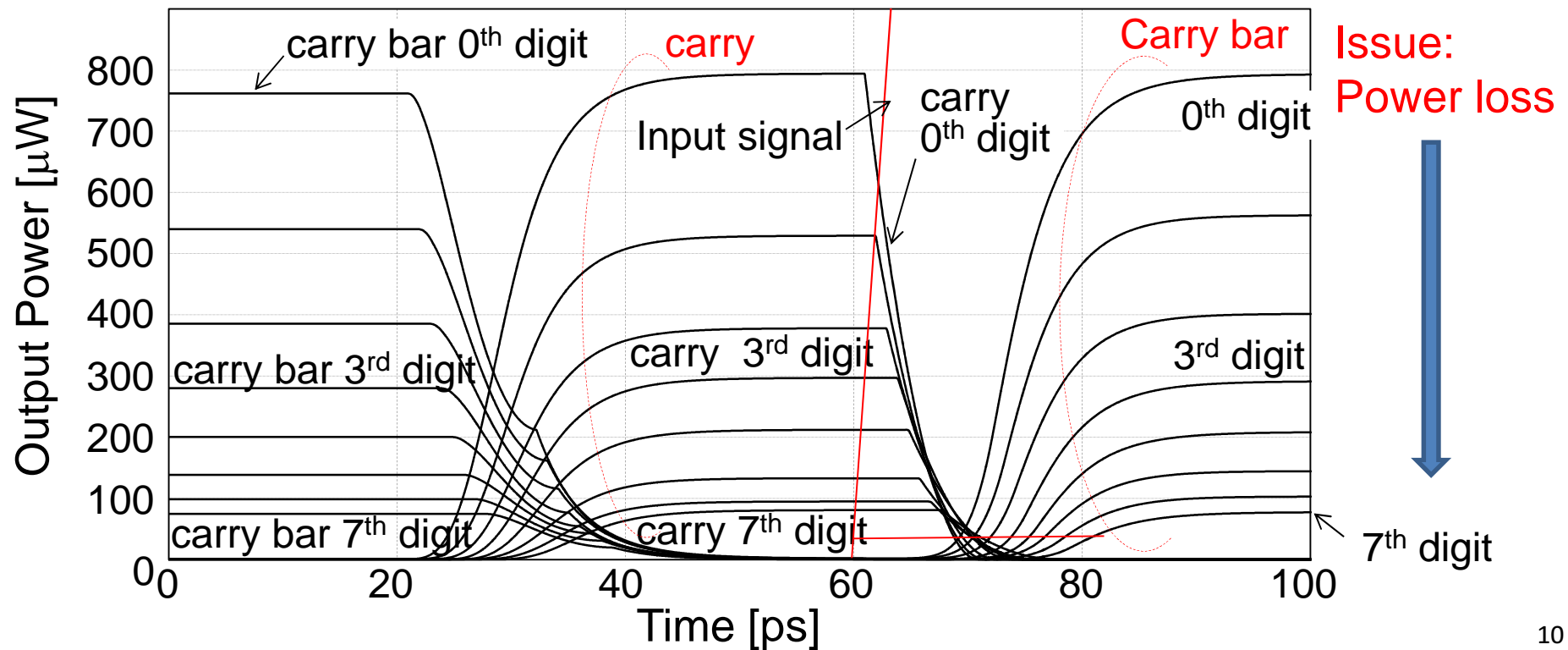── S_0 ── S_1 ── S_{n-1}

8

8-bit CMOS Adder as Comparison

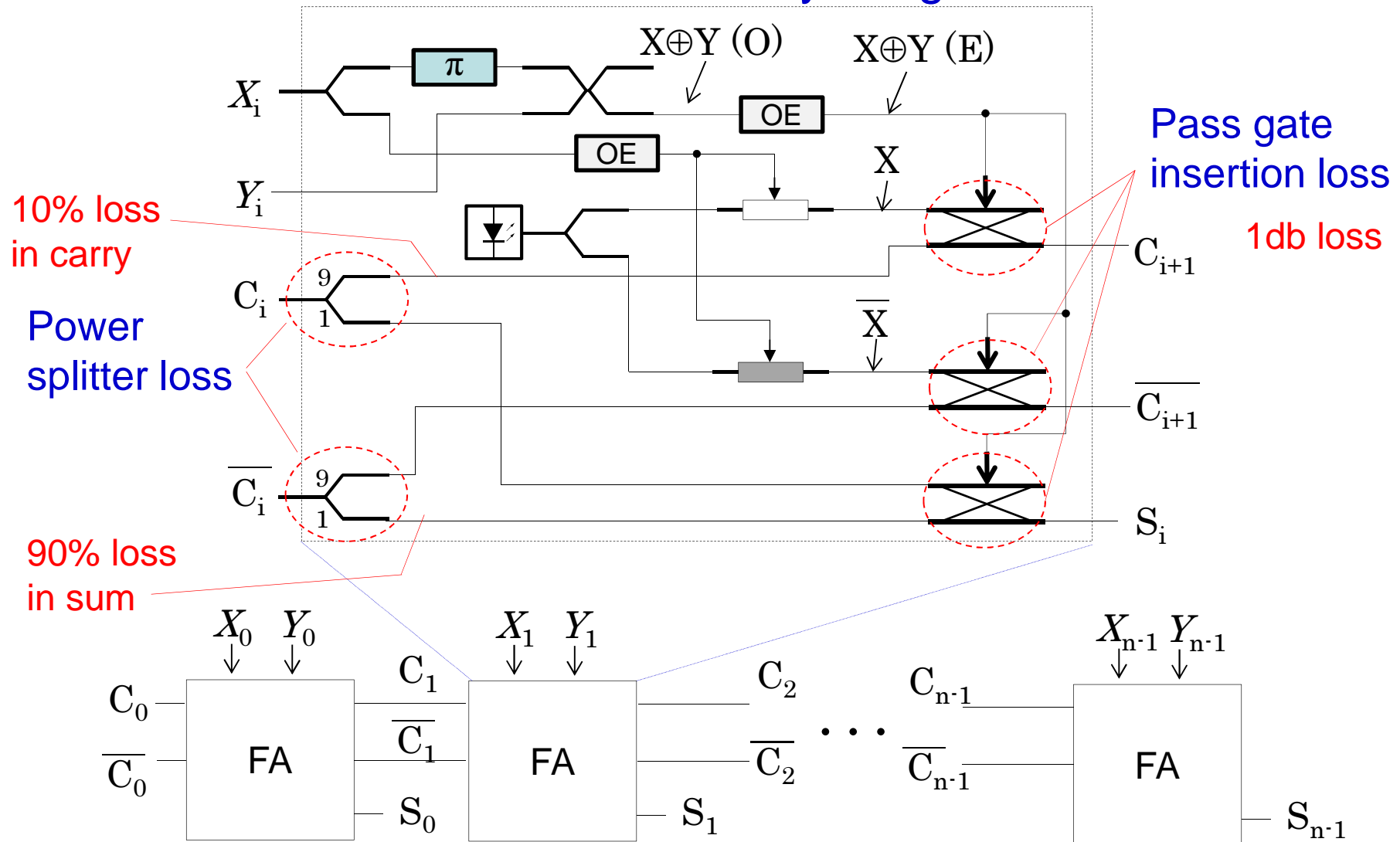16 nm High Performance CMOS Technology PTM
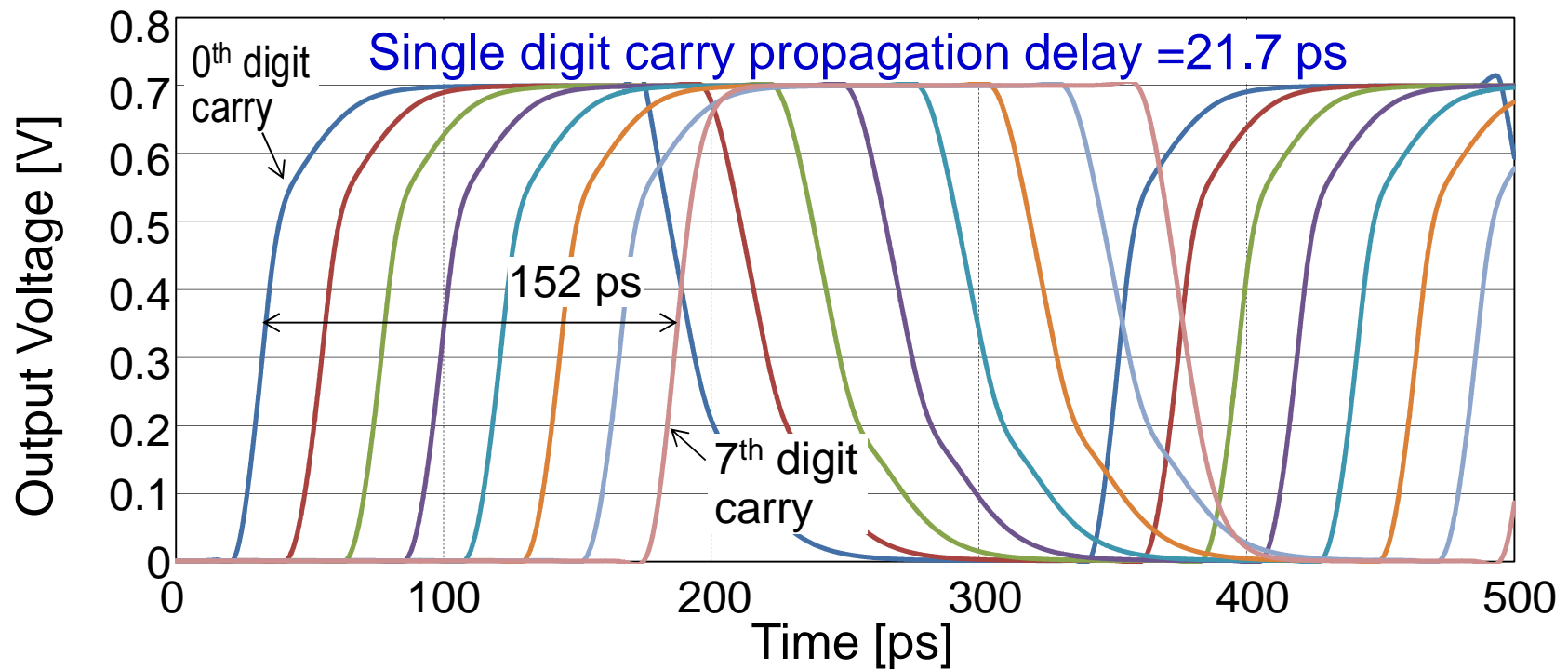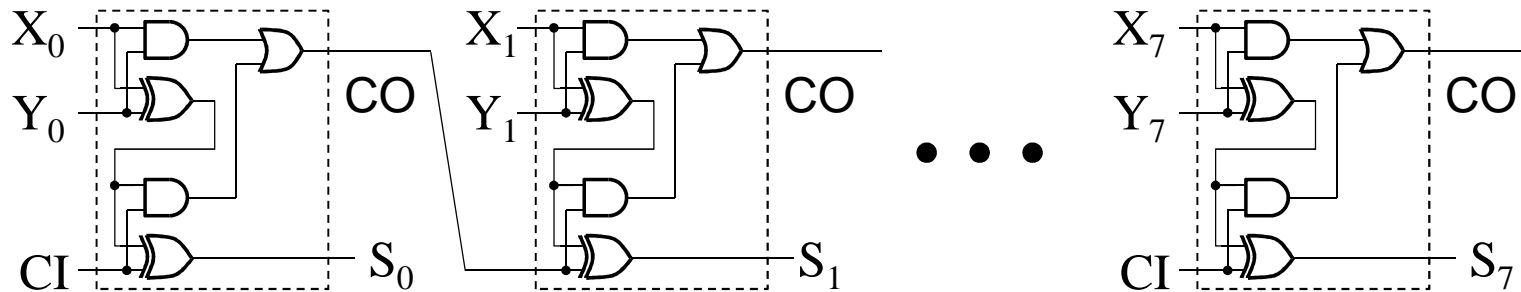
Results of OptiSPICE Simulation

➢ Optoelectronic Circuit Simulator (HSPICE engine)

➢ Light-speed parallel adder operation confirmed

- Per stage delay: ~1ps, Initial OE and switching delay: ~10ps

- 8-bit CMOS adder with 16nm HP PTM: 174 ps

Power Loss in Adder Operation

Power halves every 2 digits

Summary

- 8-bit parallel adder is designed with OPG
- Light-speed operation is confirmed
  - Per digit delay: OPG ~1 ps, CMOS 22 ps
  - 8-bit total delay: OPG ~17 ps, CMOS 174 ps
- Power loss is big issue to be resolved
  - Per digit power loss ~30%

- Future work
  - Extend it to more complicated functions