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# What does power management bring for heterogeneous MPSoCs?

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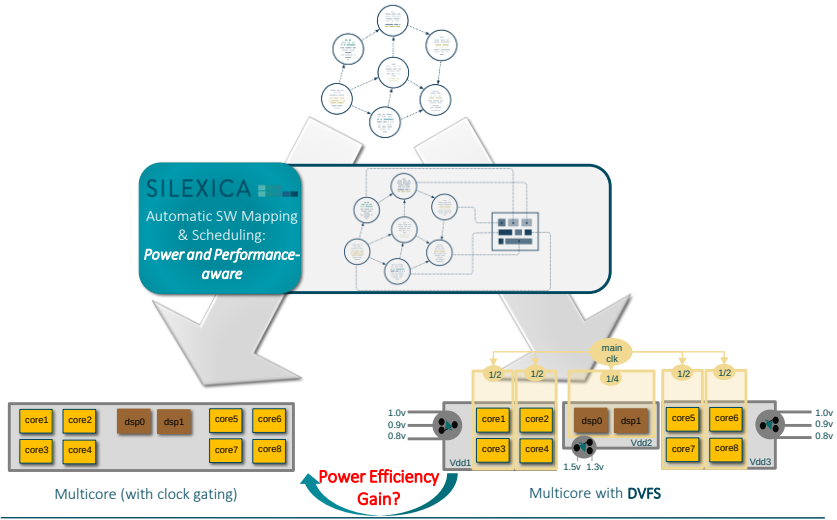
## Problem Statement

*Identify the **power efficiency gain** from the sophisticated power management (DVFS) in multicore SoCs*



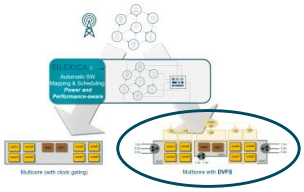
# Outline

- Preparations / Prerequisites
  - Architectural modeling with power models
  - Automatic SW Mapping & Scheduling extension towards power-aware
- Results



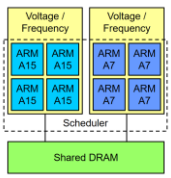
# Architectural modeling with power models

- ESL power model and methodolody for processors
  - Case Studies: ARM Cortex A9, Blackfin 609
    - ➢ Power estimation error <5%
  - Further investigations on methodoloy robustness

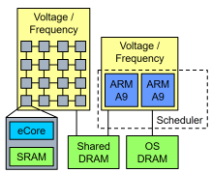


*How to describe the multicore SoC architecture **with performance and power models**?*

- Extend SLX architecture description model
  - Frequency / Voltage Domains
  - Processor models
  - ...




Samsung Exynos 5 Octa




Adapteva Parallella

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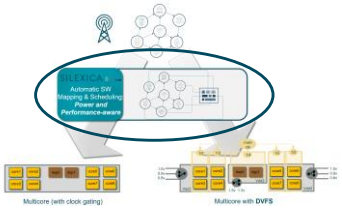
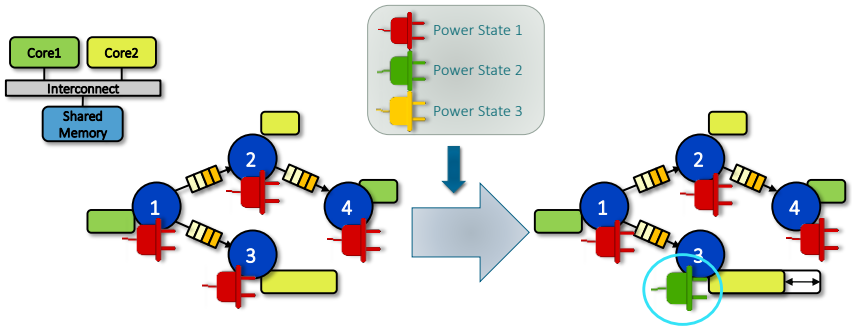
# Automatic SW Mapping & Scheduling extension towards power-aware

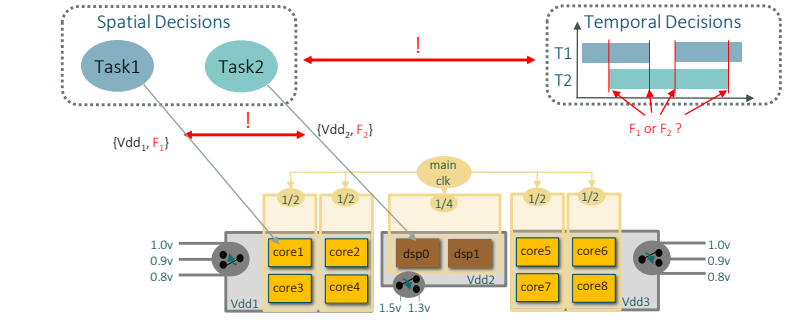



*Extend the automatic SW Mapping & Scheduling by adding **heuristics** that are both performance- and **power-aware***



## A Word on Voltage and Frequency Domains Complexity

- Typical mapping heuristics are developed towards static (compile-time) mapping, e.g.
  - Where the task is mapped to;
  - V/F setting for the task.
- **Sophisticated power management** now provides more opportunites but also complexity

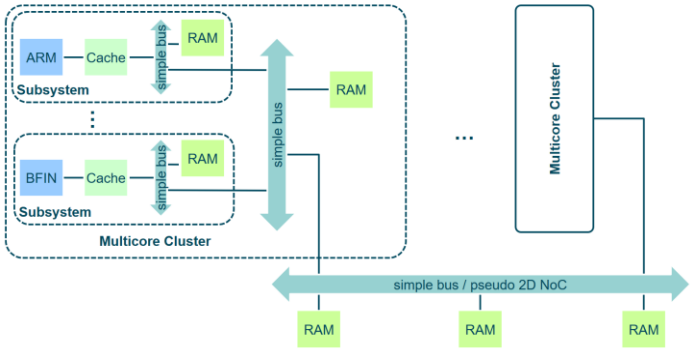





## Outline

- Preparations / Prerequisites
  - Architectural modeling with power models
  - A realistic LTE Benchmark
  - Automatic SW Mapping & Scheduling extension towards power-aware
- Results

# Architecture used in experiments

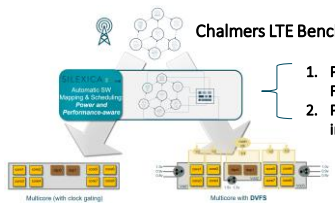



- 4 clusters, each with 4 ARM and 4 BFIN subsystems
- Independent Frequency and Voltage settings per cluster and per core type

| Core Type | Frequency Settings (MHz) | Voltage Settings (V) |
|---|---|---|
| ARM Cortex A9 | [0, 1200], in steps of 100 | [0.91, 1.22], in steps of 0.2 |
| BFIN | [0, 500], in steps of 100 | 1.25 |

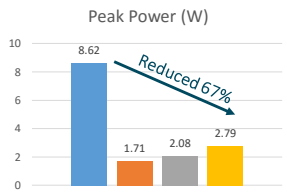


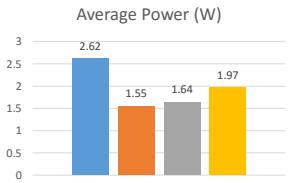
# Results

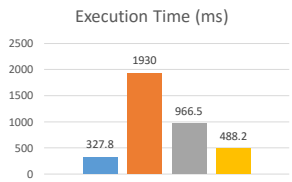


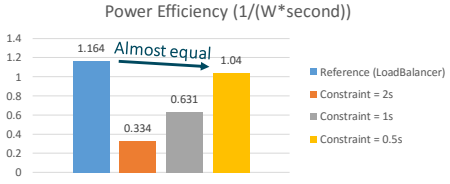
Chalmers LTE Benchmark

1. Performance mapping (LoadBalancer): Fixed Vdd + Clock Gating
2. Power mapping (PowerMinAvg) with a user input on time constraint: DVFS

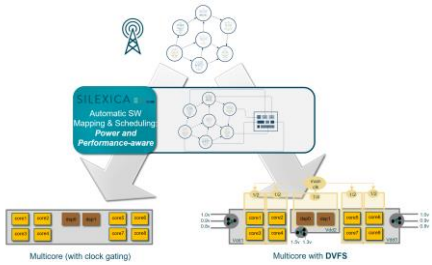


# Summary




- In order to investigate *„Identify the **power efficiency gain** from the sophisticated power management (DVFS) in multicore SoCs“*
  - Architectural modeling with power models: **processor power estimation error < 5%**
  - Automatic SW Mapping & Scheduling extension towards power-aware: **Power-aware heuristics developed in SLX Tools**

→

- ✓ **Peak Power is reduced 67% using DVFS**
- ✓ **Power Efficiency: Using DVFS is on a par with Fixed Vdd + Clock Gating.**
- ✓ **Results are only valid for this case configuration (application + architecture)!**