Information Processing Factory – Conquering MPSoC Complexity with Self-Aware Computing Platforms

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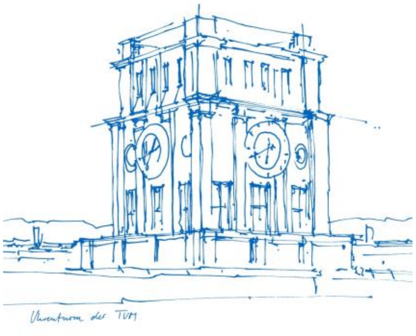
MPSoC Forum 2017



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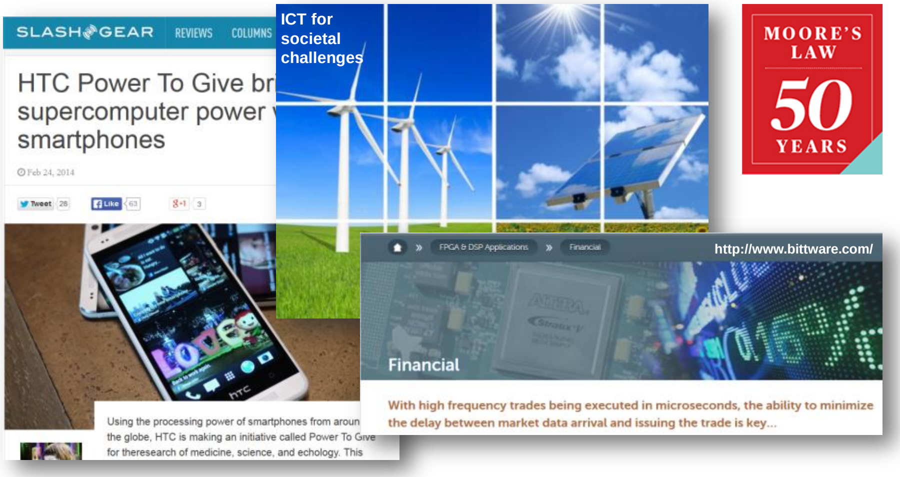
Computing Platform Evolution – The Excitement



SLASH GEAR REVIEWS COLUMNS

HTC Power To Give br
supercomputer power
smartphones

Feb 24, 2014

Using the processing power of smartphones from aroun
the globe, HTC is making an initiative called Power To Give
for theresearch of medicine, science, and echology. This

ICT for societal challenges

http://www.bittware.com/

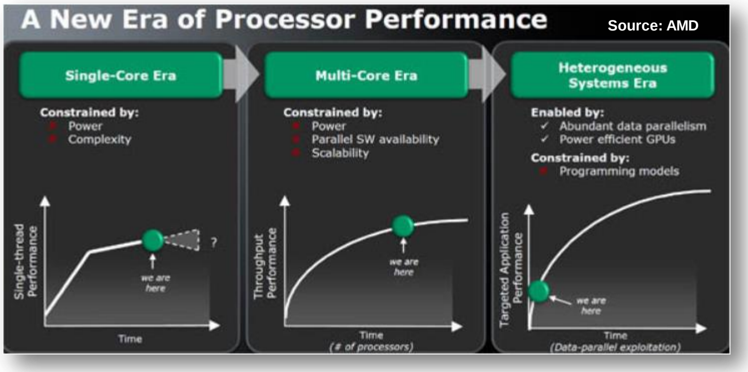
Financial

With high frequency trades being executed in microseconds, the ability to minimize the delay between market data arrival and issuing the trade is key…

Computing Platform Evolution – The Excitement

- Massive increase in terms of number of functions per device and sophistication per application
- Increasing demand for adopting (heterogeneous) multi-cores
- Many different form factors:
  - Compute performance
  - Power / energy budget
  - Safety, Security
  - Hard real-time
  - Reliability
  - Cost

Computing Platform Evolution – The Challenges



A New Era of Processor Performance

Source: AMD

Single-Core Era

Constrained by:
- Power
- Complexity

Multi-Core Era

Constrained by:
- Power
- Parallel SW availability
- Scalability

Heterogeneous Systems Era

Enabled by:
- ✓ Abundant data parallelism
- ✓ Power efficient GPUs

Constrained by:
- Programming models

Computing Platform Evolution – The Challenges

IEEE MICRO, November – December 2005

DESIGNING RELIABLE SYSTEMS FROM UNRELIABLE COMPONENTS: THE CHALLENGES OF TRANSISTOR VARIABILITY AND DEGRADATION

Shekhar Borkar
Intel Corp.

AS TECHNOLOGY SCALES, VARIABILITY IN TRANSISTOR PERFORMANCE WILL CONTINUE TO INCREASE, MAKING TRANSISTORS LESS AND LESS RELIABLE.

Appears in the Proceedings of the 38th International Symposium on Computer Architecture (ISCA '11)

Dark Silicon and the End of Multicore Scaling

Hadi Esmaeilzadeh† Emily Blem‡ Renée St. Amant§ Karthikeyan Sankaralingam‡ Doug Burger*
†University of Washington ‡University of Wisconsin-Madison
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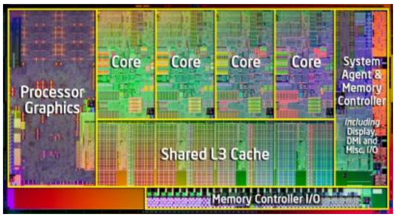
Heterogeneity ⇔ Complexity



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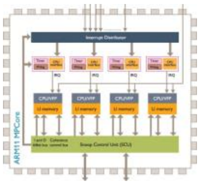
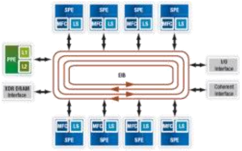
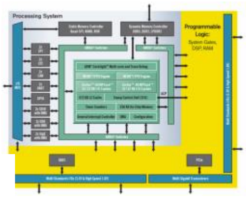
Intel Core i7 (Sandy Bridge)



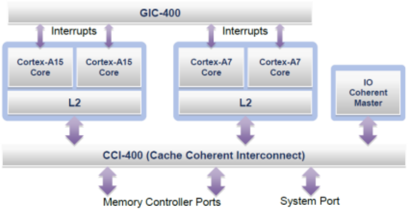
ARM MPcore



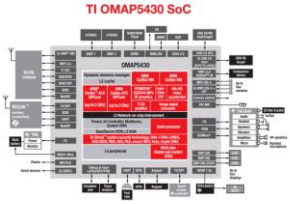
IBM CELL



XILINX Zynnc



ARM Big.LITTLE



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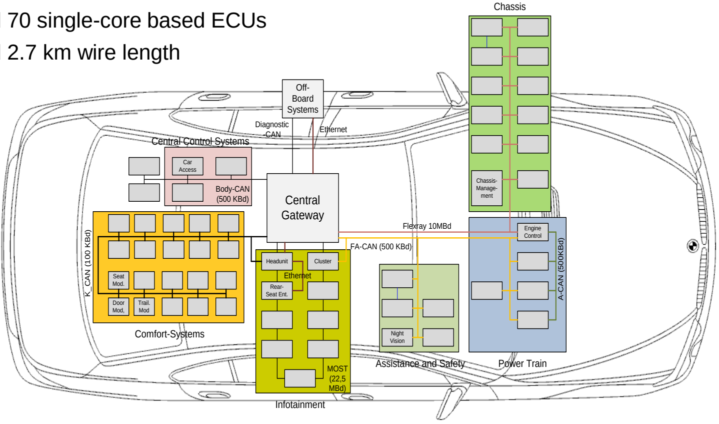
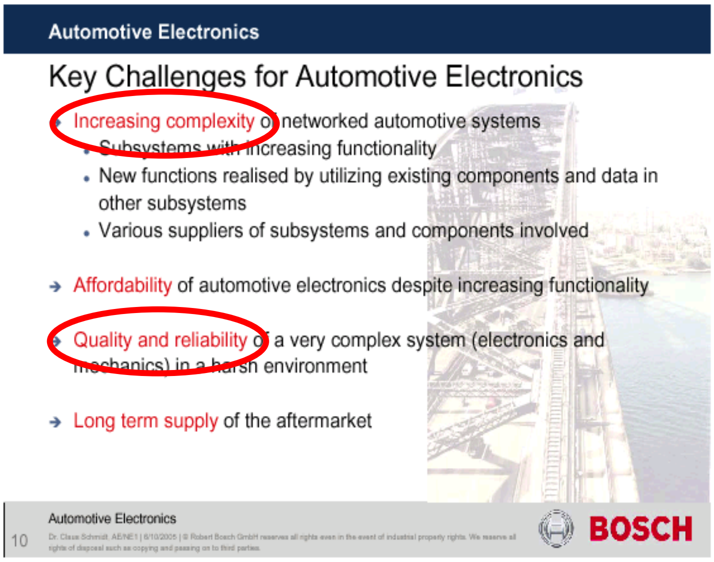
State-of-the-Art Automotive Embedded System (of Systems)

- Highly complex and historically grown network
- Around 70 single-core based ECUs
- Around 2.7 km wire length



[Michel 2013] **Taming multicores for safe transportation: ARAMiS in the automotive domain**
Workshop on the Integration of mixed-criticality subsystems on multi-core processors at HiPEAC 2013



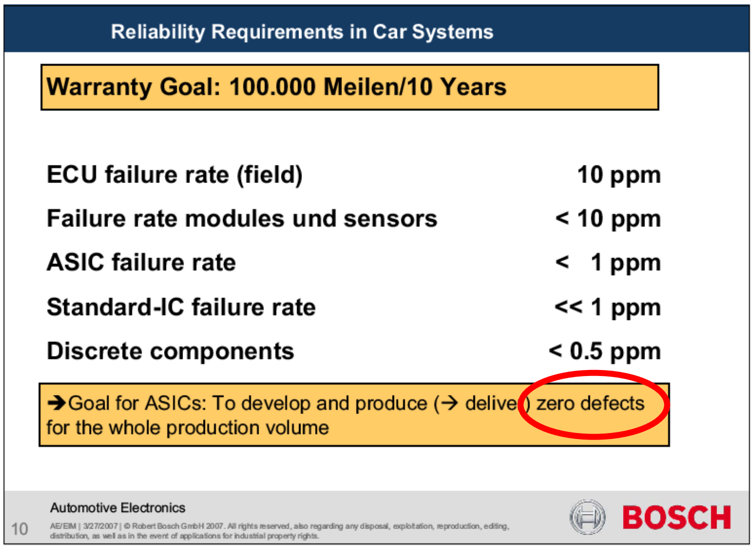
Automotive Electronics

Key Challenges for Automotive Electronics

- Increasing complexity of networked automotive systems
  - Subsystems with increasing functionality
  - New functions realised by utilizing existing components and data in other subsystems
  - Various suppliers of subsystems and components involved
- Affordability of automotive electronics despite increasing functionality
- Quality and reliability of a very complex system (electronics and mechanics) in a harsh environment
- Long term supply of the aftermarket

Automotive Electronics

BOSCH



Reliability Requirements in Car Systems

Warranty Goal: 100.000 Meilen/10 Years

ECU failure rate (field)	**10 ppm**
Failure rate modules und sensors	**< 10 ppm**
ASIC failure rate	**< 1 ppm**
Standard-IC failure rate	**<< 1 ppm**
Discrete components	**< 0.5 ppm**

→Goal for ASICs: To develop and produce (→ deliver) zero defects for the whole production volume

Automotive Electronics

BOSCH

Challenges for Future Embedded / CPS Computing Platforms

- **Programming and application partitioning for efficient utilization of nominally available processing resources**
  - Migration (with and without parallelization) of existing legacy code onto multicore processors
  - Model-based design, programming models and tools for the design and validation of multicore processor hardware and applications

- **Guarantees for extra-functional requirements**
  - Real-time, energy & power efficiency, security, safety
  - Mixed-criticality applications accessing shared processing resources (memory, on-chip interconnect, I/O interfaces)
  - Technology induced variability challenges

- **Overwhelming complexity** at multiple abstraction levels of Hardware/Software systems

Self-Aware / Self-Organizing Information Processing Factory

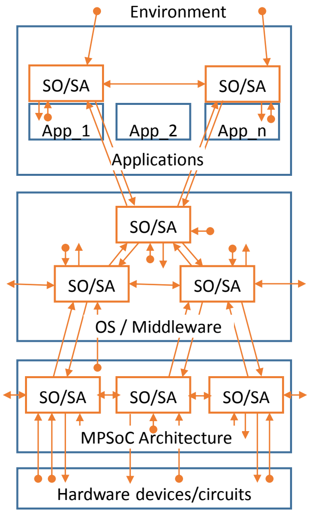
- Scalability of control through higher sub-system autonomy …

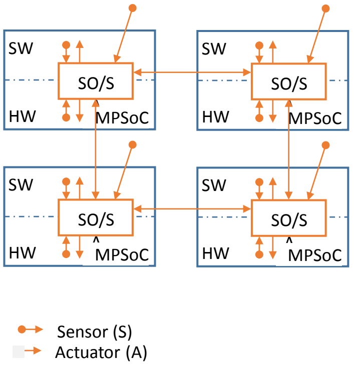
- … while operating within a corridor of guaranteed objectives and operation parameters

Objectives of a Self-Aware Information Processing Factory

- **Envision a holistic, hierarchically structured platform control**
  - As modular and decentralized as possible, …
  - … as much centralized as necessary
  - Scalability and dynamic elasticity to react on short/long term workload fluctuation and platform uncertainties
- **Orthogonal functional and control complexity**
  - Self-awareness through ubiquitous sensing of platform and environment
  - Self-organized local actions
  - Inspired by self-organization and emergent phenomena in nature
- **Predictive guarantees for critical tasks / functions**
  - Long term planning and logistics

Self-Aware / Self-Organizing Information Processing Factory





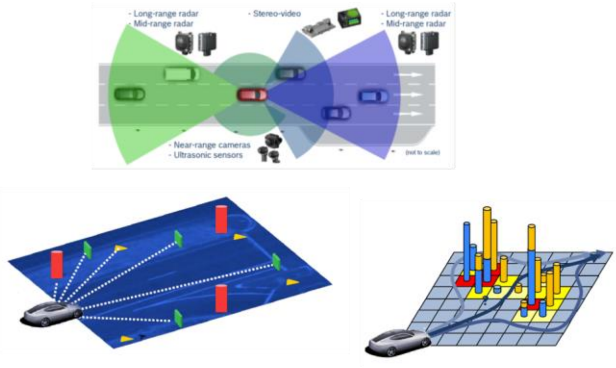
IPF Use Case: ECU Platform for Automated Driving

Perception
- Surround sensing (sensors)
- Online map data (internet)
- Grid fusion (uncertainty)

Orientation
- Location sensing (GPS)
- Image processing (landmarks)
- Online map data (landmarks)
- Data fusion (GPS+landmarks)

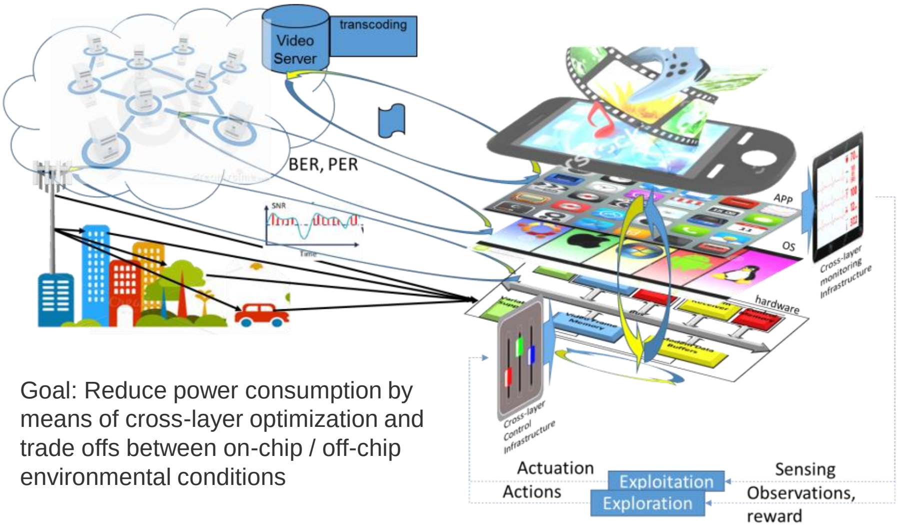
Intelligence
- Trajectory calculation and assessment
- Target trajectory

Motion
- Motion control



Source: Michael Fausten, Bosch, ESWEEK 2015

IPF Use Case: Self-Aware SmartPhone Platform



- Goal: Reduce power consumption by means of cross-layer optimization and trade offs between on-chip / off-chip environmental conditions

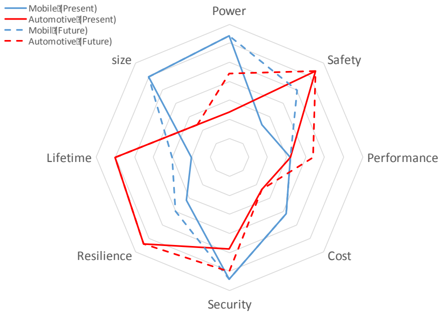
Comparison on Use Case Requirements

Automated Driving

- Safety, lifetime and resilience dominated
- Foreseeable future challenges with power, security and performance

Mobile Devices

- Performance / W, size, security and cost are main challenges
- Safety in context of medical applications expected to rise



Trend: System evolution and convergence (SmartPhones as integrated devices in future cars) will lead to requirements convergence

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Related Work

There is a rich portfolio of related work from which we plan to adopt proven concepts and enhance wherever relevant to our work

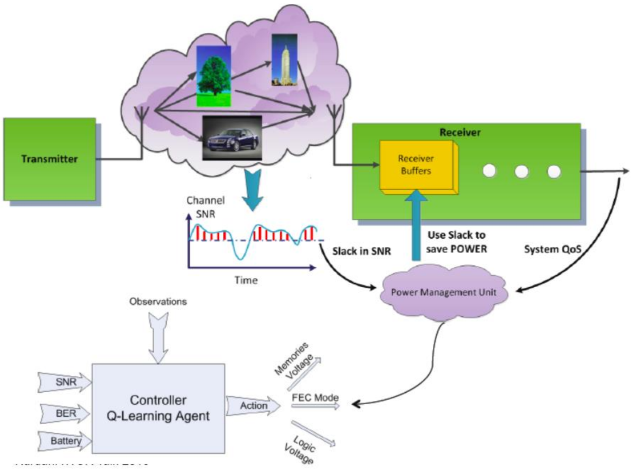
Coarse classification of relevant related work:

- Autonomous Computing
  - Primarily dealing with large scale, self-organizational IT systems
- Self-aware Computing for Control
- Multi-agent Systems in services and operation

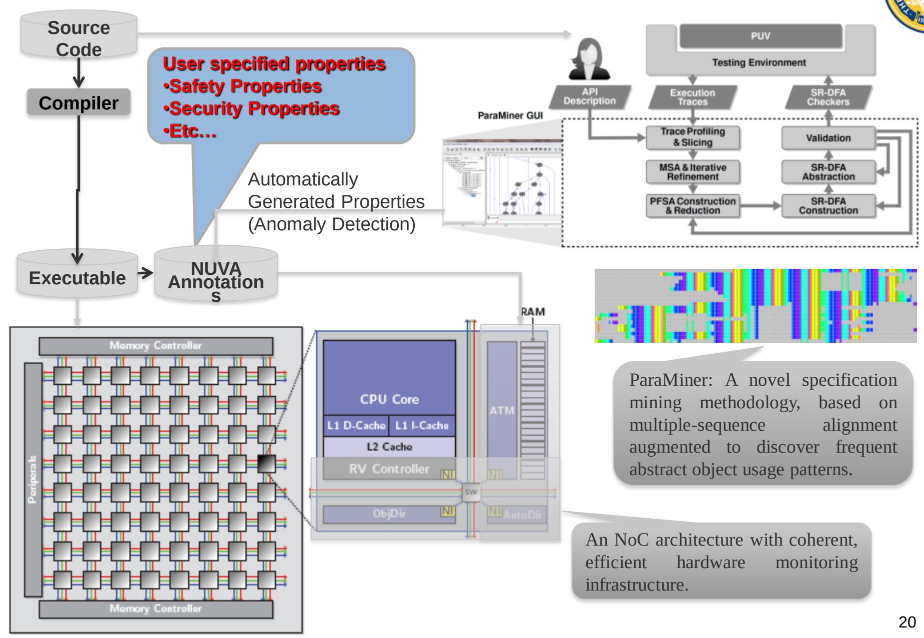
Prior Art: Cognitive Power Management

Reactive, channel-aware power management

- Learning-based cognitive control across multiple layers and multiple applications within one layer



NUVA – Runtime Verification Architecture



User specified properties
•Safety Properties
•Security Properties
•Etc…

Automatically Generated Properties (Anomaly Detection)

ParaMiner: A novel specification mining methodology, based on multiple-sequence alignment augmented to discover frequent abstract object usage patterns.

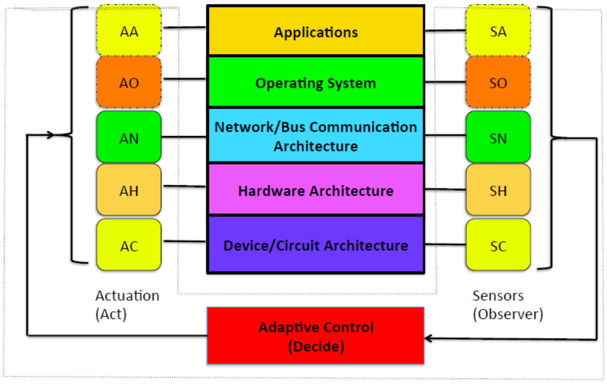
An NoC architecture with coherent, efficient hardware monitoring infrastructure.

Prior Art: CPSoC - Cyber Physical System on Chip

Sensor/Actor rich SoC with software enabled adaptive control of platform resources

- Self-aware, reflective (observe-decide-adapt) architecture to achieve closed loop system control
- Dynamic characterization of platform variability across multiple levels of system stack

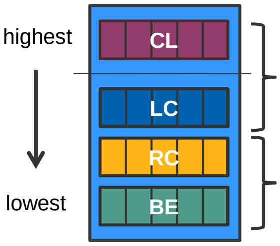
See next presentation for in depth treatment



Prior Art: IDAMC – Dependable Architecture for Many-Cores

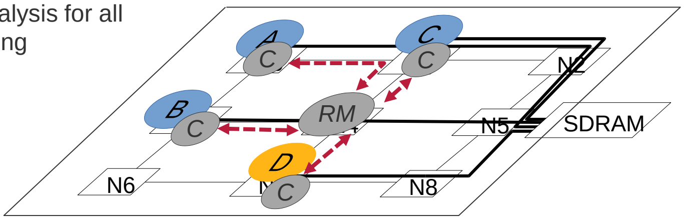
Configurable NoC with central Resource Manager provisioning VC-based interconnect channel assignments and memory accesses for safety critical applications

- Decoupled data flow and control protocol
- Protocol based synchronization
- Predictable SDRAM scheduling
- Worst case timing analysis for all traffic levels and routing mechanisms

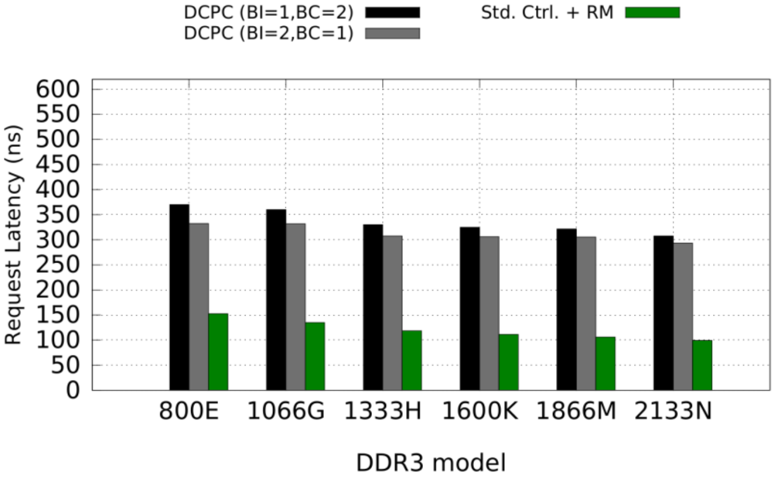


shaping: RM
routing: sep. buffers

reservation: RM
router: shared buffer



Resource Managers and SDRAM scheduling



Worst-case latency for a 4x64B request on DDR3 devices (with 32-bit wide interfaces)

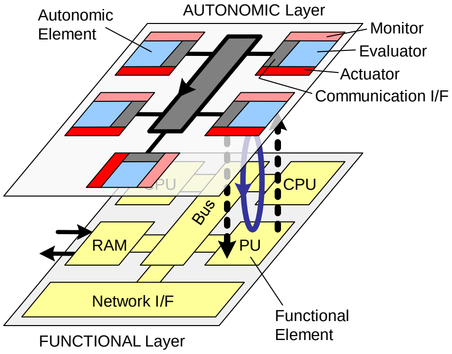
Prior Art: ASoC - Autonomic System on Chip

Evolutionary, platform-centric approach with compatibility to SoC design method:

- Functional layer containing conventional IPs
- Autonomic layer extends IPs with self-x properties
    - Improved Reliability
    - Performance / Power optimization at runtime

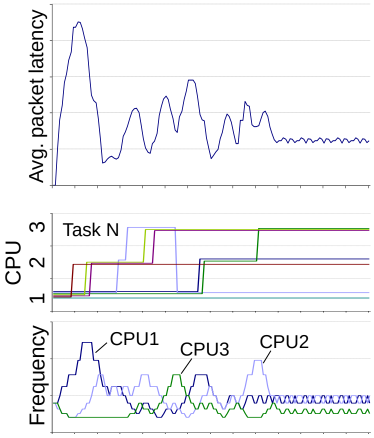
Dedicate part of chip capacity to self-x abilities at autonomic layer

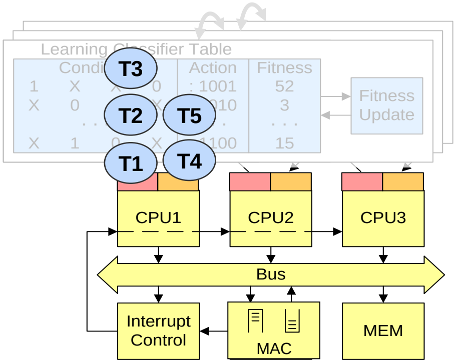
Future SoC shall have the ability to learn to live with environmentally imposed variations or work around defects autonomously



Joint project with University of Tübingen and FZI Karlsruhe (W. Rosenstiel, O. Bringmann)

ASoC: Self-Optimization through Runtime Learning





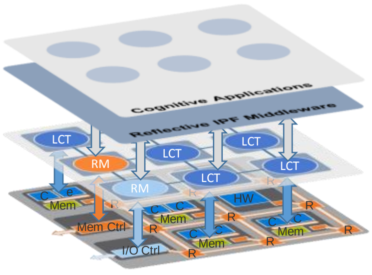
Self-Aware IPF Platform Integration

Moving long term, robust and interdependent system operation in the focus of platform design

- Reuse, converge and enrich existing HW/SW building blocks
  - Interworking between TUBS RM and TUM LCT, …
  - … as well as with UCI CPSoC middleware
  - and cognitive control within applications

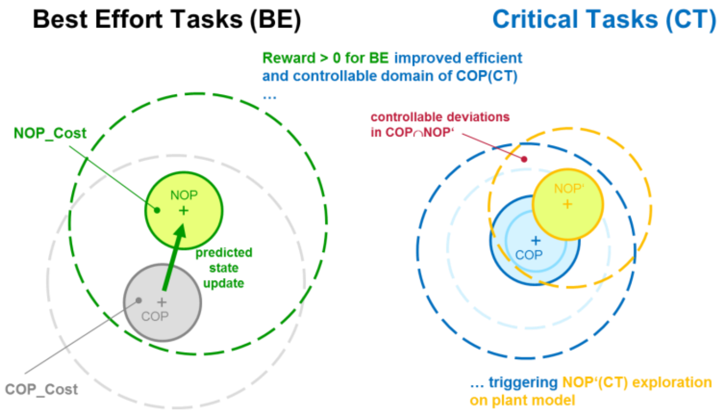
Facilitate

- Exploitation of emergent control efficiency, …
- … with hard guarantees for critical tasks
- Stable and effective coexistence of HW/SW machine learning entities at different layers



Relevant IPF Research Challenges

- **Ensure robust, predictable system properties with a hybrid combination of self-aware / self-organizing emergent control and classical WC-oriented control?**



Relevant IPF Research Challenges

- **Ensure robust, predictable system properties with a hybrid combination of self-aware / self-organizing emergent control and classical WC-oriented control?**

- **How to combine various self-aware individual system constituents into higher-layer group awareness?**
  - What type and amount of sensor information to transfer among different SO/SA levels?

- **What cost/overhead for a holistic IPF control framework is realistic?**

- **On a more general perspective: What can we learn from logistics and organization of factories given our societal experience in this field?**

Thanks!