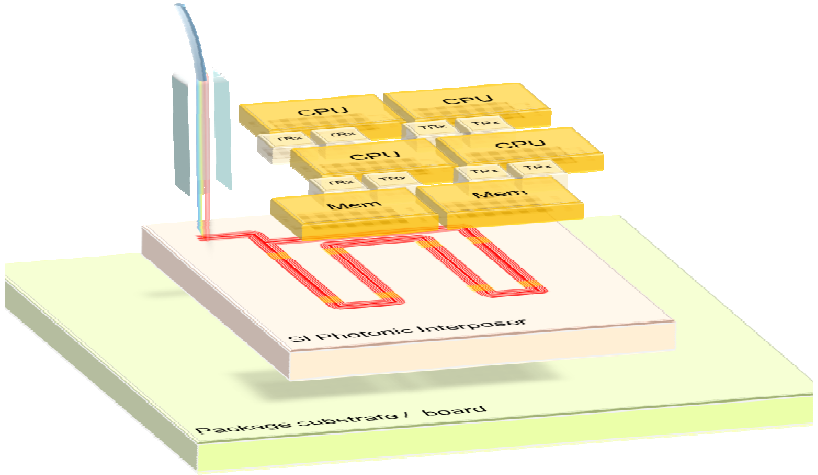
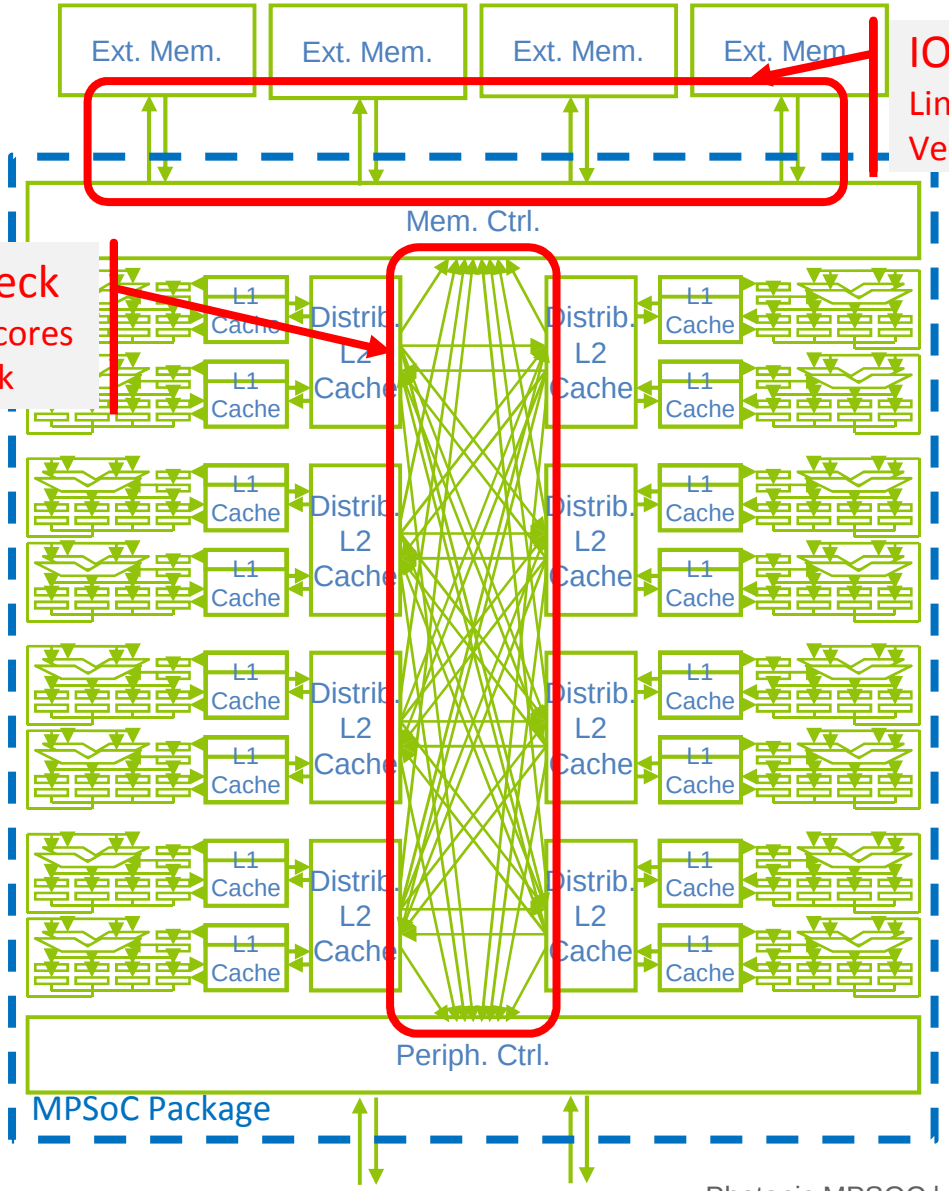



# PHOTONIC MPSOC

# COMMUNICATION BOTTLENECKS IN MANYCORES




**IO Bottleneck**
Linear BW increase w. #cores
Very high throughput muxed links

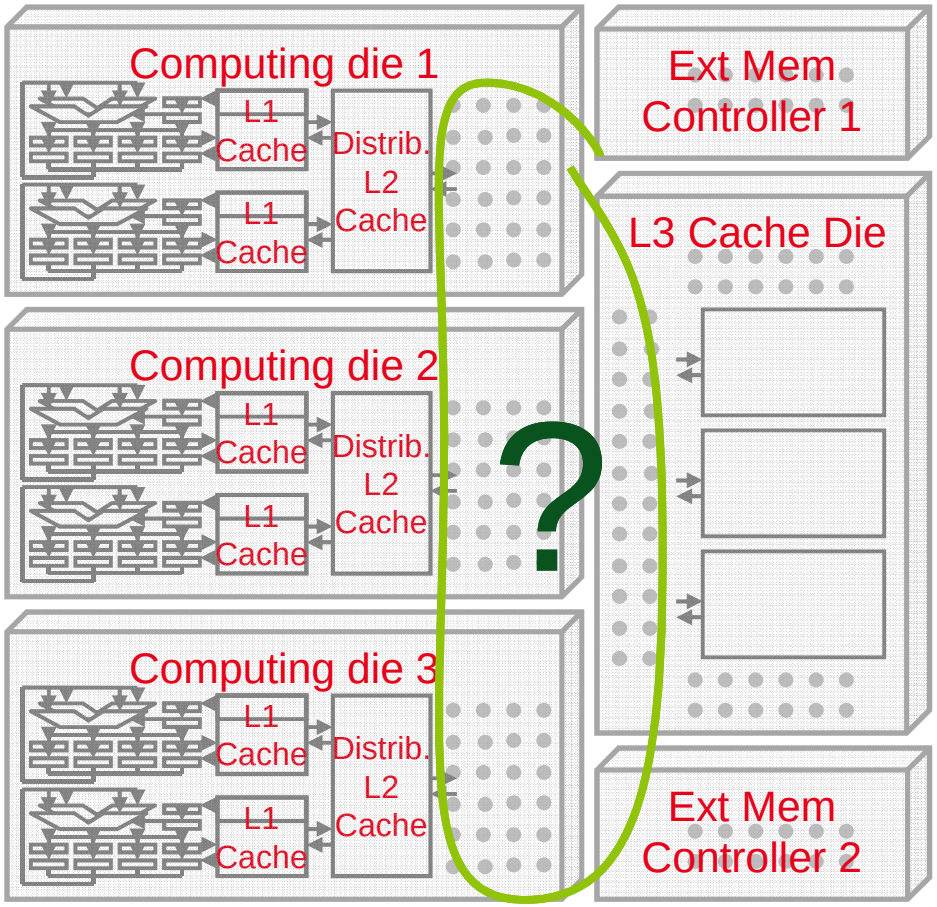
**Internal Com. Bottleneck**
Quadratic BW increase w. #cores
Constant throughput per link

(2015)[NOCS] Thonnart, Y.

# CHIPLET PARTITIONING ON INTERPOSERS TO INCREASE YIELD… AND REDUCE DESIGN COST

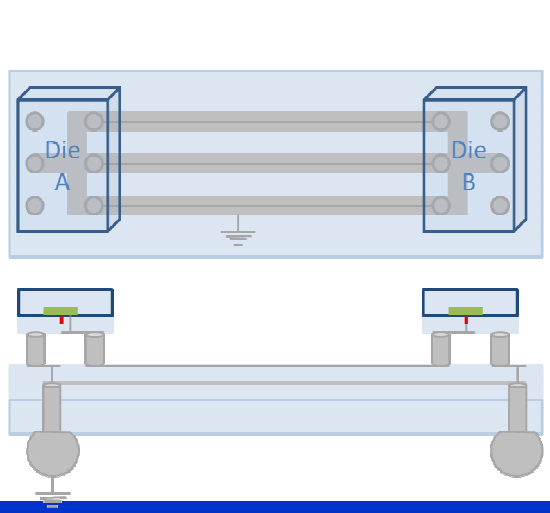
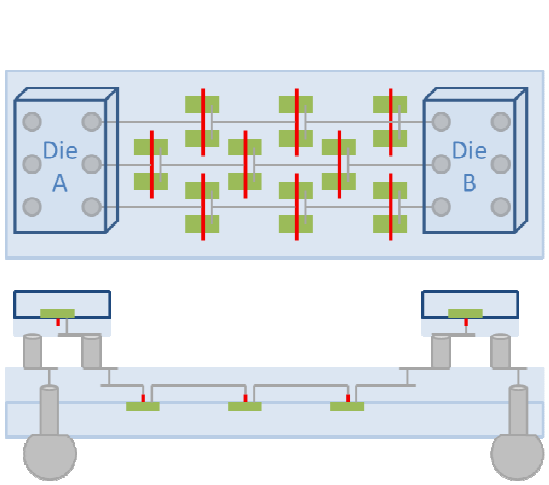
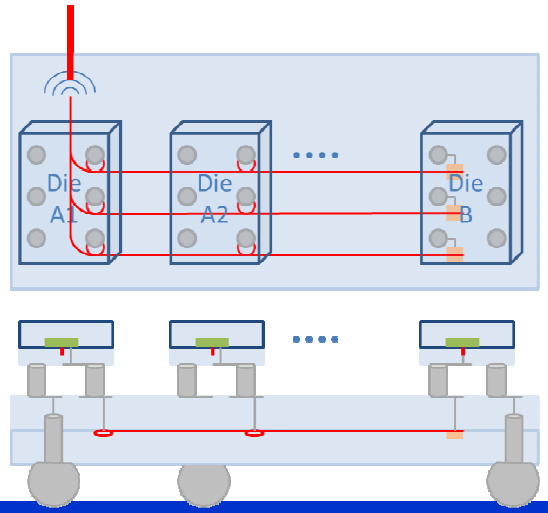
- **Higher manufacturing defects per cm² in advanced CMOS nodes**
  - Very-low yield on large monolithic dies
- **Options:**
  - Design 4–6 cm² dies, deactivate processors, sell as lower grade
  - Design **≤1 cm²**, and stack on variability tolerant interposer

➔ **Need an efficient and scalable interconnect solution**

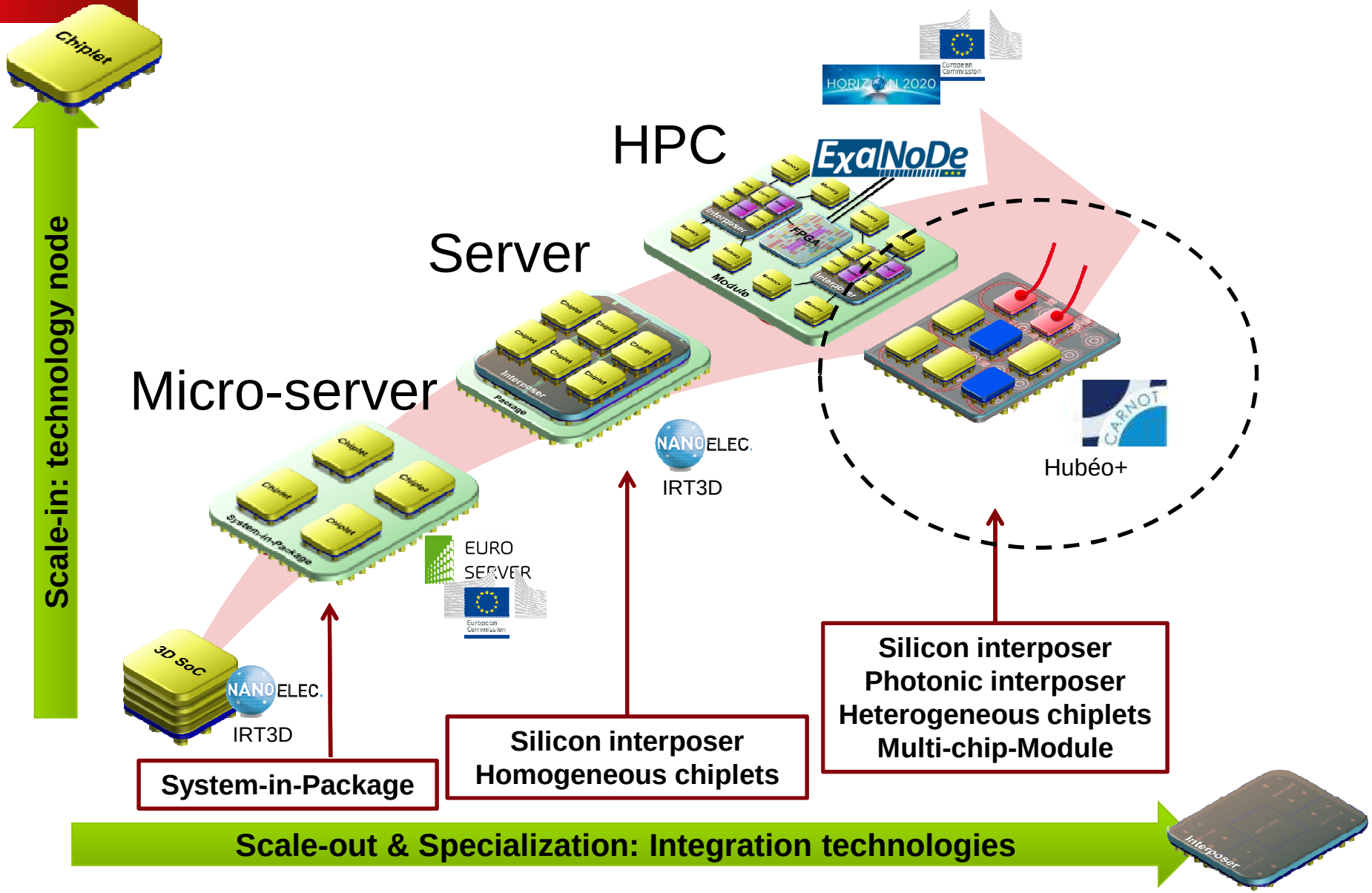



(2015)[NOCS] Thonnart, Y.

# INTERPOSER STRATEGIES

| Metallic interposer | Active interposer | Photonic interposer |
|---|---|---|
|  |  |  |
| + High yield, low cost<br>+ Low latency<br>- Don't scale<br>- Low flexibility<br>- Low bandwidth | + Chiplets scaling<br>+ Communication adaptation<br>- Cost (?)<br>- Medium bandwidth | + Low latency<br>+ Huge bandwidth density<br>- Flexibility<br>- Static power |

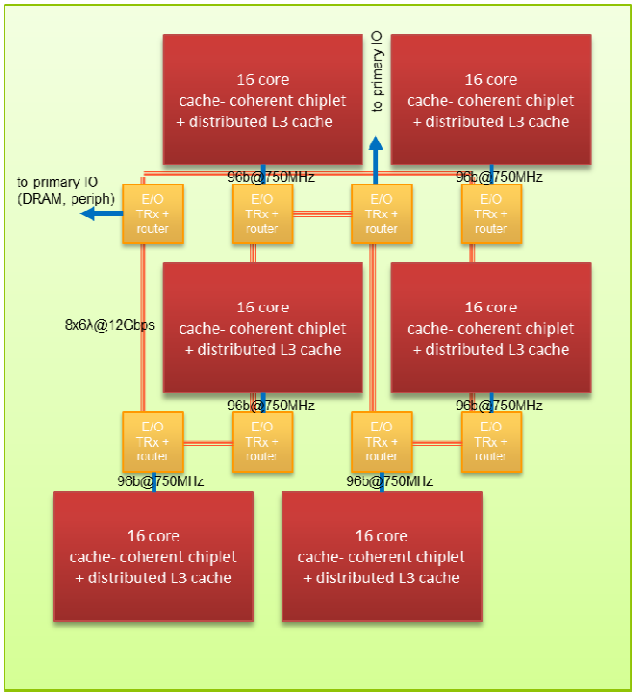
# 3D COMPUTING ROADMAP @ LETI

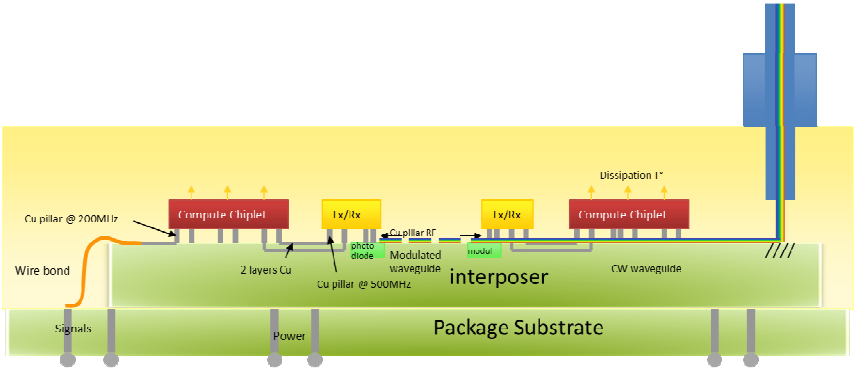


# HUBEO+ MANYCORE ARCHITECTURE

- **96 cores in 6 chiplets on the interposer**
  - Coherent shared-memory
  - Boots a single Linux OS
- **ONoC to convey cache coherence protocol**
  - 6 wavelengths used in parallel at 12 Gbps
  - Complete connection between 8 transceivers/routers
  - Fan-out to the distributed L3 caches, main memory and peripherals.

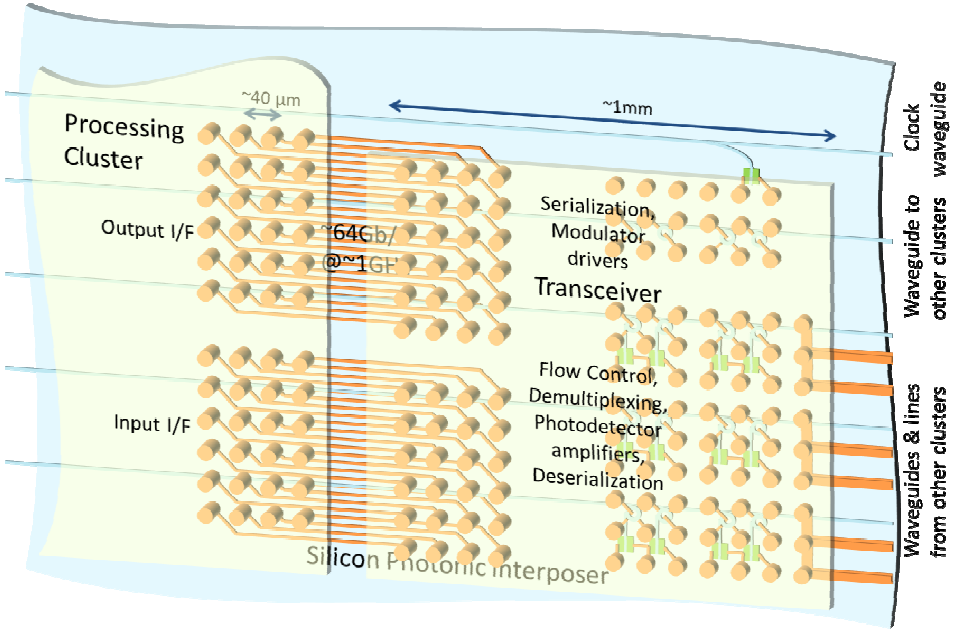
➔ Peak aggregated bandwidth on the interposer is 576 Gbit/s



# ONOC DESIGN CHALLENGES

- **Ultra-dense integration**
  - Implementing a complete graph interconnection
  - ➔ Drivers limited to ~0.01mm² per channel




- **Power-efficient architecture**
  - But with good scaling properties
  - Synchronous NoC point-to-point communication power budget > 20pJ/bit

- **Wide temperature range**
  - The system should also be operational at ambient temperature and full load
  - ➔ 0°C to 90°C operating range

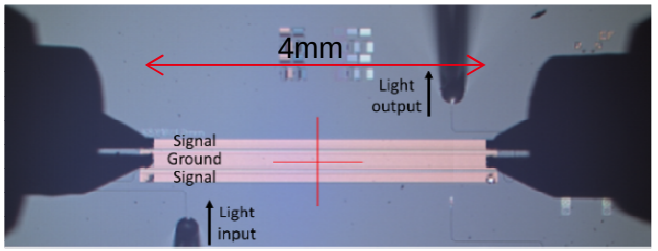
(2014)[FETCH] Y. Thonnart (invited)

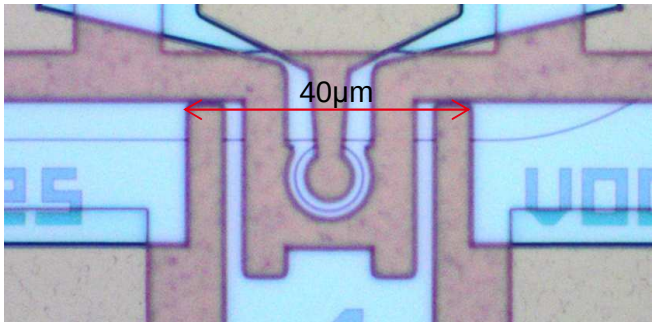
# ULTRADENSE MICRORING RESONATORS

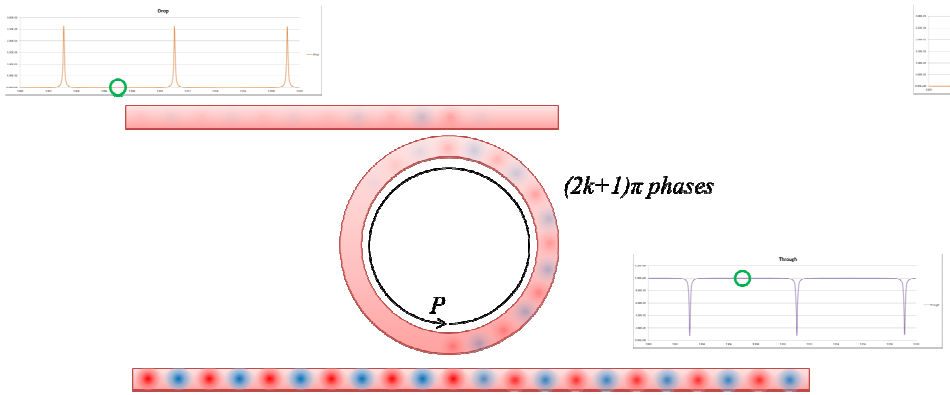
- **Dense integration requirement:**
  - Mach-Zehnder modulators are too long to be matriced locally (>1mm)

  ➔ Microring resonators are compact
    - ➔ have sharp resonances allowing WDM
    - ➔ PN or PIN diode junction for electrical control

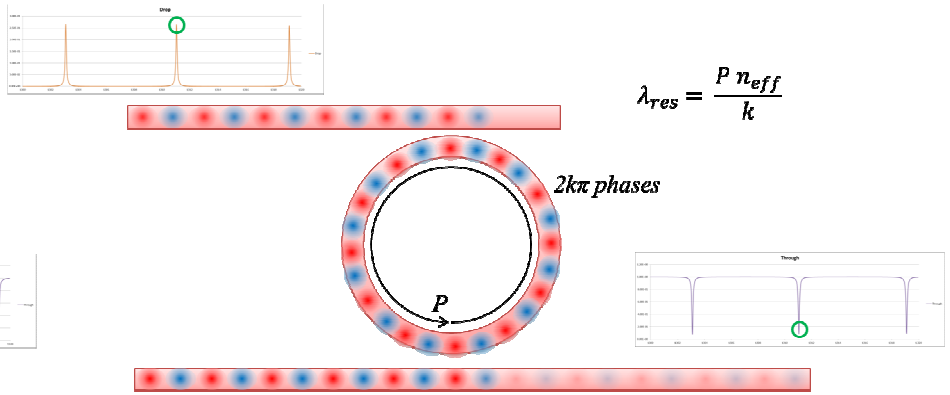
    - ➔ PN rings can be used as modulators (> 10 Gbps)
    - ➔ PIN rings can be used as filters (<500 MHz) for routing and wavelength demultiplexing



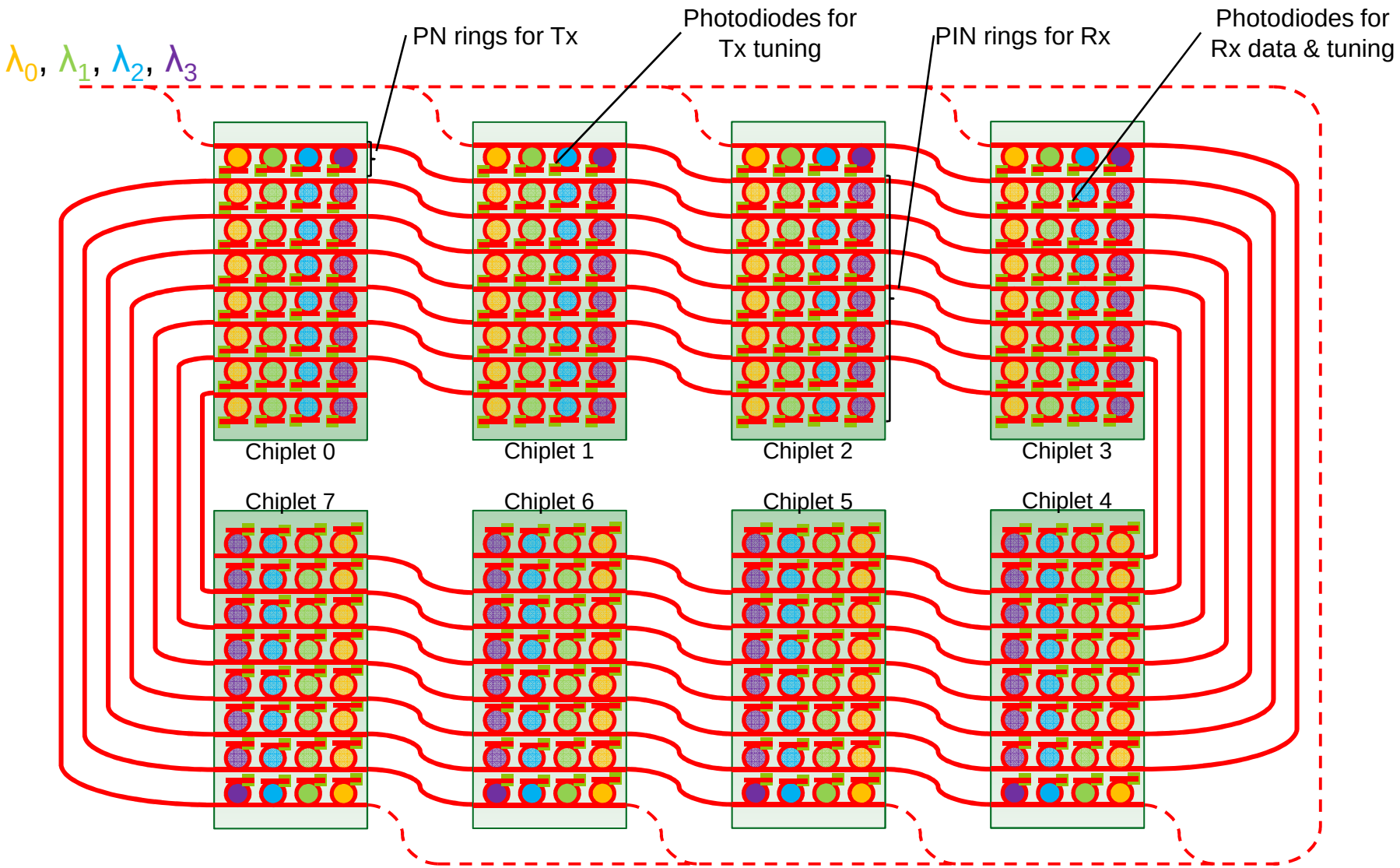

Out of resonance




At resonance

(2016)[SPIEOI] Reboud et al.

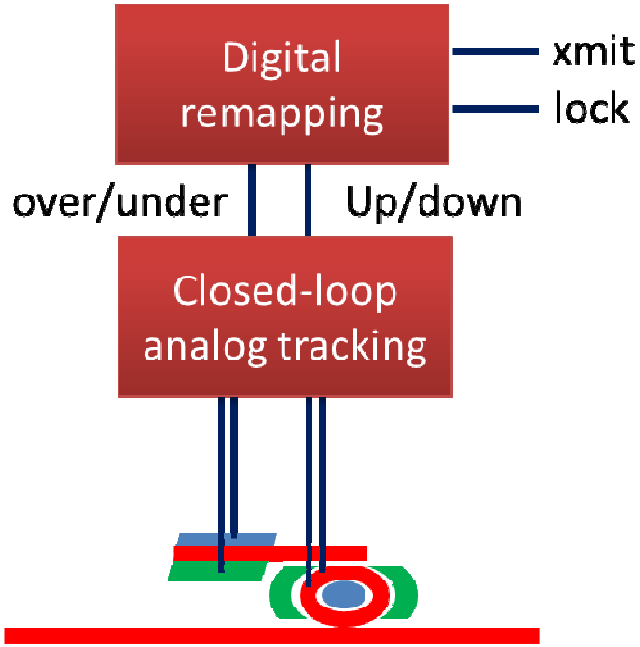
# POWER EFFICIENT ARCHITECTURE: ONOC TOPOLOGY

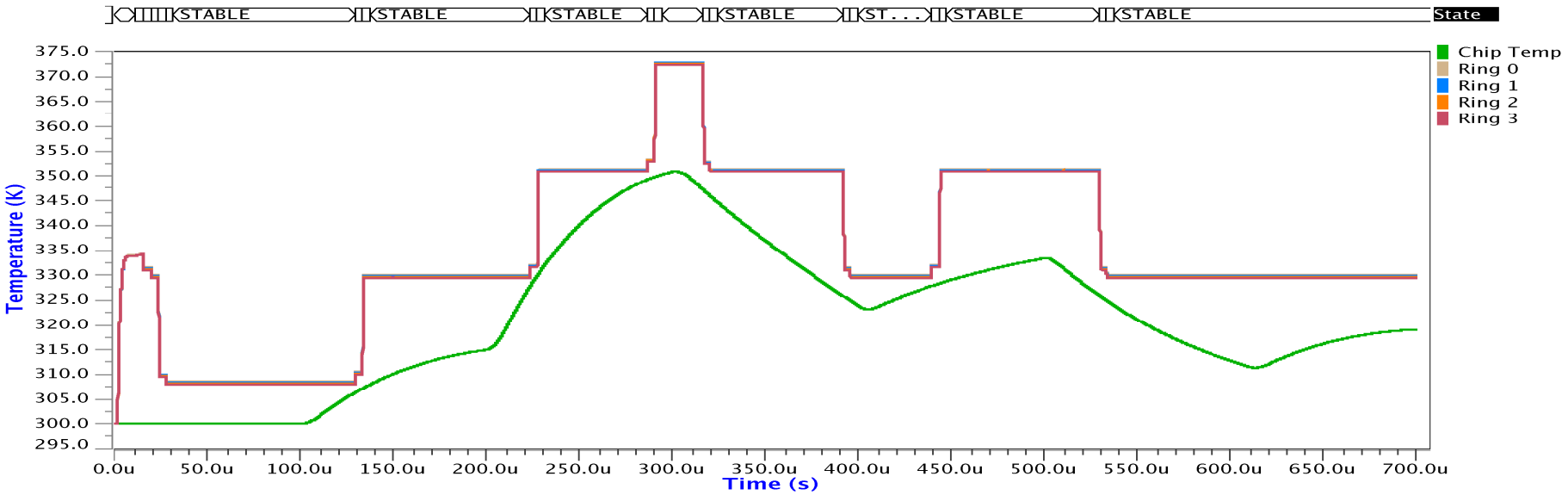



Patent (2013) EP2874334 / US9479256

# THERMAL TUNING

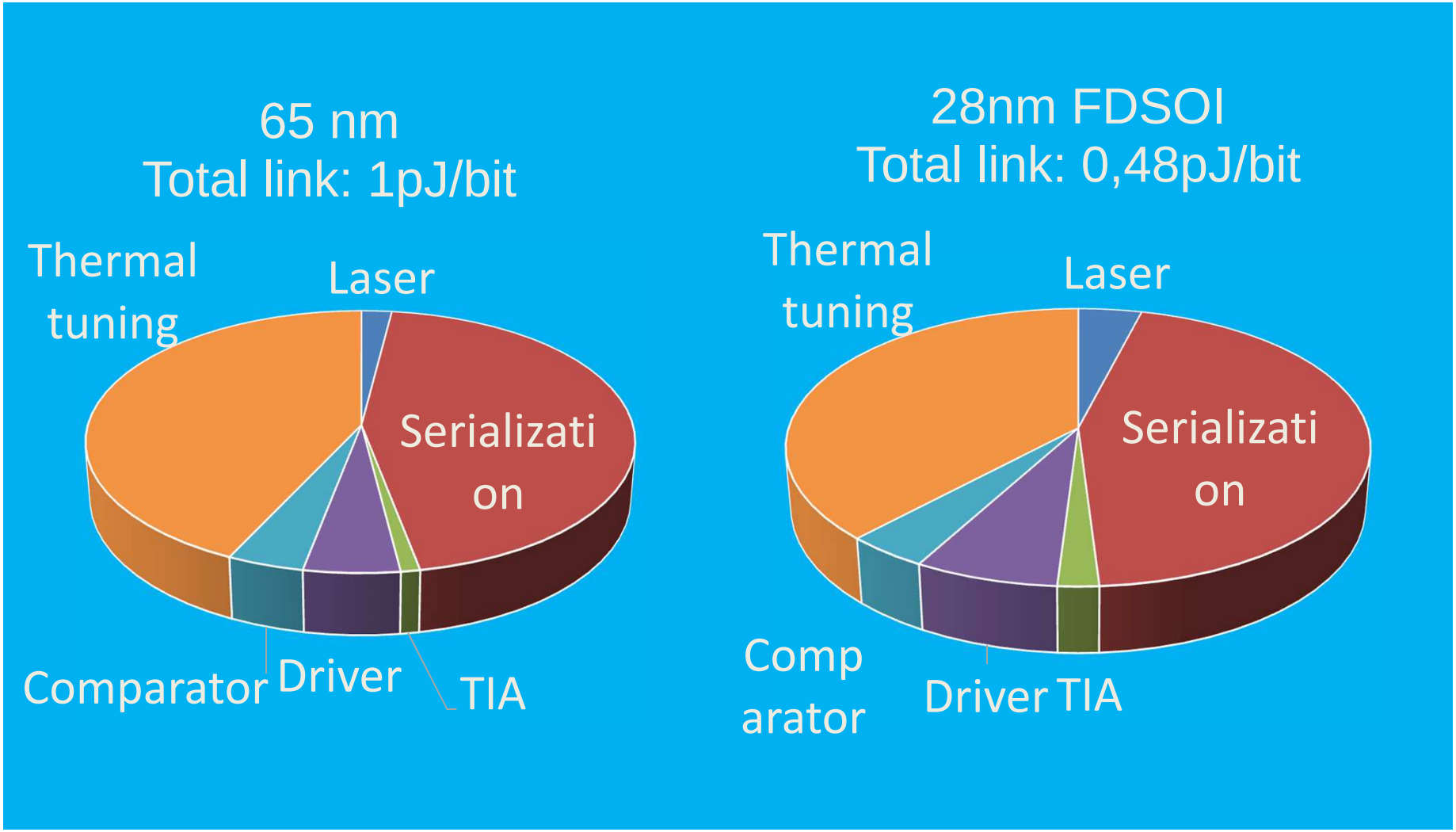
- **Use of the drop-port of the modulator**
  - Robust closed-loop control
  - Decision thresholds for remapping with hysteresis
  - Digital remapping decision from the different rings of the WDM
  - Automatic remapping to higher/lower wavelength



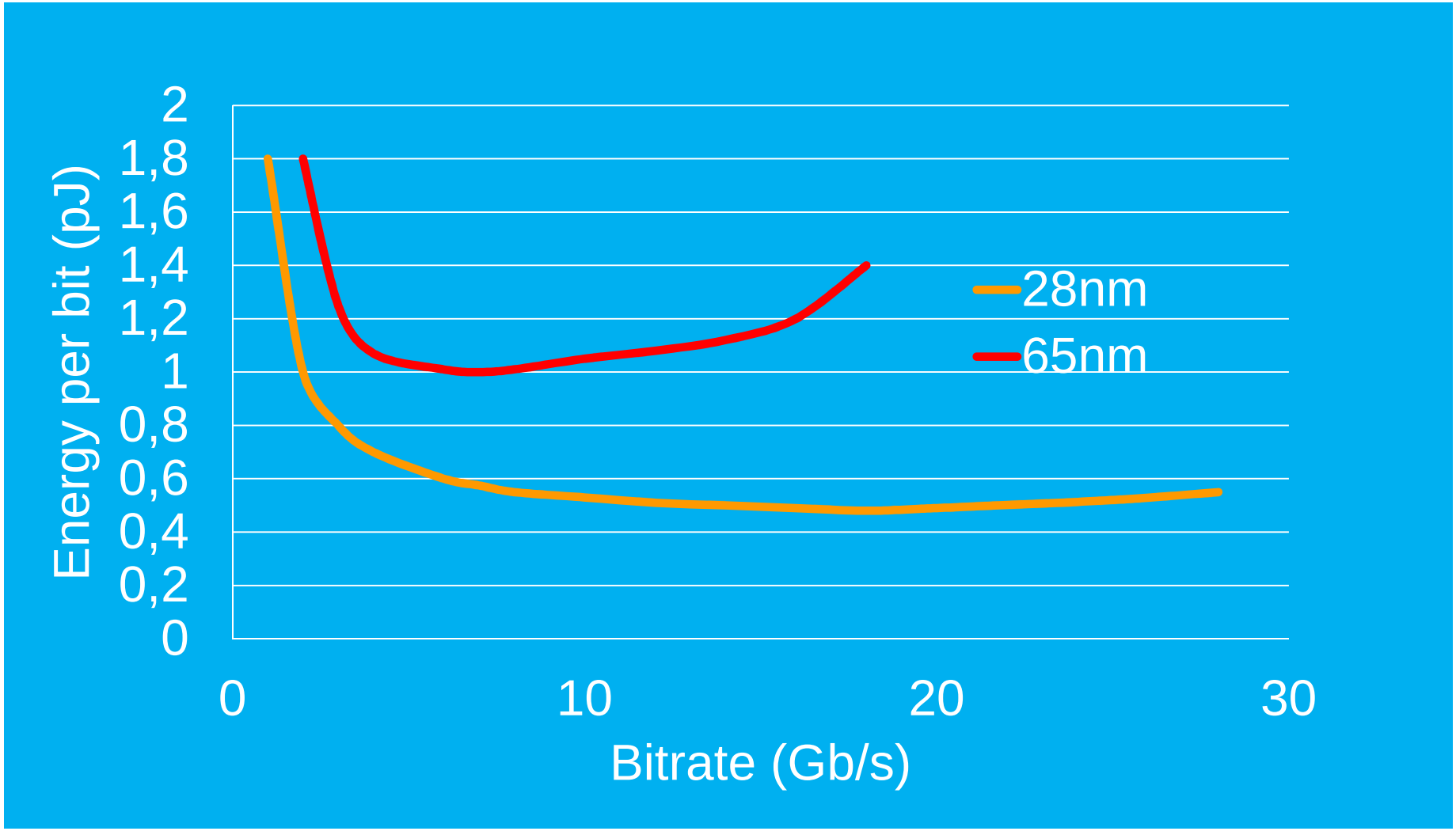




Patent (2014) EP3018526 / US2016131959

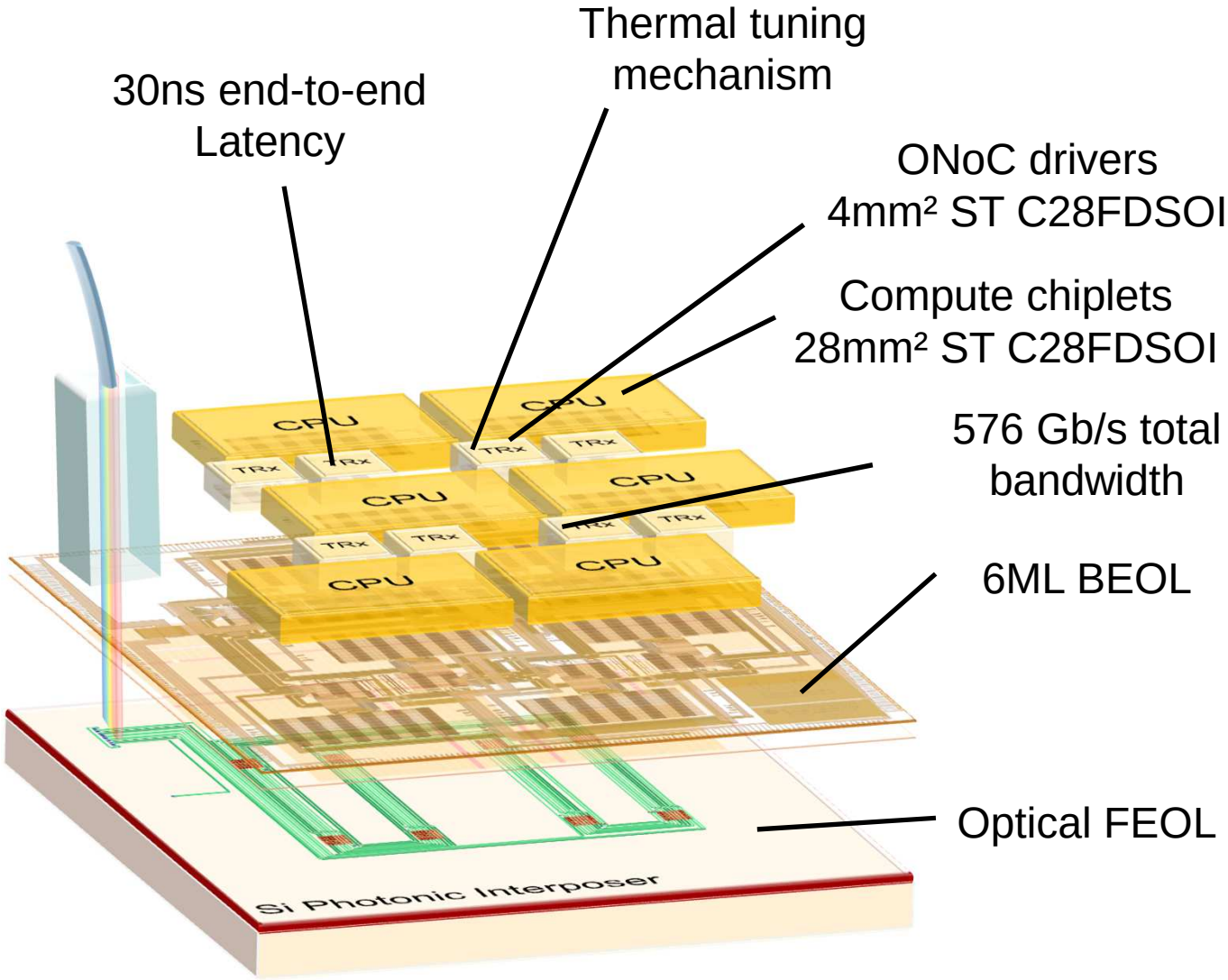
# PHOTONIC TRANSMISSION RESULTS



# HIGH BANDWIDTH @ OPTIMAL ENERGY EFFICIENCY

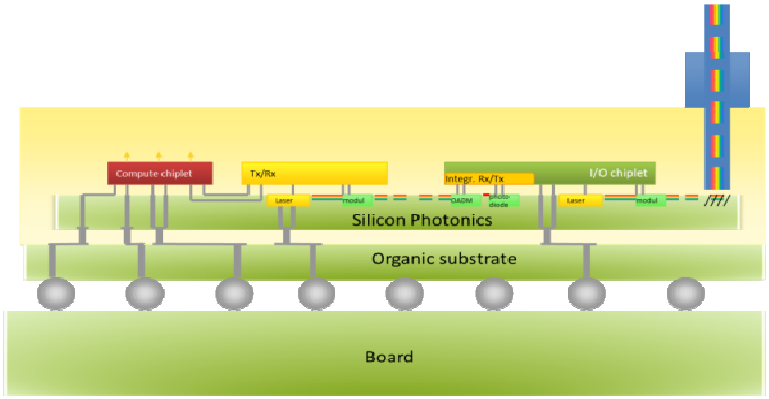


# PROTOTYPE: POPSTAR



# CONCLUSION

- Interposers are key to continue many-core integration
- Silicon photonics are high-end solutions providing the best scaling capabilities
- In the long run, with unified optical interfaces for on-chip and off-chip communication, the computation model itself could evolve



Many thanks to Yvain Thonnart
And its HUBEO+ team

**Leti, technology research institute**
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
**www.leti.fr**