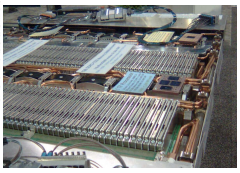
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

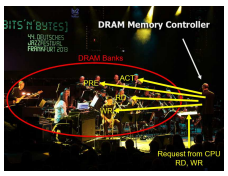
MPSoC'2017
July 2-7, 2017
Annecy, France

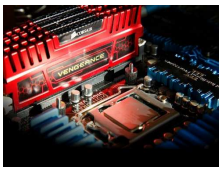
DRAM Memory Controller

From General Purpose to Application Specific Architectures

Norbert Wehn
//ems.eit.uni-kl.de



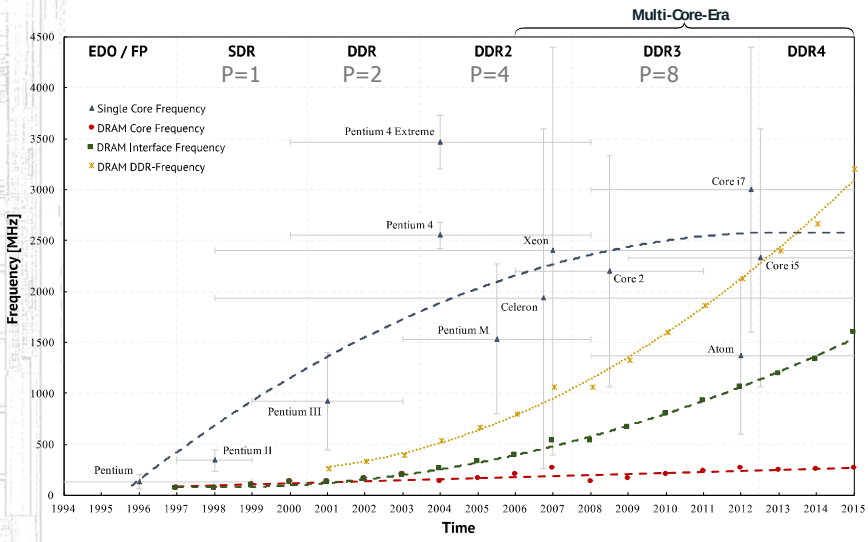




TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

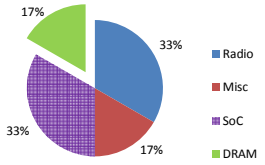
The Memory Wall



MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

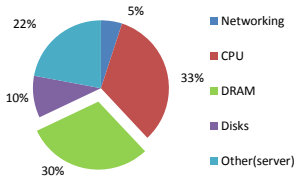
Power Breakdowns for …

… Suspended 3G State



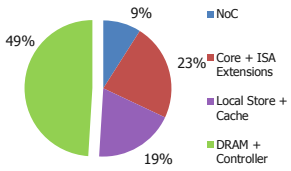
Source: The systems hackers guide to the galaxy: Energy usage in a modern smartphone

… Google Datacenter



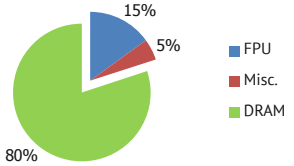
Source: The Datacenter as a Computer: An Introduction to the Design of Warehouse-Scale Machines. 2009

… Big Data Application



Source: Power Consumption of Green Wave Architecture 2011

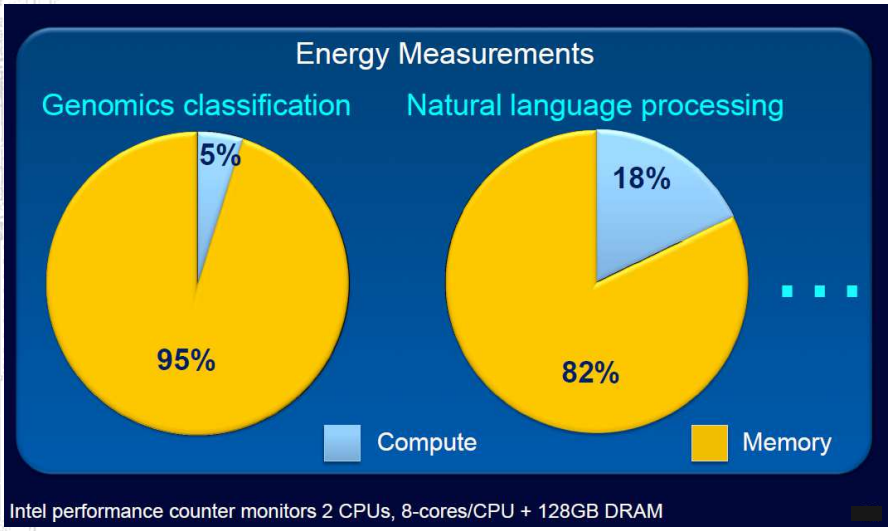
… eBrain



Source: A Scalable Custom Simulation Machine for the Bayesian Confidence Propagation Neural Network model of the Brain, 2014

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

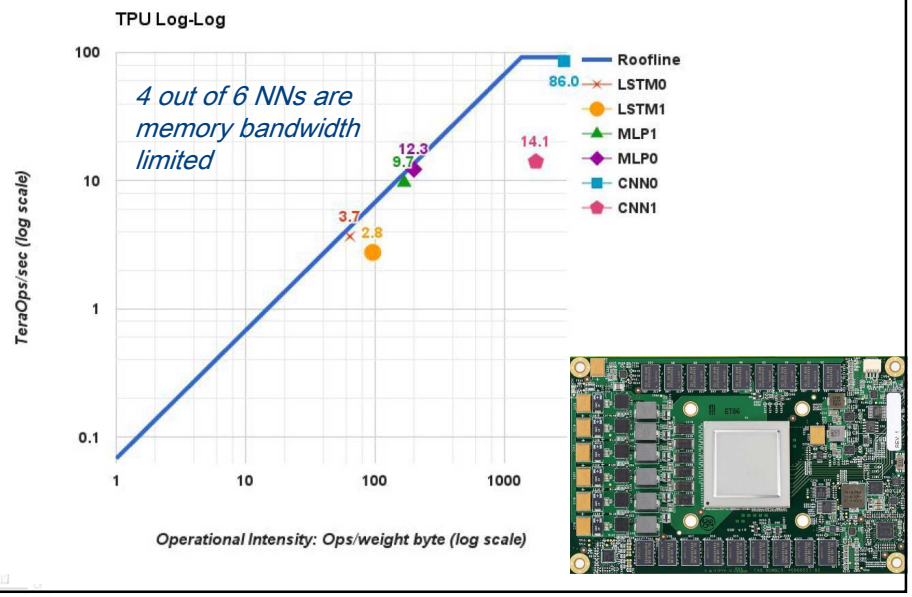
DRAM Energy Contribution



Source Subhasish Mitra

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

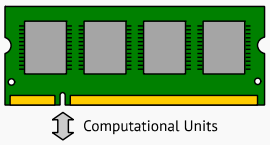
Roof Line Model Googles Tensor ASIC



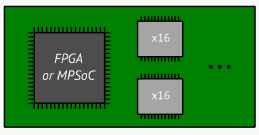
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

DRAM Subsystems

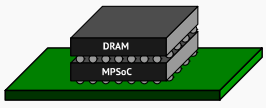
DIMM Based:
General Purpose Computers
e.g. DDR3, DDR4



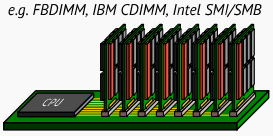
Device Based:
Embedded / Tablets / Graphic Cards
e.g. LPDDR3, GDDR5



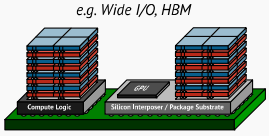
Package on Package (PoP):
Soldered on top of the MPSoC.
Smartphones
e.g. LPDDR3, LPDDR4



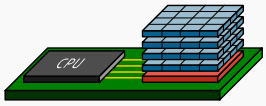
Buffer on Board:
Memory Controller on Buffer Chip,
Serial Connection
e.g. FBDIMM, IBM CDIMM, Intel SMI/SMB



3D/2.5D-Integrated:
Stacked on Logic or Silicon Interposer
by means of TSVs
e.g. Wide I/O, HBM

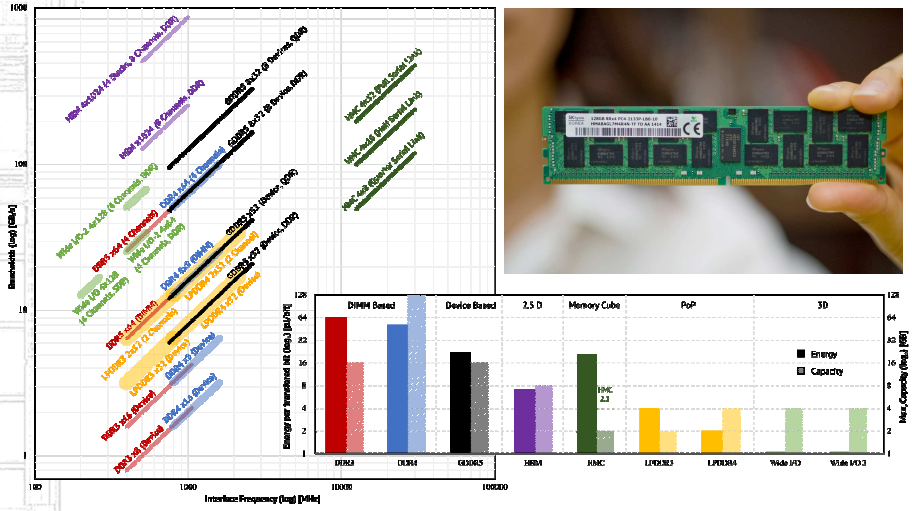


Memory Cube:
3D-Stacked, Memory Controller on
Bottom Layer, Serial Interconnect (SerDes)
e.g. HMC, SMC



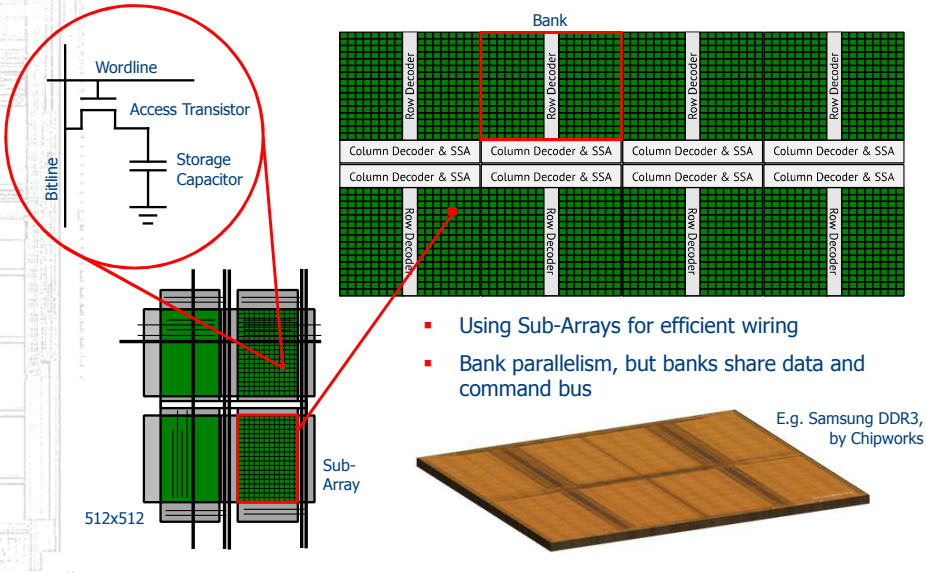
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

DRAM Subsystem Performance



MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

The DRAM Device

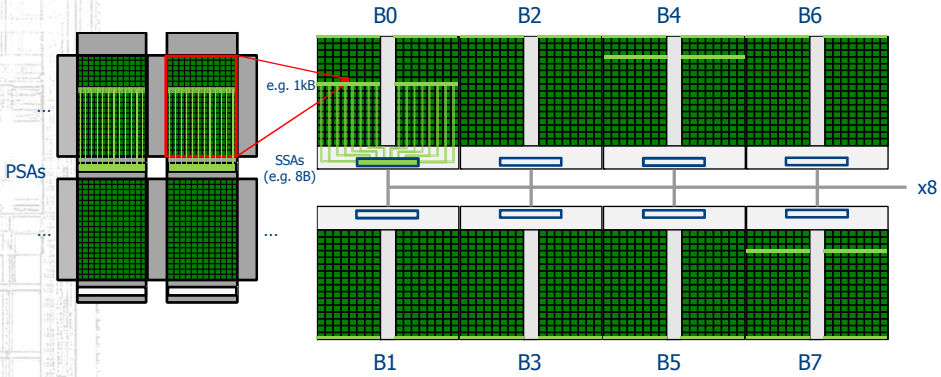


- Using Sub-Arrays for efficient wiring
- Bank parallelism, but banks share data and command bus

E.g. Samsung DDR3, by Chipworks

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

DRAM Device Operations

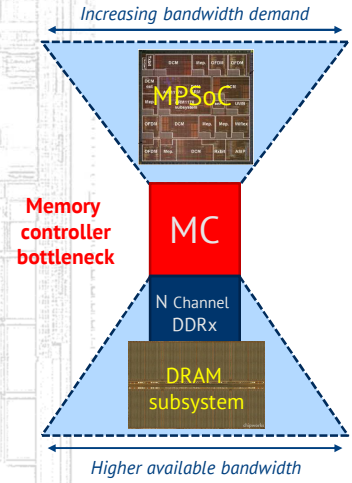


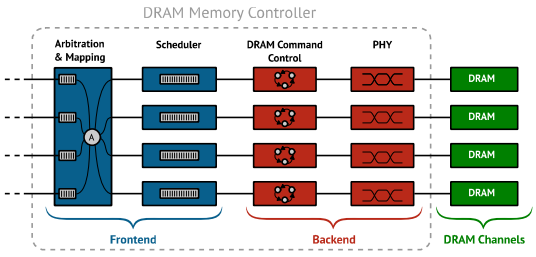
Important DRAM Commands

- ACT: Activates a specific row in a specific bank (sensing into PSA) — *tRCD*
- RD: Read from activated row (prefetch from PSA to SSA and burst out) — *tCL + tBURST*
- PRE: Precharges set LWL=0 set LBL=VDD/2 — *tRP*
- REFA: DRAM cells are leaky and have to be refreshed — *tREFI & tREF*

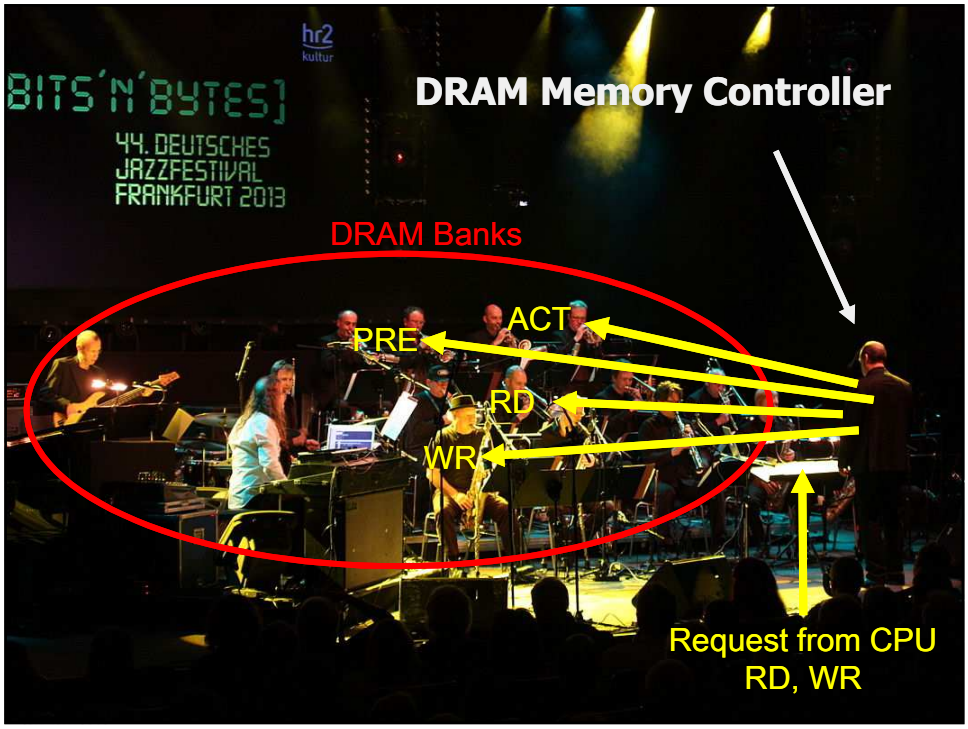
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

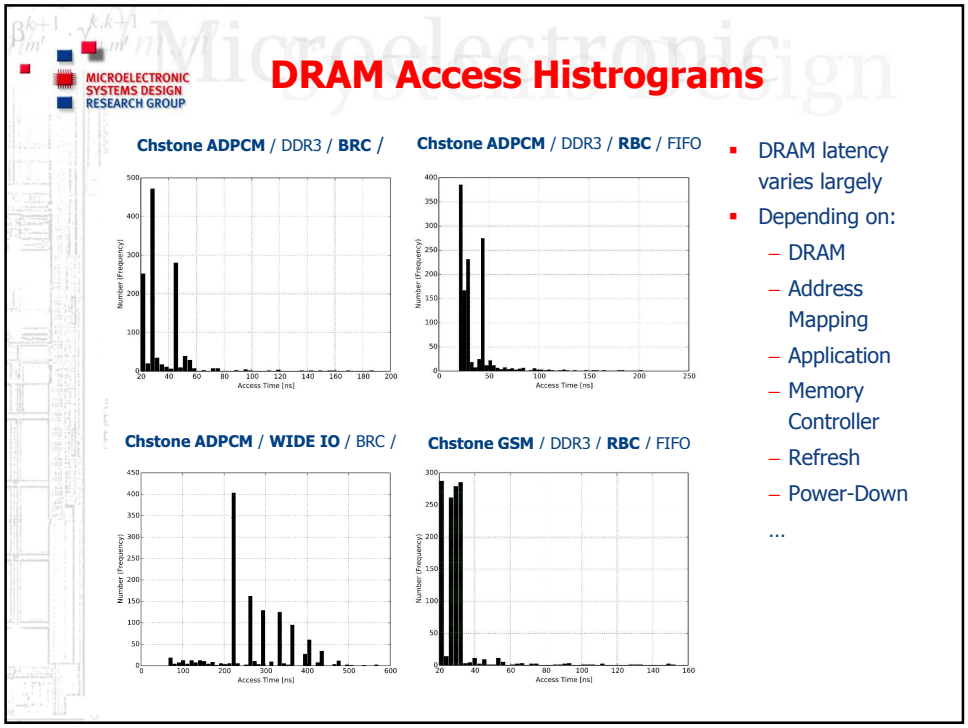
DRAM Memory Controller





- DRAM controllers must provide higher bandwidth and low latency
- New controllers and approaches are mandatory, especially in the fronted

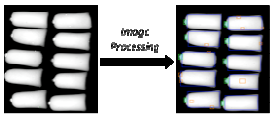

hr2
kultur
BITS'N'BYTES
44. DEUTSCHES
JAZZFESTIVAL
FRANKFURT 2013
DRAM Memory Controller
DRAM Banks
ACT
PRE
RD
WR
Request from CPU
RD, WR

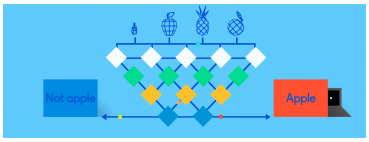

MICROELECTRONIC
SYSTEMS DESIGN
RESEARCH GROUP
DRAM Access Histrograms
Chstone ADPCM / DDR3 / BRC /
Chstone ADPCM / DDR3 / RBC / FIFO
Chstone ADPCM / WIDE IO / BRC /
Chstone GSM / DDR3 / RBC / FIFO
Number (Frequency)
Access Time [ns]
DRAM latency varies largely
Depending on:
– DRAM
– Address Mapping
– Application
– Memory Controller
– Refresh
– Power-Down
...

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Application Specific Memory Controller

- Many applications have a regular or fixed DRAM access pattern.
- Especially for embedded like FPGA / Streaming / Real-Time Signal Processing / Neuronal Networks: access pattern does not depend on data.
- COTS DRAM controllers only **local view** on the application, due to limited scheduler buffer size
- Application Specific Memory Controller: **global view** on the application

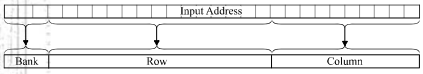




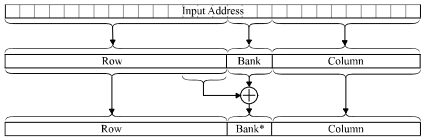
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Address Mapping

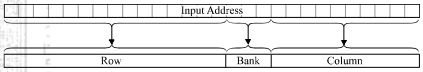
Standard Mapping (BRC)



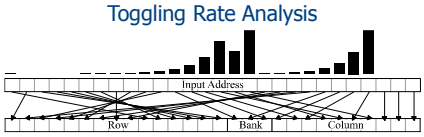
Permutation-Based Page Interleaving



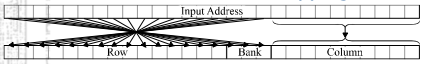
Bank Interleaving (RBC)

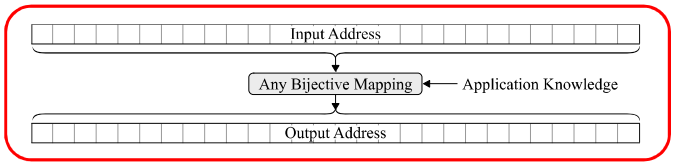


Toggling Rate Analysis



Bit Reversal Address Mapping

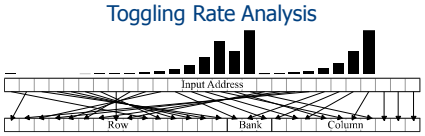


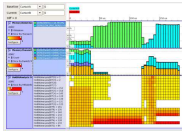


MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

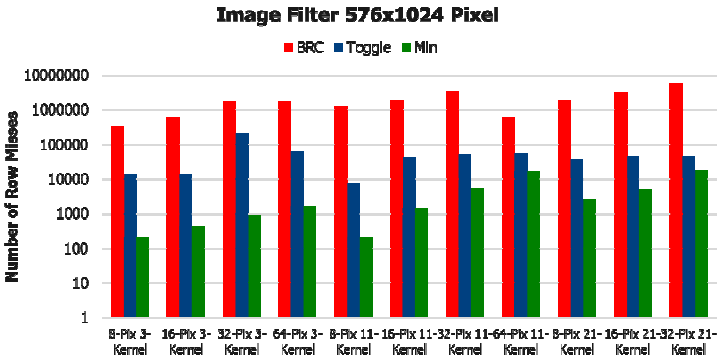
Toggling Analysis

Toggling Rate Analysis





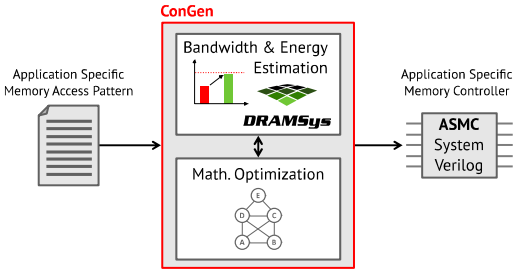
SYNOPSYS®
Designware
DDR Explorer



MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

ConGen Methodology

OPT Optimization Research Group



- Exploit full application knowledge i.e. determinism
- Goals:
  - Minimize #row misses
  - Decrease energy
  - Increase bandwidth
- Analysis of application access pattern
- Using mathematical optimization
- Generate the optimal controller for this application

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Optimum Address mapping: ILP

$$\min \sum_{t=1}^{T} \sum_{b=1}^{B} y_b(t)$$

Minimize number of row misses

$$s.t. \sum_{r=1}^{R} \sum_{b=1}^{B} x_{rb}(i) = 1 \qquad \forall i = 1,\dots,n$$

x_{rb} = 1 iff address i is in row r and bank b (each address i is assigned to exactly one row and one bank)

$$\sum_{i=1}^{n} x_{rb}(i) \le C \qquad \forall r = 1,\dots,R \;\; \forall b = 1,\dots,B$$

Every row r in bank b has at most C addresses assigned to columns

$$\sum_{r=1}^{R} s_{rb}(t) \le 1 \qquad \forall t = 1,\dots,T \;\; \forall b = 1,\dots,B$$

$s_{rb}(t)$ = 1 iff row r in bank b is opened at time t (only one row per bank can be active)

$$s_{rb}(t) \ge x_{rb}(f(t)) \qquad \forall t = 1,\dots,T \;\; \forall r = 1,\dots,R \;\; \forall b = 1,\dots,B$$

The row r in bank b must be open at time t if it is accessed at time t

$$y_b(t) \ge |s_{rb}(t+1) - s_{rb}(t)| \qquad \forall t = 1,\dots,T\text{-}1 \;\; \forall r = 1,\dots,R \;\; \forall b = 1,\dots,B$$

1: if row miss, 0: if row hit

$$s_{rb}(0) = 0 \qquad \forall r = 1,\dots,R \;\; \forall b = 1,\dots,B$$

All rows are closed at the beginning

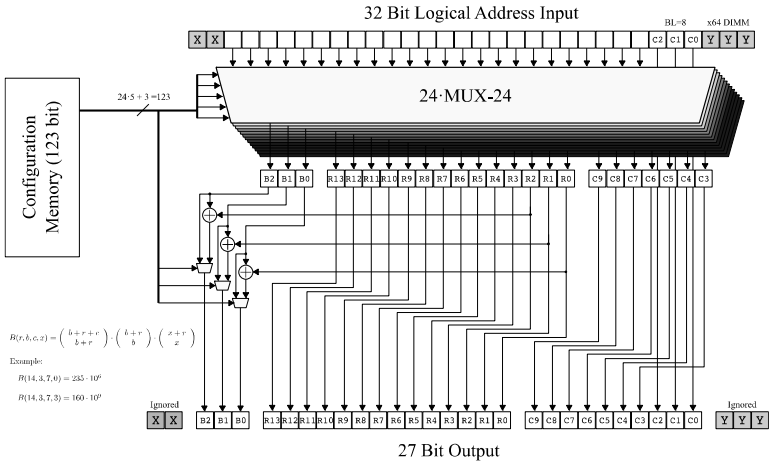
We could show if B=1 eq. Min-k-Cut ⇒ NP-Hard Problem

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

OPT Optimization Research Group

ConGen Methodology

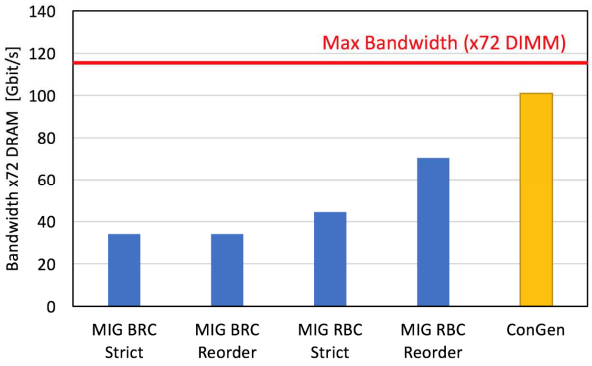
- Use configurable hardware template
- Find exact solution with minimal row misses under this HW constraints



MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Congen vs. COTS Controller

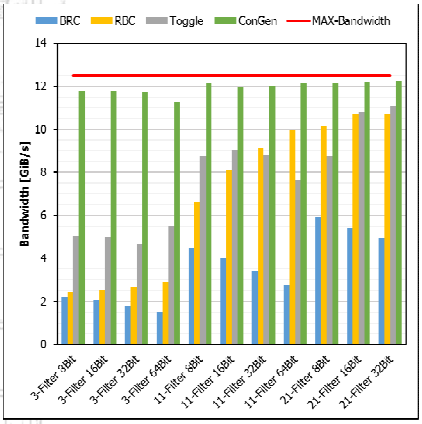
- Using Xilinx MIG Controller
- Holographic 3D image processing application
- X72 DDR3 DIMMs

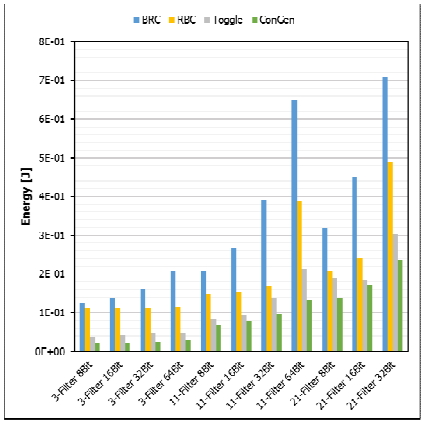


Only 9 LUTs necessary

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Convolutional Image Filter (1024x 576 Pixel)



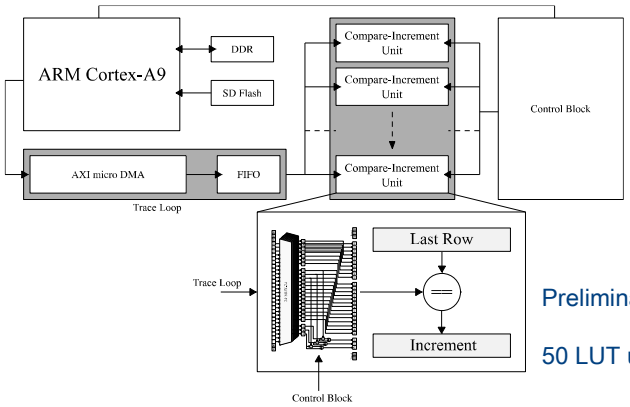


MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Future Work

Speeding-Up the Processing

- Branch & bound methods
- Dedicated FPGA accelerator for full enumeration



Preliminary Result:

50 LUT und 140 FF

Thanks for your attention

Further information on http://ems.eit.uni-kl.de