Minimum Energy Point Tracking for Self-Powered IoT Processors

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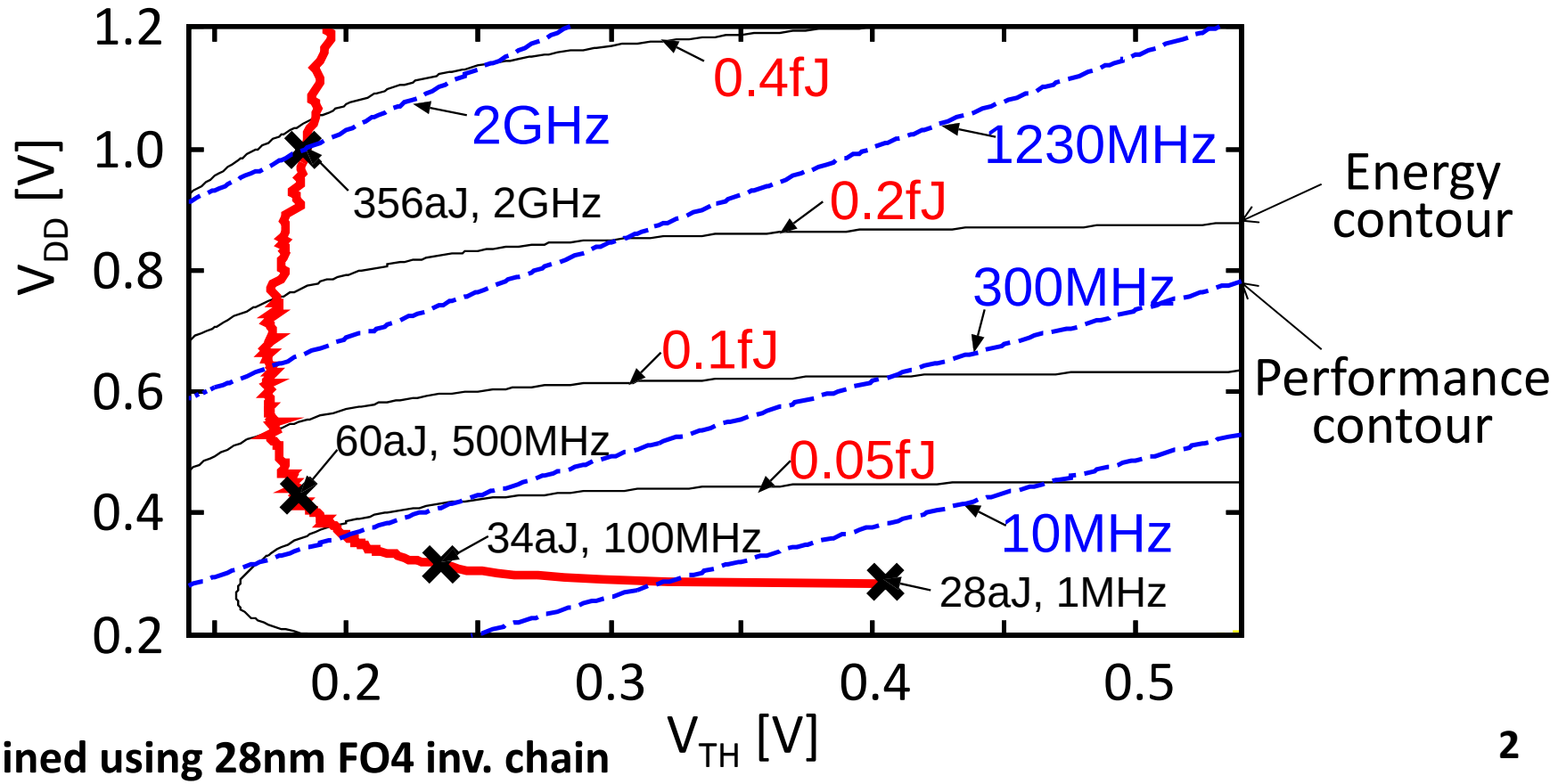
My Talk in MPSoC 2015

— Minimum Energy Point —

A set of V_{DD} and V_{TH}, which minimizes the energy consumption of a circuit for a given time constraint



Obtained using 28nm FO4 inv. chain

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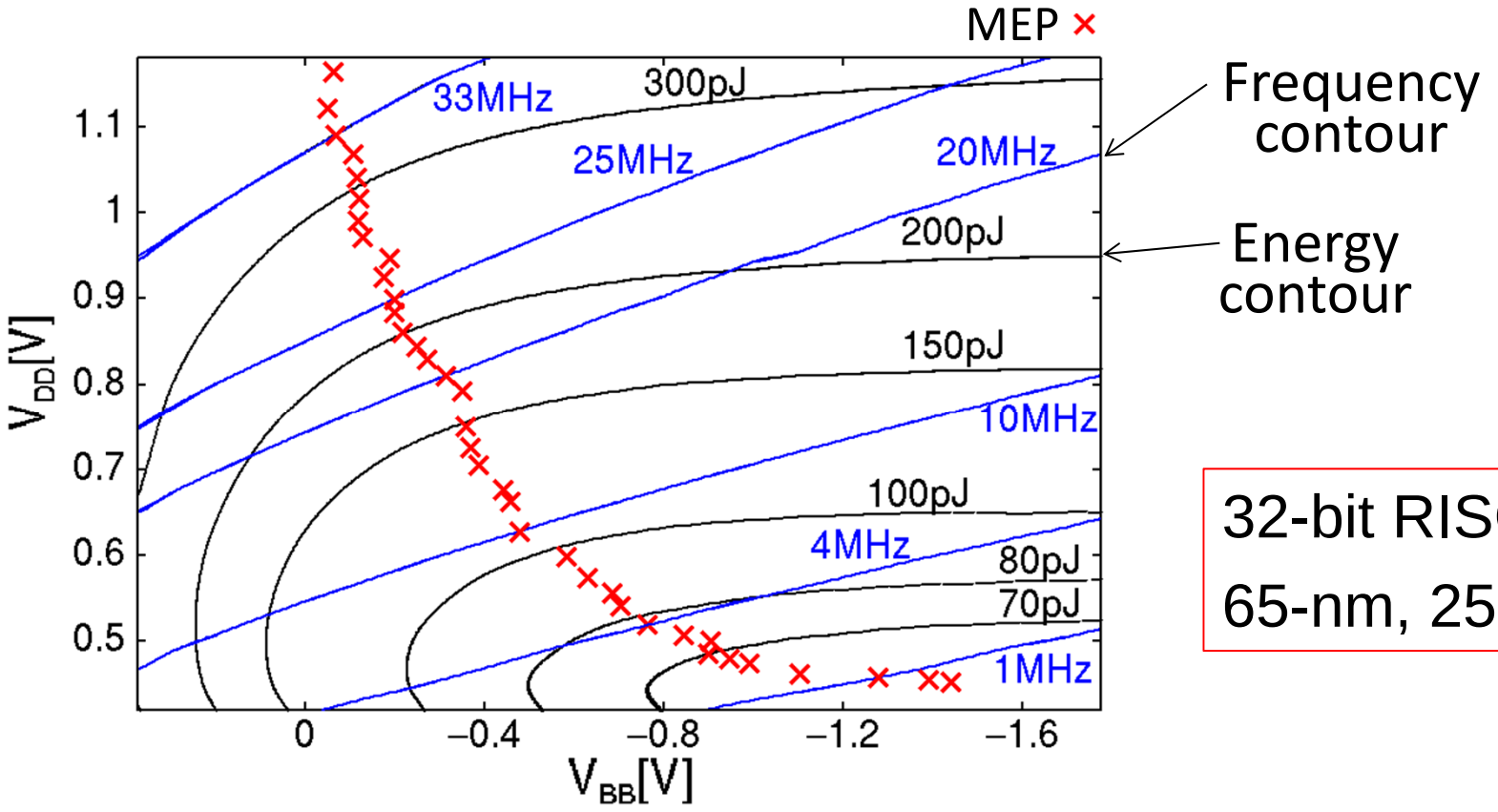
Minimum Energy Point in a Processor

MEP: tangent point of frequency and energy contours



32-bit RISC
65-nm, 25 ◦C

Obtained using post-layout simulation of a processor

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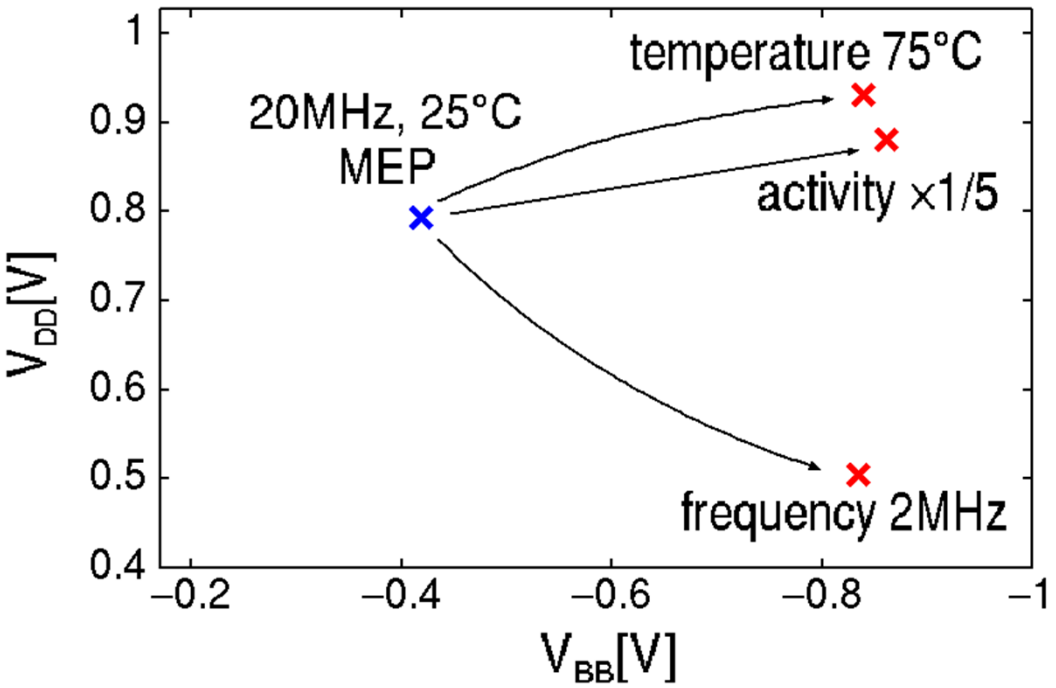
Motivation of Finding MEP

- MEP depends on operating conditions



- Frequency
- Temperature
- Activity factor

32-bit RISC processor
65-nm process

Goal: develop algorithm for tracking MEP

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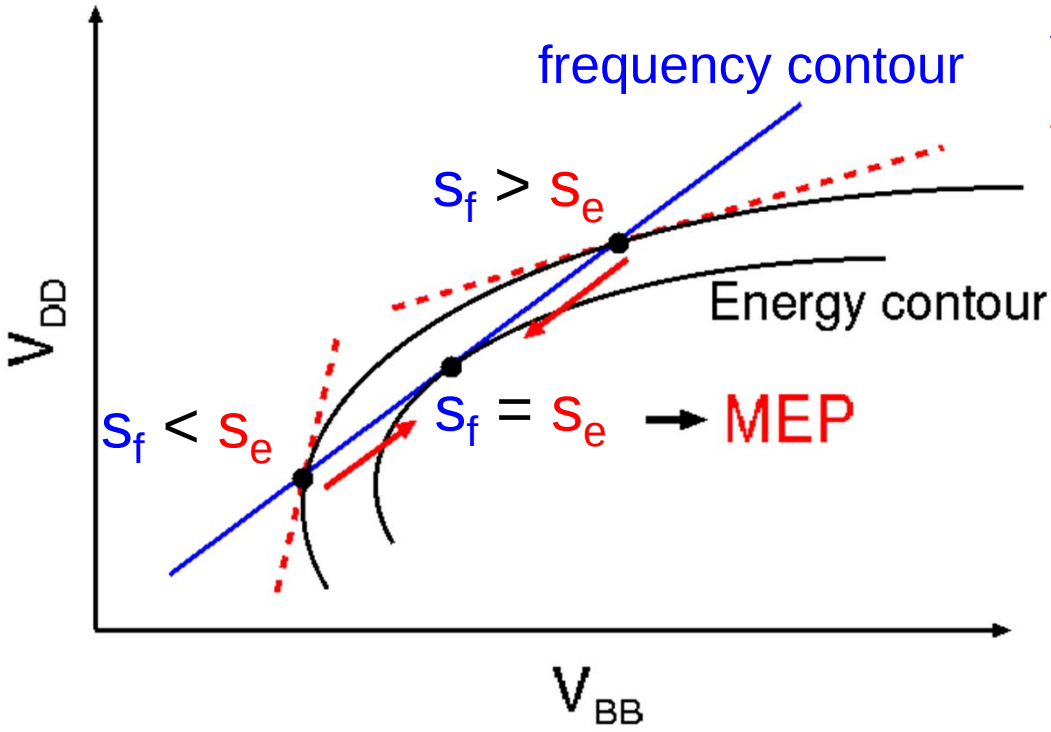
Concept of MEP Identification



s_f: slope of frequency contour

s_e: slope of energy contour

$s_f = s_e$ at MEP

$s_f > s_e$ ⇒ MEP exists lower left

$s_f < s_e$ ⇒ MEP exists upper right

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MEP Identification Function

s_f : slope of frequency contour

$$s_f = \frac{\alpha V_{DD}}{\alpha V_{DD} - (V_{DD} - V_{TH})} \quad \cdots \quad V_{DD} > V_{TH}$$

Control Parameters

$$s_f = 1 \quad \cdots \quad V_{DD} \leq V_{TH}$$

s_e : slope of energy contour

Observed Parameters

$$s_e = \frac{E_s V_{DD}}{(2E_d + E_s)} \cdot \frac{1}{N_s}$$

Linear to Temperature

Once E_d, E_s and T are obtained,
MEP identification can be easily done.

S. Hokimoto, T. Ishihara, and H. Onodera, “Minimum energy point tracking using combined dynamic voltage scaling and adaptive body biasing,” Proc. of *IEEE System-on-Chip Conference, Sep. 2016*

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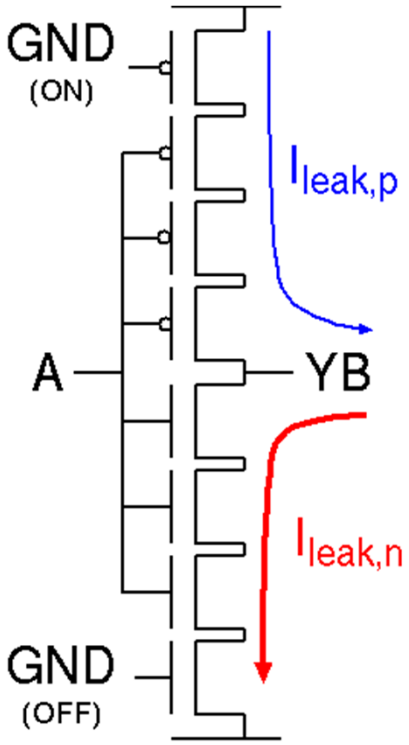
Leakage Sensor

- Leakage to digital converter [1]
- Leakage power is proportional to V_{DD} and oscillation frequency f_{leak}
- E_S is estimated from V_{DD} and f_{leak}
- k_s is calibrated at test-time



$$E_s = I_{leak} V_{DD} D = k_s f_{leak} V_{DD}{}^2 D$$

D: Delay of a critical-path replica

[1] I. Mahfuzul, J. Shiomi, T. Ishihara, and H. Onodera, “Wide-Supply-Range All-Digital Leakage Variation Sensor for On-Chip Process and Temperature Monitoring,” *IEEE Journal of Solid-State Circuits 2015*

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MEP Tracking Algorithm

1. Delay Tracking

Measure critical path delay

Find (V_{DD}, V_{BB}) which satisfy a given frequency requirement

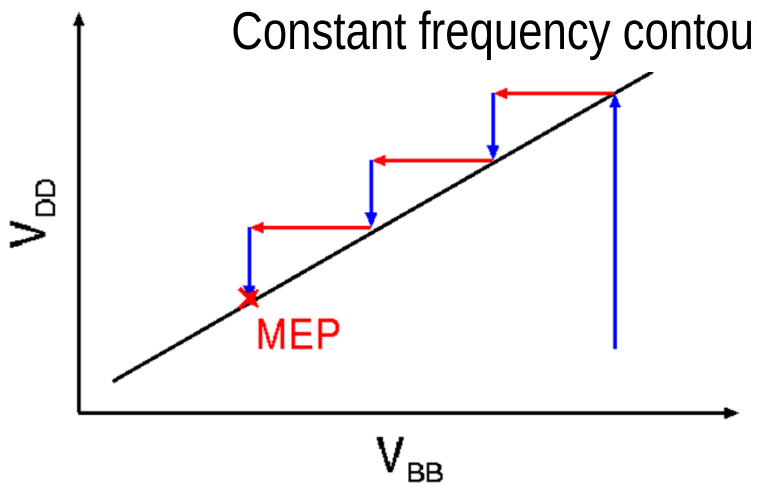
2. MEP Identification

(V_{DD}, V_{BB}) is MEP ?

yes → Finish

no

Update V_{DD} or V_{BB} to get close to MEP



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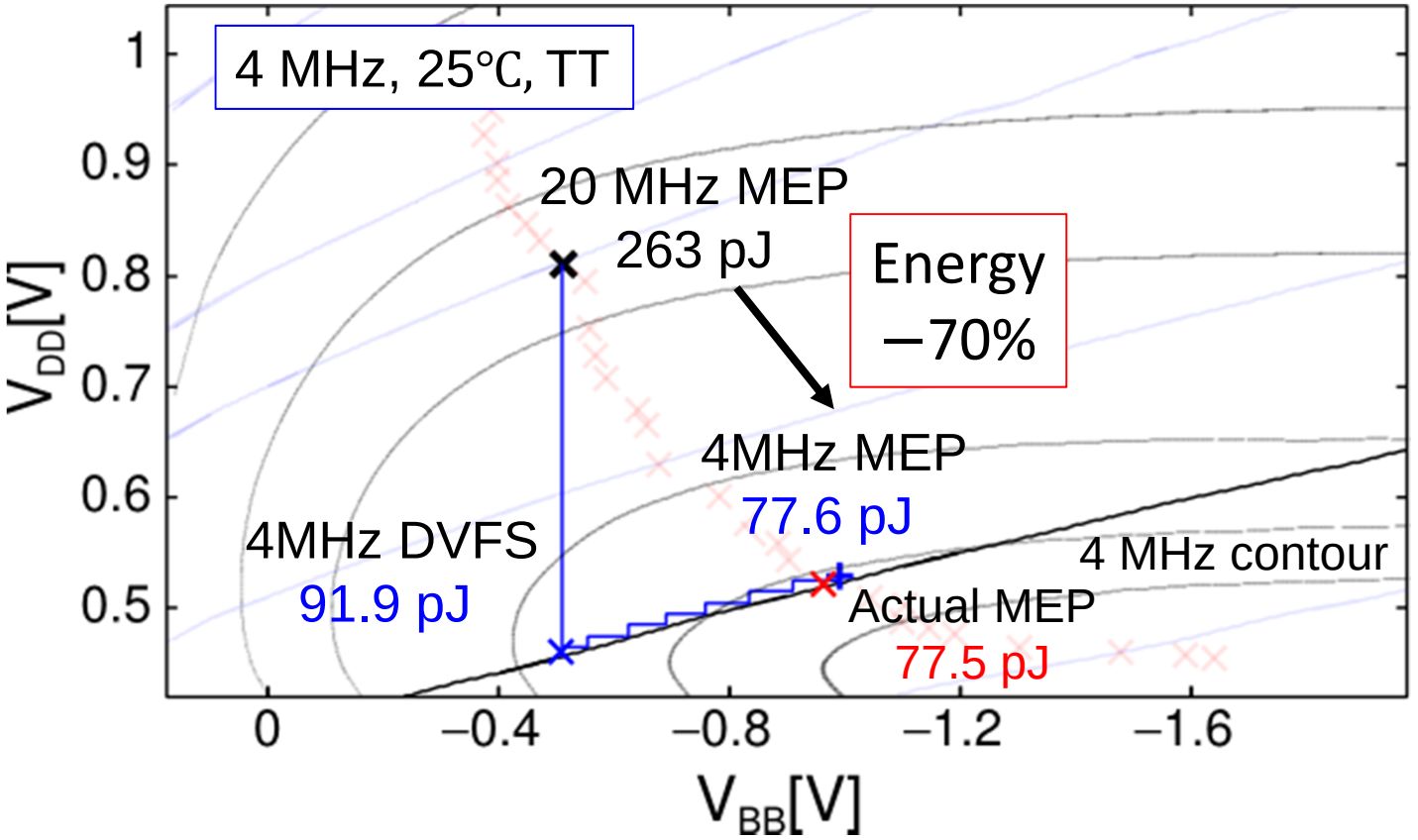
Result of MEPT (20MHz → 4MHz)



32-bit RISC processor

65-nm TT corner, 25 ◦C, 4 MHz

- 74% energy reduction obtained
- 16% energy reduction over DVFS
- The max tracking error is 1.2%

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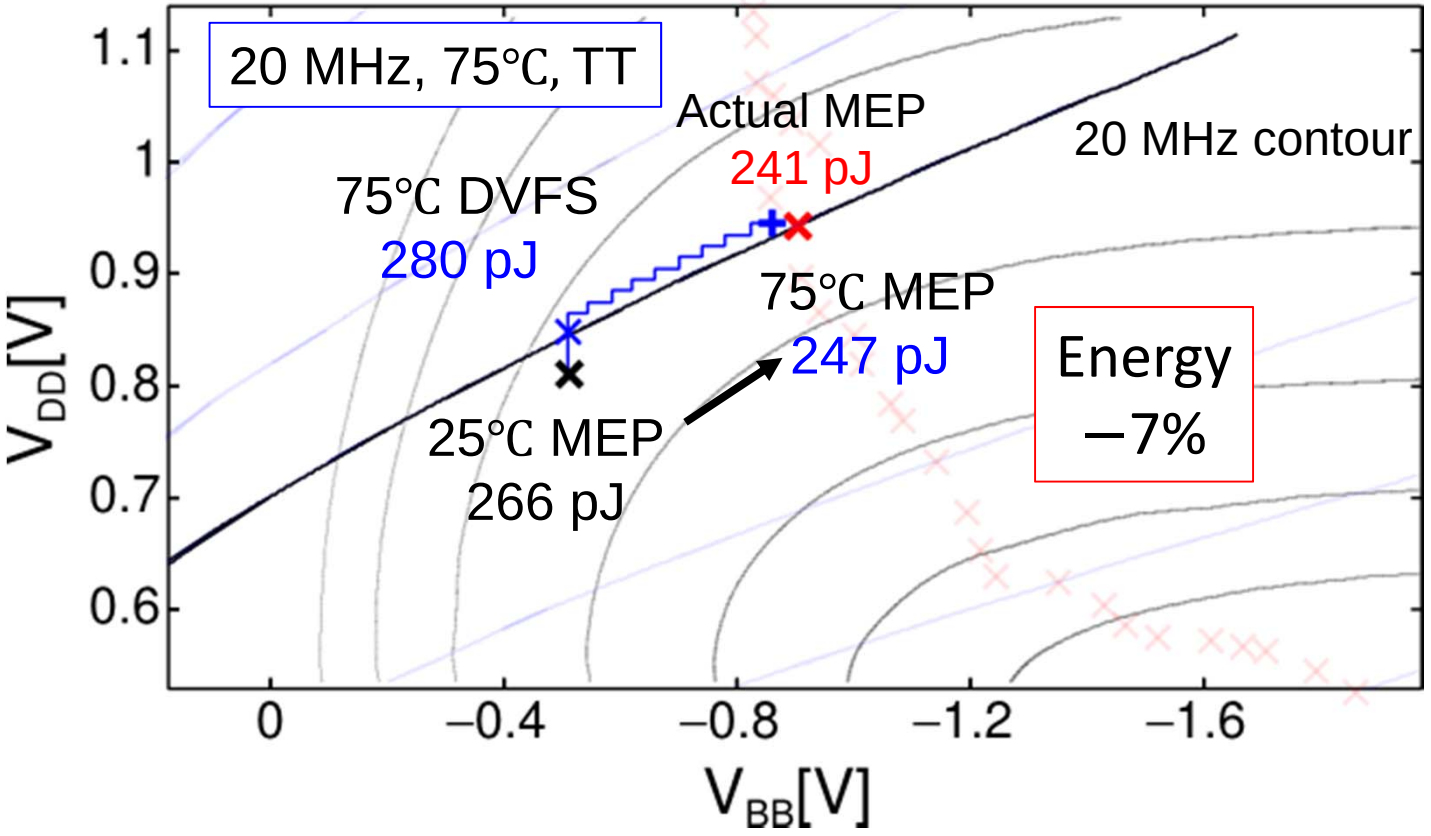
Result of MEPT (25°C → 75°C)



32-bit RISC processor

65-nm TT corner, 75 ◦C, 20 MHz

- 7% energy reduction obtained
- 12% energy reduction over DVFS
- The max tracking error is 2.5%

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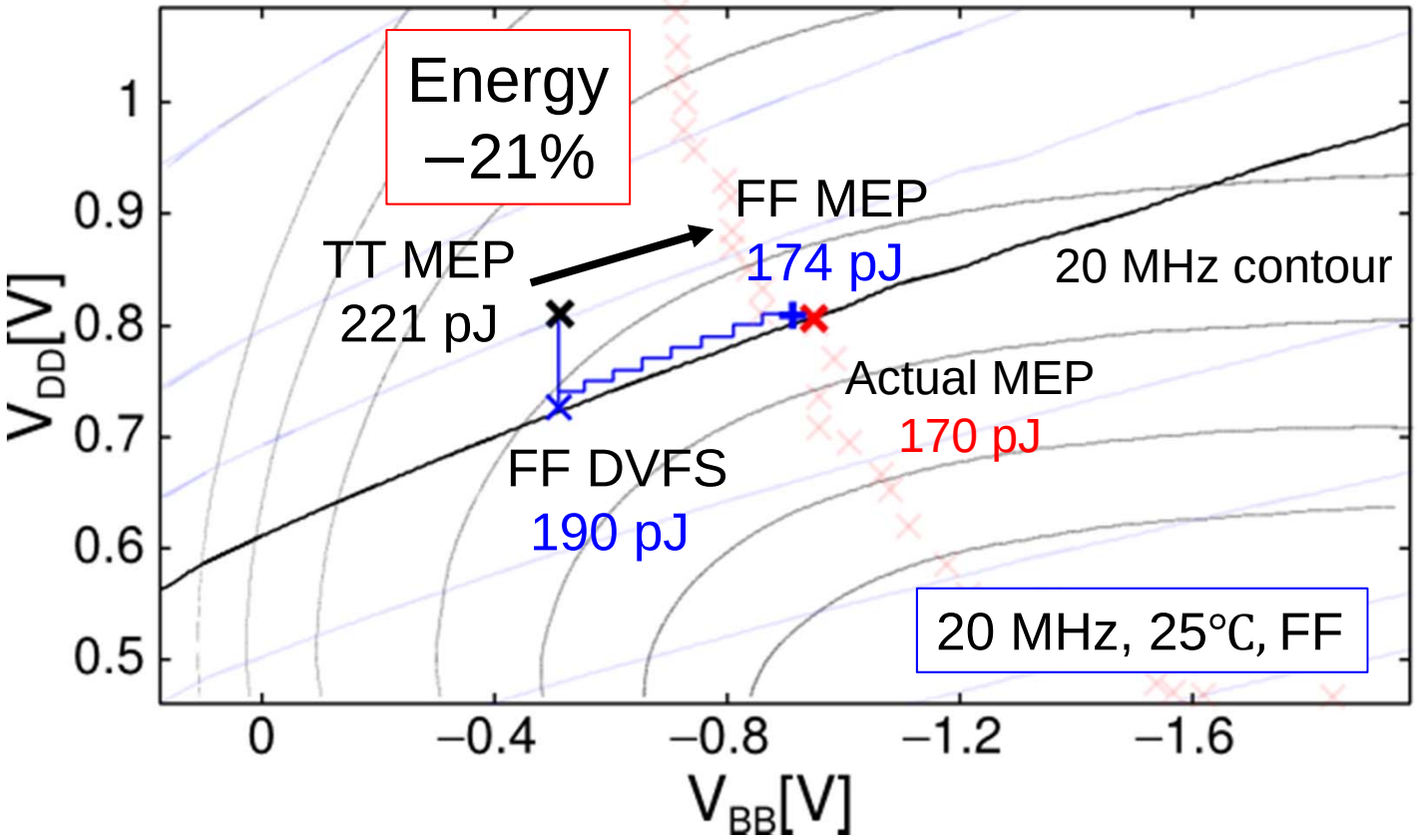
Result of MEPT (activity 1.0 → 0.2)



32-bit RISC processor

65-nm FF corner, 25 ◦C, 20 MHz

- 21% energy reduction obtained
- 8.4% energy reduction over DVFS
- The max tracking error is 2.4%

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Conclusion and Future Work

- MEPT algorithm proposed
  - Algorithm validated by 32-bit RISC processor
  - Tracking error is only 2.5% at the worst case
  - Large energy reduction observed
    - 70% reduction observed when 20MHz → 4MHz

- On-going work
  - Run-time measurement of *delay*, E_d, E_s and *temperature*