MPSoC'18 — 18th International Forum on MPSoC for Software-defined Hardware

SUNDAY, JULY 29

06:00 pm Registration
07:00 pm Welcome reception

MONDAY, JULY 30
ENABLING TECHNOLOGIES FOR MPSOCS

08:00 am Registration
08:30 am Opening

SESSION 1: KEYNOTE
CHAIR: PIERRE-EMMANUEL GAILLARDON

08:30 am Farhang Yazdani, *Broadpak, USA.*
Next Move: Heterogeneous Integration
09:30 am Break

SESSION 2: MINI-KEYNOTES
CHAIR: PIERRE-EMMANUEL GAILLARDON

10:00 am Fumio Arakawa, *The University of Tokyo, Japan.*
An efficient micro-architecture for cryptographic engine of IoT devices
10:12 am Eric Monchalin, *Atos, France.*
Think AI First
10:24 am Andreas Herkersdorf, *TU Munich, Germany.*
Regional Coherence and Near Memory Acceleration in Distributed-Shared-Memory Architectures
10:36 am Yoshifumi Sakamoto, *IBM Japan, Japan.*
Study to apply accelerator using FPA to learning server of self-driving vehicle
10:48 am Sungjoo Yoo, *Seoul National University, Korea.*
Towards 4-bit Hardware Accelerator for Very Deep Neural Networks
11:00 am Gabriela Nicolescu, *Ecole Polytechnique de Montréal, Canada.*
Security for smart applications
11:12 am Panel Discussion
12:12 pm Lunch

SESSION 3: IN-DEPTH/MINI-KEYNOTES
CHAIR: YOSHIFUMI SAKAMOTO

02:00 pm Yankin Tanurhan, *Synopsys, USA.*
There's Safety in Numbers: Heterogenous Processors for ADAS Applications
02:30 pm Gerhard Fettweis, *TU Dresden, Germany.*
On Designing a 5G MPSoC
03:00 pm Masaaki Kondo, *The University of Tokyo, Japan.*
Reinforcement Learning-Based Adaptive Power Management for Energy Harvesting IoT Devices
03:12 pm Tohru Ishihara, *Kyoto University, Japan.*
Minimum Energy Point Tracking Exploiting All-Digital On-Chip Sensors
03:24 pm Break

SESSION 4: IN-DEPTH/MINI-KEYNOTES
CHAIR: YOSHIFUMI SAKAMOTO

04:00 pm K. Charles Janac, *Arteris Inc., USA.*
Interconnect Physical Optimization
04:30 pm Takashi Miyamori, *Toshiba Corporation, Japan.*
200m-Range-Imaging LiDAR with Smart Accumulation Technique for Autonomous Driving Systems
05:00 pm Norbert When, *University of Kaiserslautern, Germany.*
The (DRAM) Memory Challenge in Computing Systems
05:12 pm Panel Discussion
07:00 pm Dinner

TUESDAY, JULY 31
HIGH PERFORMANCE COMPUTING

08:00 am Registration

SESSION 1: KEYNOTE
CHAIR: KEES VISSERS

08:30 am Paul Joyce, *Dell EMC, USA.*
IoT: Transforming Industries and Enabling Human Progress
09:30 am Break

TUESDAY, JULY 31
HIGH PERFORMANCE COMPUTING

SESSION 2: IN-DEPTH/MINI-KEYNOTES
CHAIR: KEES VISSERS

10:00 am Kerry Kelly, *University of Utah, USA.*
AQ&U: Using low-cost IoT solutions to understand and address local air-quality challenges

10:30 am Tsuyoshi Isshiki, *Tokyo Institute of Technology, Japan.*
C2RTL SoC Synthesis/Verification Framework for IoT Edge Devices

10:42 am Akihiko Shinya, *NTT Nanophotonics Center, Japan.*
Nanophotonics technology for low-latency and low-energy optical information processing

10:54 am Shinya Takamaeda, *Hokkaido University, Japan.*
QUEST: A Log-Quantized Deep Neural Network Engine with 3D Stacking SRAMs

11:06 am MarilynWolf, *Georgia Tech, USA.*
Smart Stacked Image Sensors

11:18 am Jiang Xu, *Hong Kong University of Science and Technology, Hong Kong.*
RSON: Silicon Photonic Network for Rack-Scale Computing System

11:30 am Panel Discussion

12:30 pm Lunch

SESSION 3: IN-DEPTH/MINI-KEYNOTES
CHAIR: YANKIN TANURHAN

02:00 pm Francois Neumann, *Safran Electronics & Defense, France.*
High performance computing within constraints of certification and embedded environment

02:30 pm Greg Nielson, *Nielson Scientific, USA.*
3D Silicon Nanofabrication of Multi-Functional Interposers for 3D Integration

03:00 pm Rolf Ernst, *Technische Universität Braunschweig, Germany.*
Model-based MPSOC Self-adaptation for Critical Systems

03:12 pm John Goodacre, *University of Manchester/Kaleao Ltd/ARM Ltd, UK.*
Designed for scale-out: Brain vs. Brawn

03:24 pm Break

SESSION 4: IN-DEPTH/MINI-KEYNOTES
CHAIR: Yankin Tanurhan

04:00 pm Kees Vissers, *Xilinx, USA*
Design and Analysis of Reduced Precision LSTM Networks on FPGA.

04:30 pm Pierre Paulin, *Synopsys, Canada.*
Challenges and Solutions for Future-Proof Neural Network Accelerators

05:00 pm Wei Zhang, *Hong Kong University of Science and Technology, Hong Kong.*
Static and Dynamic Hybrid Cache Management for CPU-FPGA Platforms

05:12 pm Panel Discussion

07:00 pm Dinner

WEDNESDAY, AUGUST 1
EMBEDDED SOFTWARE

08:00 am Registration

SESSION 1: KEYNOTE
CHAIR: GABRIELA NICOLESCU

08:30 am Ike Nassi, *TidalScale, USA.*
Software-Defined Servers

09:30 am Break

SESSION 2: IN-DEPTH/MINI-KEYNOTES
CHAIR: GABRIELA NICOLESCU

10:00 am Masaki Gondo, *eSOL Co., Ltd., Japan.*
Update on AUTOSAR Adaptive Platform and application of scalable distributed microkernels

10:30 am Arnaud Grasset, *Thales Research & Tech., France.*
Reliable Embedded Systems for Critical Applications

10:42 am Youn-Long Lin, *Professor at National Tsing Hua University, Taiwan.*
DRAM-Centric Accelerator Design for Large DNNs

10:54 am Gerd Ascheid, *RWTH Aachen University, Germany.*
Towards a Power Efficient Embedded DNN (Deep Neural Network) ASIP

11:06 pm Victor Grimblatt, *Synopsys, Chile.*
Smart Agriculture – How to Improve the Throughput of the Soil using IoT?

11:18 am Contest Winner

11:30 am Panel Discussion

12:30 pm Lunch

SESSION 3: IN-DEPTH/MINI-KEYNOTES
CHAIR: K. CHARLES JANAC

02:00 pm John Bainbridge, *NetSpeed Systems, USA.*
A Software-Defined SoC Interconnect Fabric for Enabling AI Applications

02:30 pm Yoshihiko Hirota & Masahiro Murakami & Yoshitaka Yaguchi, *Konica Minolta, Japan.*
Acceleration technology to support the evolution of next-generation MFP

WEDNESDAY, AUGUST, 1
EMBEDDED SOFTWARE

03:00 pm Ittetsu Taniguchi, *Osaka University, Japan.*
An Efficient Parts Counting Method based on Intensity Distribution Analysis for Industrial Vision Systems

03:12 pm Tsuyoshi Sato, *Pioneer, Japan.*
3D-LiDAR technology for high level autonomous driving systems and sensor interface requirements for SoC (ECU)

03:24 pm Panel Discussion
04:24 pm Speakers Meeting
05:30 pm Social Activity
08:00 pm Gala Dinner

THURSDAY, AUGUST 2
HETEROGENEOUS MPSOCS

08:00 am Registration

SESSION 1: KEYNOTE
CHAIR: FRÉDÉRIC, PÉTROT

08:30 am Shuichi Yamane, *Socionext Inc., Japan.*
Hyper scale server

09:30 am Break

SESSION 2: MINI-KEYNOTES
CHAIR: FRÉDÉRIC, PÉTROT

10:00 am Nicolas Ventroux, *CEA-List, France.*
Neural Computing in Embedded Systems

10:12 am Yuko Hara-Azumi, *Tokyo Institute of Technology, Japan.*
Highly-Scalable and Flexible Multicore Processors with Limited ISAs

10:24 am Hiroki Matsutani, *Keio University, Japan.*
Accelerating Anomaly Detection Algorithms on FPGA-Based High-Speed NICs

10:36 am Kees van Berkel, *Ericsson, Eindhoven University of Technology, The Netherlands.*
Exascale Computing for Radio Astronomy: Mapping Dataflow Graphs to Circuits

10:48 am Jishen Zhao, *UCSD, USA.*
Heterogeneous Processing-in-memory for Energy-efficient CNN Training

11:00 am Anca Molnos, *CEA-Leti, France.*
Towards secure, low-power IoT

11:12 am Panel Discussion
12:12 pm Lunch

SESSION 3: IN-DEPTH/MINI-KEYNOTES
CHAIR: TSUYOSHI ISSHIKI

02:00 pm Shahar Kvatinsky, *Technion - Israel Institute of Technology, Israël.*
Real Processing-in-Memory with Memristive Memory Processing Unit

02:30pm Pei-Lin Pai, *Winbond, Taiwan.*
Emerging Memory for Artificial Intelligence and IoT

03:00 pm Yoshinori Takeuchi, *Kindai University, Japan.*
Coding Analysis for Spiking Neural Network Models

03:12 pm Hiroyuki Tomiyama, *Ritsumeikan University, Japan.*
Malleable Task Scheduling for Multi-/Many-core Platforms

03:24 pm Break

SESSION 4: IN-DEPTH/MINI-KEYNOTES
CHAIR: TSUYOSHI ISSHIKI

04:00 pm Yuan Xie, *UCSB, USA.*
Memory-centric architecture to close the gap between compute and memory

04:30 pm Yuichi Nakamura, *NEC Corp., Japan.*
SX-Aurora Tsubasa, HPC meets machine learning

05:00 pm Frédéric Rousseau, *TIMA Lab - Grenoble University, France.*
Communication Consistency for Hardware Context Switch on Heterogeneous FPGAs

05:12 pm Panel Discussion
07:00 pm Dinner

FRIDAY, AUGUST 3
DEEP LEARNING AND NEURAL NETWORKS

08:00 am Registration

SESSION 1: KEYNOTE
CHAIR: WEI ZHANG

08:30 am Rob Aitken, *ARM, UK.*
Buzzword spotting: Machine learning at the edge of a trillion node IoT

09:30 am Break

SESSION 2: IN-DEPTH/MINI-KEYNOTES
CHAIR: WEI ZHANG

10:00 am Peter van der Made, *BrainChip Inc., USA.*
Introducing the Akida Spiking Neural Network Reconfigurable NeuroSoC

10:30 am Masatoshi Ishii, *IBM Research - Tokyo, Japan.*
NVM neuromorphic core with on-chip learning capability

11:00 am Song Yao, *DeePhi Tech, China.*
The Evolution of Deep Learning Accelerators Upon Evolution of Deep Learning Algorithms

11:12 am Danilo Pau, *STMicroelectronics, Italy.*
The (Artificial Intelligent) Cyber-Physical Revolution: From Theory to Practice

11:24 am Frédéric, Pétrot, *TIMA Lab - Grenoble University, France.*
Acceleration of software simulation in dynamic binary translation

11:36 am Panel Discussion

11:40 am Closing

12:40 pm Lunch