MPSoC'19 Program

July 7 (Sunday) Networking

19:00 Welcome Reception

July 8 (Monday) Automotive and AI

Session 1 (Chairs: Tsuyoshi Isshiki and Hiroyuki Tomiyama)

8:50 Opening
9:00 Hideki Sugimoto (NSITEXE, Japan) Architecture Challenge for Future Automotive or Embedded Compute SoC
10:00 Break
10:30 Masaaki Kondo (The University of Tokyo, Japan) A Design of Scalable Deep Neural Network Accelerator Cores with 3D Integration
10:42 Eric Monchalin (ATOS, France) Are next generation architectures suitable?
10:54 Andreas Herkersdorf (TU Munich, Germany) Near Memory Accelerators for Efficient Inter-Tile Communication in Distributed-Shared-Memory Architectures
11:06 Gerd Ascheid (RWTH Aachen University, Germany) Scalability Aspects of a Many-Core ASIP Platform targeted at Convolutional Neural Networks
11:18 Yoshifumi Sakamoto (IBM Japan, Japan) Study to apply accelerators using FPGA to learning path-planning of self-driving vehicles
11:30 Masahiro Murakami & Yuji Okamoto (Konica Minolta, Japan) Acceleration Technology to Realize Super Resolution Processing of Scanned Image for MFP
11:42 Panel
12:30 Lunch

Session 2 (Chair: Frédéric Pétrot)

14:00 Arnaud Grasset (Thales Research & Tech., France) A Look at Computer Architectures for Mission-Critical Embedded Systems
14:30 Timothée Levi (University of Tokyo, Japan / University of Bordeaux, France) Biomimetic Spiking Neural Network and Neurohybrid systems for AI and biomedical
15:00 K. Charles Janac (Arteris Inc., USA) Interconnect for Machine Learning
15:30 Break
16:00 Atsushi Hasegawa (Renesas Electronics, Japan) Smart Factory with Artificial Intelligence at Endpoint
16:30 Hironori Kasahara (Waseda Univ., Japan) Green Multicore Compiler
17:00 Kiyoung Choi (Seoul National University, Korea) Algorithms and Architectures for Efficient Neural Processing
17:30 Panel
19:00 Dinner

July 9 (Tuesday) Photonics and HPC

Session 3 (Chairs: Ahmed Jerraya and Yoshinori Takeuchi)

9:00 Naim Ben-Hamida (CIENA, Canada) A path to 1Tb/s Coherent Optical Modem: From Light to Silicon
10:00 Break
10:30 Shuichi Yamane (Socionext Inc., Japan) Benefit of flexible multi-core server
10:42 Masaki Gondo (eSOL Co.,Ltd., Japan) SHIM 2.0 - an update to the new way to describe hardware for software tools
10:54 Wei Zhang (Hong Kong University of Science and Technology, Hong Kong) Modeling and Optimization of High-Level Synthesis for FPGA
11:06 Jishen Zhao (UCSD, USA) Towards Safety-Aware Computing System Design in Autonomous Vehicles
11:18 Koji Inoue (Kyushu Univ., Japan) Towards Ultra High-Speed Superconducting Computing
11:48 Panel
12:30 Lunch

Session 4 (Chair: Norbert Wehn)

14:00 Sunghyun Lee (Openedges Technology, Inc., Korea) Memory Access Optimization for Modern DRAM Devices
14:30 Takashi Miyamori (Toshiba Electronic Devices & Storage Corporation, Japan) DNN-Accelerated Multi-core SoC for Automotive Applications
15:00 Hiroyuki Tomiyama (Ritsumeikan Univ., Japan) Static Scheduling of Parallel Tasks
15:12 Frederic Rousseau (TIMA, France) Lockality: a Scalable Synchronization Lock for MPSoCs
15:24 Break
16:00 Ashkan Seyedi (HP Labs, USA) Recent advances on WDM Silicon Photonics Devices for HPC Applications
16:30 Benoît de Dinechin (KALRAY, France) MPPA3 Manycore Processor for Intelligent Systems
17:00 Gerhard P. Fettweis (TU Dresden, Germany) A first step to building a 6G HW/SW platform
17:30 Panel
19:00 Dinner

July 10 (Wednesday) Advanced Design

Session 5 (Chairs: Tohru Ishihara and Youn-Long Lin)

9:00 Hiroyuki Kitayama (IBM, Japan) Trend and Industrial Usage of Advanced Technology (AI, Blockchain, New Computing etc.)
10:00 Break
10:30 Victor Grimblatt (Synopsys Chile R&D Center, Latin America) An SoC for IoT Applied to Smart Agriculture
10:42 Jiang Xu (Hong Kong University of Science and Technology, Hong Kong) BOSIM: A Comprehensive Electro-Optical Model for Silicon Photonic Switches
10:54 Yoshinori Takeuchi (Kindai University, Japan) Challenges for processor instruction extension in MPSoC Era
11:06 Ittetsu Taniguchi (Osaka University, Japan) Challenges for online optimization of drone path planning problem
11:18 Norbert Wehn (University of Kaiserslautern, Germany) Channel Coding for Tb/s Communications
11:30 Frédéric Pétrot (TIMA Lab, Grenoble University, France) A Scalable Sharing Set Management Approach for Large Scale MPSoC
11:42 Panel
12:30 Lunch

Session 6 (Chair: Kees Vissers)

14:00 Hideki Takase (Kyoto Univ. / JST PRESTO, Japan) mROS: How to integrate ROS components into the embedded devices
14:30 Tamon Sadasue (Ricoh, Japan) Scalable Logic Architecture for Accelerating Gradient Boosted Tree Learning
15:00 Kees van Berkel (Technical University Eindhoven, The Netherlands) Exascale Computing for Radio Astronomy: Mapping Pulsar Search on Dataflow
15:12 Shinya Takamaeda (Hokkaido University, Japan) Model/Architecture Co-design for Accurate Binary Neural Network
15:24 Panel
16:30 Speakers Meeting
18:00 Social Dinner

July 11 (Thursday) Annealing and AI

Session 7 (Chairs: Tohru Ishihara and Sungjoo Yoo)

9:00 Masanao Yamaoka (Hitachi, Japan) An In-memory Computing Accelerator, CMOS Annealing Machine, to Solve Combinatorial Optimization Problems
10:00 Break
10:30 Pierre Paulin (Synopsys, Canada) Scaling Deep Neural Network Accelerator Performance
10:42 Kees Vissers (Xilinx, USA) Versal: The New Xilinx Adaptive Compute Acceleration Platforms (ACAP) in 7nm
10:54 Youn-Long Lin (National Tsing Hua University, Taiwan) SOC Design of a Neural Network for Real-Time Semantic Segmentation of 2Kx1K@60fps Video
11:06 Lorena Anghel (Grenoble Institute of Technology, University Grenoble-Alpes, Grenoble, France) On Dependability of Spiking Neural Networks
11:18 Song Yao (DeePhi Tech, China) Xilinx AI Solutions with DeePhi Technologies
11:30 Panel
12:30 Lunch

Session 8 (Chair: Pierre Paulin)

14:00 Yuichi Nakamura (NEC Corp., Japan) Real Quantum Annealing, Architecture and Applications
14:30 Yankin Tanurhan (Synopsys, USA) Evolving Vision and Deep Neural Network Processors for Emerging Applications in the Edge
15:00 Break
15:30 Gabriela Nicolescu (Ecole Polytechnique de Montréal, Canada) Security for AI-based applications
15:42 Fumio Arakawa (The University of Tokyo, Japan) Trusted Execution Environment (TEE) with Open Processor Cores
15:54 Tsuyoshi Isshiki (Tokyo Institute of Technology, Japan) CNN Training HW Architecture Design Using C2RTL SoC Synthesis/Verification Framework
16:06 Tohru Ishihara (Nagoya University, Japan) Near-Threshold Cache Architecture for Ultra-Low Energy Computing
16:18 Marilyn Wolf (Georgia Tech, USA) Thoughts on Edge Intelligence
16:30 Nicolas Ventroux (CEA-List, France) Let's FACE the Future of Automotive E/E Architectures
16:42 Yuan Xie (UCSB, USA)
16:54 Panel
19:00 Dinner

July 12 (Friday) Photonics, Memory and AI

Session 9 (Chair: Yankin Tanurhan)

9:00 Akihiko Shinya (NTT Nanophotonics Center, Japan) Nanophotonics Technology for Photonic Integrated Circuits
9:30 Yukoh Matsumoto (TOPS Systems, Japan) Challenges on Designing Parallel Processing for realizing Real-Time Applications
10:00 Break
10:30 Masatoshi Ishii (IBM Research - Tokyo, Japan) On-chip trainable spike-based neuromorphic core using phase change memory as synapse
10:42 Sungjoo Yoo (Seoul National University, Korea) Reinforcement learning-based optimization for solid state disks
10:54 Hiroki Matsutani (Keio University, Japan) An On-Device Learning Approach for Unsupervised Anomaly Detection
11:06 John Goodacre (Kaleao Limited, UK) Reusable Arm computational chiplet with 128bit shared global address space access
11:18 Panel
12:30 Lunch