A Cell-based DRAM for Fully Synthesizable PiM Accelerator Design

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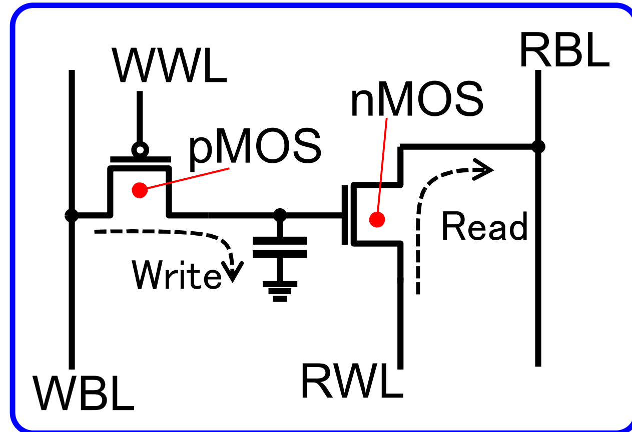
(mostly done by Tai-Feng Chen)

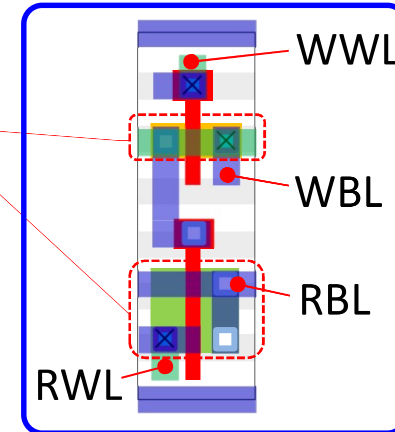
My Talk at MPSoC 2023

Gein Cell DRAM bit-cell

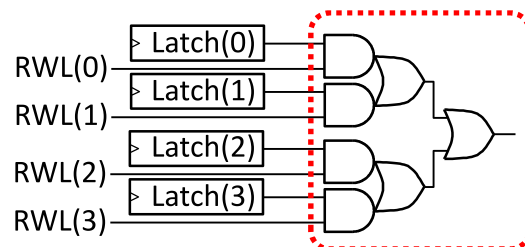


P-N pairing for
Standard-Cell friendly
layout structure

Cell-layout example



Traditional
Standard-Cell-Memory

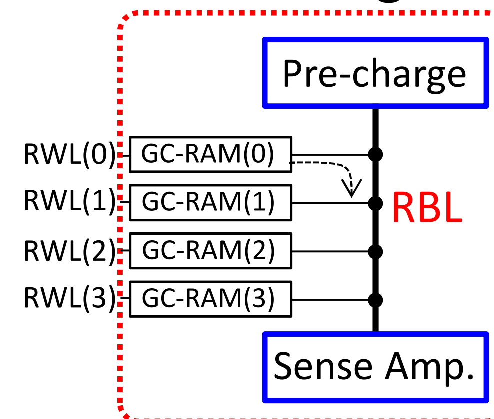


MUX: Large area

Eliminate MUX cells
from readout circuit

Pack into a std cell

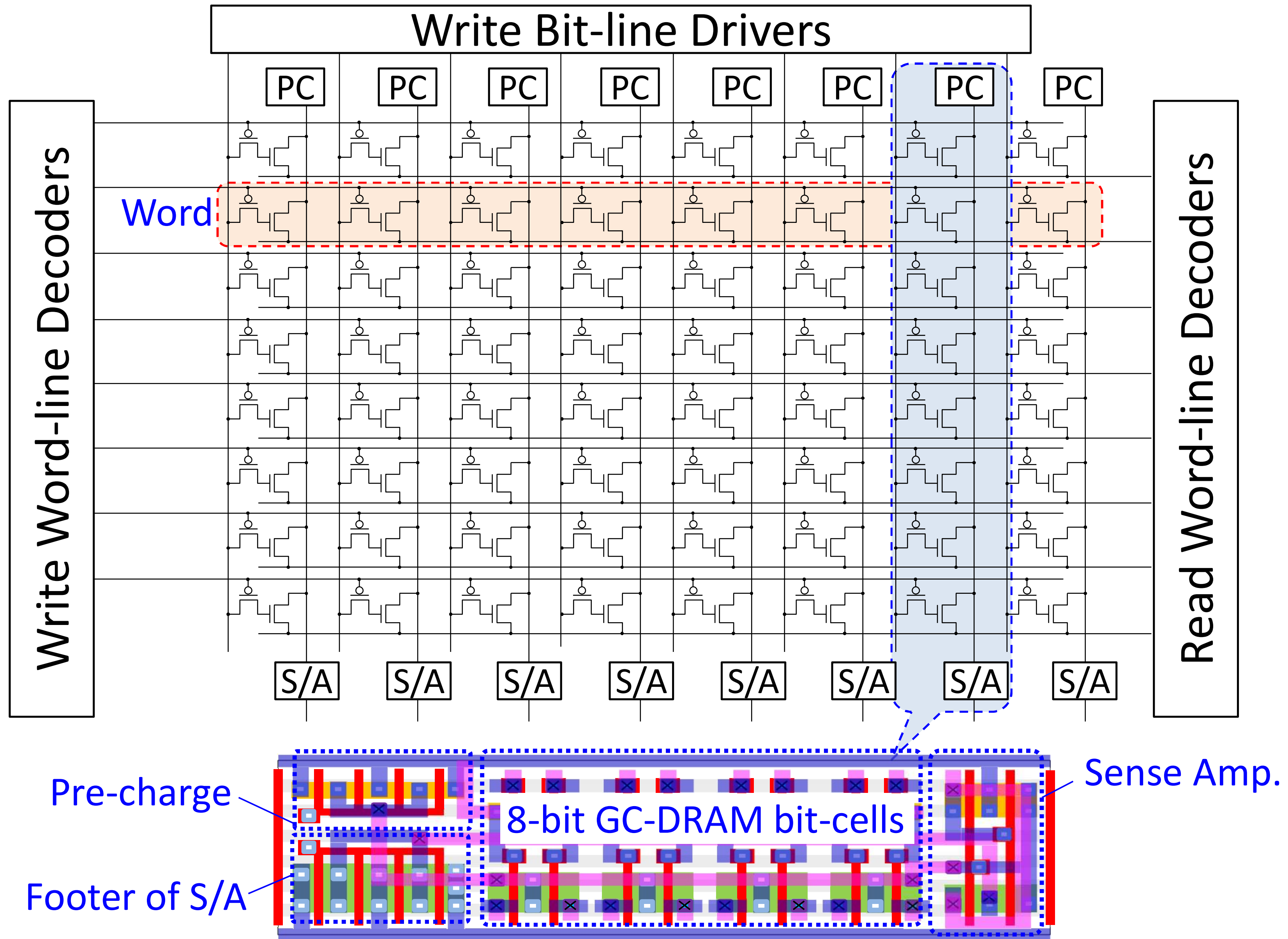
Our design



Compact wired-OR

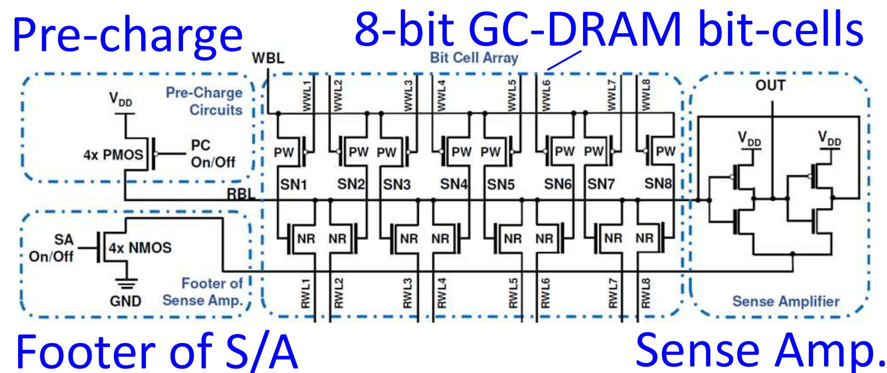
A. Teman, et al., “Power, Area, and Performance Optimization of Standard Cell Memory Arrays Through Controlled Placement”, ACM TODAES, vol.21, No.4, Article 59, May 2016.

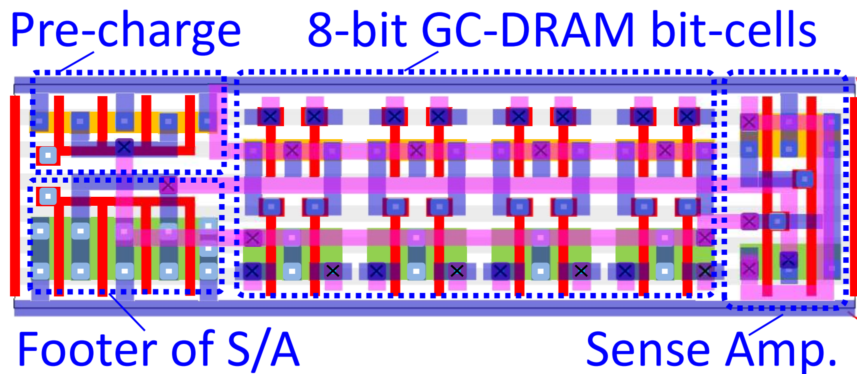
DRAM block as a Standard Cell

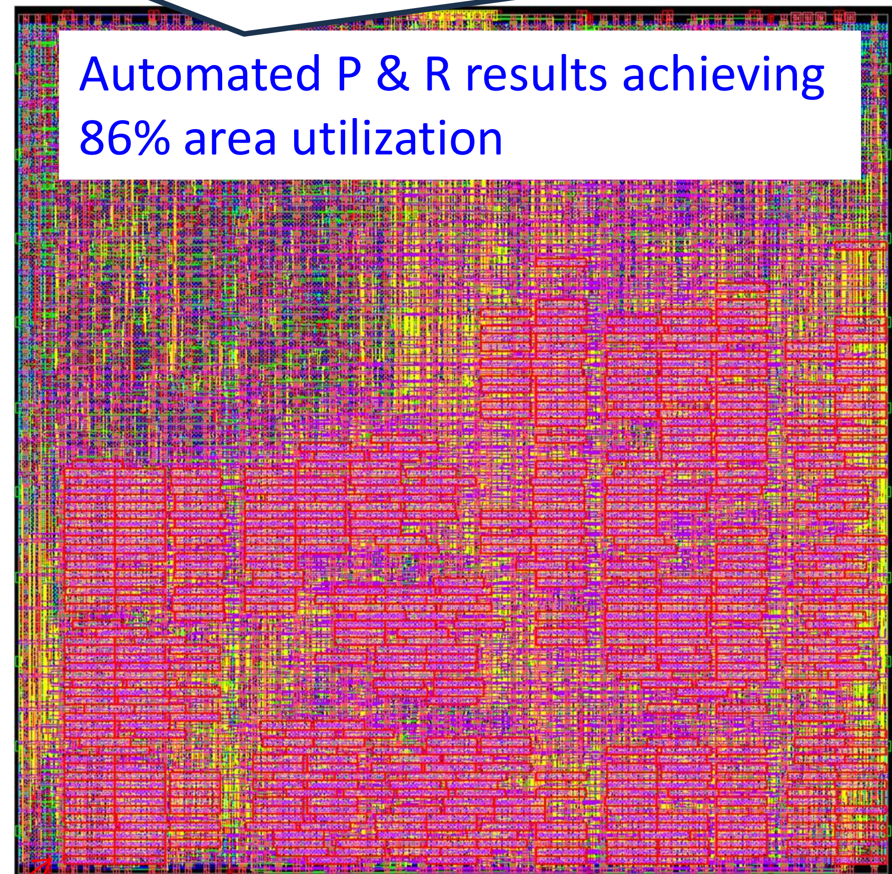


Processing in DRAM

A 128kb (16-word x 32-bit x 256 sets) PiM circuit where cell-based DRAMs, address decoders, word-line drivers, and simple MAC units are placed and routed all together using a commercial APR tool.







Red rectangles show the cell-based DRAM

Area and Energy Comparison

	Full-custom GC-DRAM [1]	Full-custom SRAM [2]	Our previous work [3]	This work
Technology	65 nm	55 nm	65nm	55 nm
Bit-cell Type	GC-DRAM	6T-SRAM	Latch-based	GC-DRAM
Voltage [V]	1.1	1.0 - 0.6	0.35	0.9 - 0.4
Frequency [MHz]	667	940@1.0V 360@0.6V	20@0.35V	60.6@0.9V 34.0@0.4V
Bit-cell size [μm²]	0.48	0.62		0.595
Area [μm²/bit]	0.71	0.96	6.82	*1.791
Energy [fJ/bit]	1.74	94.9@1.0V 48.7@0.6V	8.8@0.35V	23.6@0.9V 3.7@0.4V

3.8x smaller

13x smaller

*Includes cell-based DRAMs, address decoders, and word line drivers.

[1] K. C. Chun, et al., IEEE JSSC, vol. 47, no. 2, pp. 547-559, 2012.

[2] Y.-W. Lin, et al., ISLPED, pp.79-84, 2012.

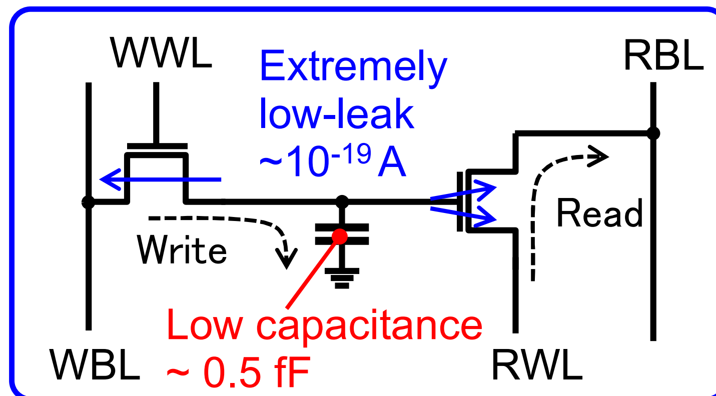
[3] J. Shiomi, et al., Integration, vol.65, 2019.

Exploit IGZO to Extend Retention

- Short retention issue in MOS-based GC-DRAM
  - Gate capacitance is ~0.5 fF and ~5 μs retention time
- Indium-Gallium-Zinc-Oxide Thin-Film Transistors
  - Capacitor-less, long-Retention time (> 400s)

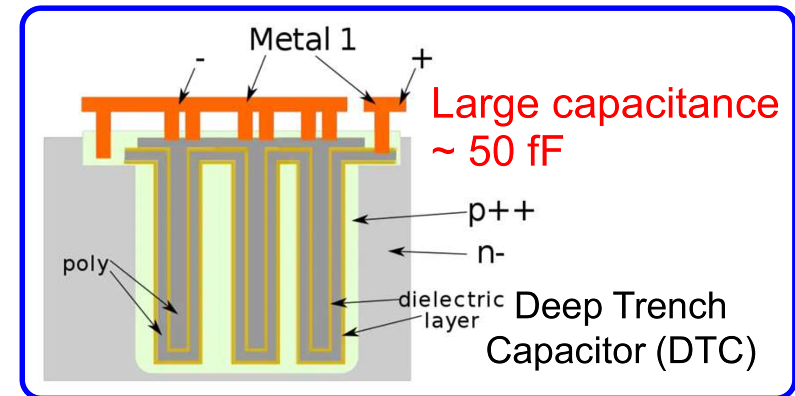
IGZO-DRAM

Low capacitance but low-leak



Traditional Deep Trench DRAM

Large capacitance but normal-leak

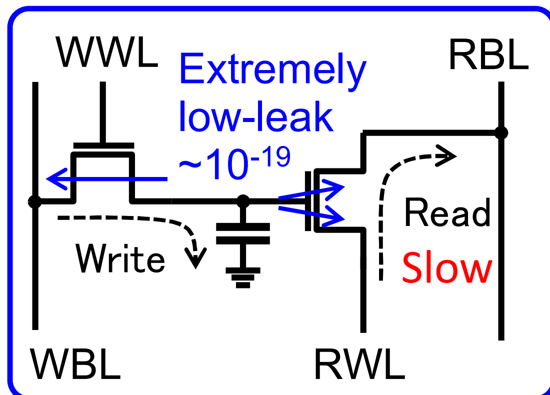


A. Belmonte *et al*., "Capacitor-less, Long-Retention (>400s) DRAM Cell Paving the Way towards Low-Power and High-Density Monolithic 3D DRAM," *proc. IEEE IEDM* 2020, pp. 28.2.1-28.

IGZO and MOS Hybrid Structure

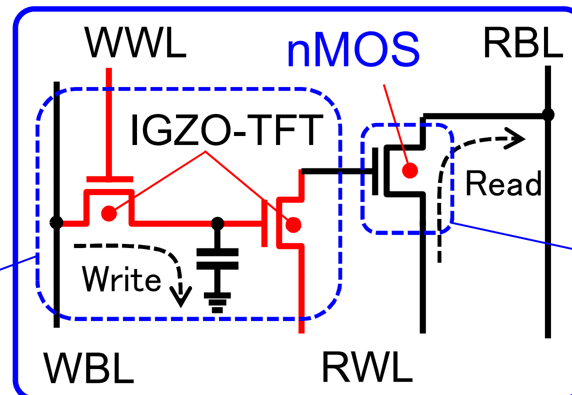
- Indium-Gallium-Zinc-Oxide Thin-Film Transistors
  - Pros: Monolithically stacked 3D structure is possible
    - Can construct in metal layer and low process cost
  - Pros: Capacitor-less, long-Retention time (> 400s)
  - Cons: Slow read access compared with MOSFET
    - This prevent IGZO-DRAM from further scaling
  - Solution: IGZO and MOS hybrid structure

IGZO-only configuration



Keep long retention time by IGZO-TFT

IGZO & nMOS hybrid



High drive current by MOSFET

Conclusions

- Automated P & R with cell-based DRAM
  - APR using commercial tool is demonstrated
    - MAC units and GC-DRAMs are closely P & R together
  - 3.8X better area efficiency than latch-based SCM
  - 13X better energy efficiency than 6T-SRAM
- Future Research Direction
  - IGZO and MOS hybrid 3D structure
    - Lower process cost than traditional deep trench structure
    - Extend retention time w/o degrading access time