MPSoC'18 — 18th International Forum on MPSoC for Software-defined Hardware

SUNDAY, JULY 29

6:00 pm Registration
7:00 pm Welcome reception

MONDAY, JULY 30
ENABLING TECHNOLOGIES FOR MPSOC

8:00 am Registration (continued)

SESSION 1: KEYNOTE

8:30 am Farhang Yazdani, *Broadpak, USA.*
Next Move: Heterogeneous Integration
9:30 am Break

SESSION 2: MINI-KEYNOTES

10:00 am Fumio Arakawa, *The University of Tokyo, Japan.*
10:12 am Eric Monchalin, *Atos, France.*
Think AI First
10:24 am Andreas Herkersdorf, *TU Munich, Germany.*
Regional Coherence and Near Memory Acceleration in Distributed-Shared-Memory Architectures
10:36 am Yoshifumi Sakamoto, *IBM Japan, Japan.*
10:48 am Sungjoo Yoo, *Seoul National University, Korea.*
Towards 4-bit Hardware Accelerator for Very Deep Neural Networks
11:00 am Gabriela Nicolescu, *Ecole Polytechnique de Montréal, Canada.*
11:12 am Panel discussion
12:15 pm Lunch

SESSION 3: IN-DEPTH/MINI-KEYNOTES

2:00 pm Yankin Tanurhan, *Synopsys, USA.*
2:30 pm Gerhard Fettweis, *TU Dresden, Germany.*
On Designing a 5G MPSoC
3:00 pm Masaaki Kondo, *The University of Tokyo, Japan.*
3:12 pm Tohru Ishihara, *Kyoto University, Japan.*
Minimum Energy Point Tracking Exploiting All-Digital On-Chip Sensors
3:24 pm Break

SESSION 4: IN-DEPTH/MINI-KEYNOTES

4:00 pm K. Charles Janac, *Arteris Inc., USA.*
Interconnect Physical Optimization
4:30 pm Pierre Paulin, *Synopsys, Canada.*
Challenges and Solutions for Future-Proof Neural Network Accelerators
5:00 pm Norbert When, *University of Kaiserslautern, Germany.*
The (DRAM) Memory Challenge in Computing Systems
5:12 pm Panel discussion
8:00 pm Dinner

TUESDAY, JULY 31
HIGH PERFORMANCE COMPUTING

SESSION 1: KEYNOTE

8:30 am Vance Checketts & Paul Joyce, *Dell EMC, USA.*
9:30 am Break

SESSION 2: MINI-KEYNOTES

10:00 am Anush Mohandass, *NetSpeed Systems, USA.*
A Software-Defined SoC Interconnect Fabric for Enabling AI Applications
10:30 am Yuko Hara-Azumi, *Tokyo Institute of Technology, Japan.*
Highly-Scalable and Flexible Multicore Processors with Limited ISAs
10:48 am Akihiko Shinya, *NTT Nanophotonics Center, Japan.*
11:00 am Shinya Takamaeda, *Hokkaido University, Japan.*
QUEST: A Log-Quantized Deep Neural Network Engine with 3D Stacking SRAMs
11:12 am MarilynWolf, *Georgia Tech, USA.*
Smart Stacked Image Sensors
11:24 am Jiang Xu, *Hong Kong University of Science and Technology, Hong Kong.*
RSON: Silicon Photonic Network for Rack-Scale Computing System
11:36 am Panel discussion
12:15 pm Lunch

SESSION 3: IN-DEPTH/MINI-KEYNOTES

2:00 pm Francois Neumann, *Safran Electronics & Defense, France.*

TUESDAY, JULY 31
HIGH PERFORMANCE COMPUTING

2:30 pm Greg Nielson, *Nielson Scientific, USA.*
3D Silicon Nanofabrication of Multi-Functional Interposers for 3D Integration

3:00 pm Rolf Ernst, *Technische Universität Braunschweig, Germany.*
Model-based MPSOC Self-adaptation for Critical Systems

3:12 pm John Goodacre, *University of Manchester/Kaleao Ltd/ARM Ltd, UK.*
Designed for scale-out: Brain vs. Brawn

3:24 pm Break

SESSION 4: IN-DEPTH/MINI-KEYNOTES

4:00 pm Kees Vissers, *Xilinx, USA.*

4:30 pm Takashi Miyamori, *Toshiba Corporation, Japan.*
200m-Range-Imaging LiDAR with Smart Accumulation Technique for Autonomous Driving Systems

5:00 pm Wei Zhang, *Hong Kong University of Science and Technology, Hong Kong.*
Static and Dynamic Hybrid Cache Management for CPU-FPGA Platforms

5:12 pm Panel discussion

8:00 pm Dinner

WEDNESDAY, AUGUST 1
EMBEDDED SOFTWARE

SESSION 1: KEYNOTE

8:30 am Ike Nassi, *TidalScale, USA.*
Software-Defined Servers

9:30 am Break

SESSION 2: MINI-KEYNOTES

10:00 am Masaki Gondo, *eSOL Co., Ltd., Japan.*
Update on AUTOSAR Adaptive Platform and application of scalable distributed microkernels

10:12 am Victor Grimblatt, *Synopsys, Chile.*
Smart Agriculture – How to Improve the Throughput of the Soil using IoT?

10:36 am Pankaj Mehra, *Samsung Electronics, USA.*
Data Centric Computer Architecture, An Update

10:48 am Anca Molnos, *CEA-Leti, France.*

11:00 am Panel discussion

12:15 pm Lunch

SESSION 3: MINI-KEYNOTES

2:00 pm Gerd Ascheid, *RWTH Aachen University, Germany.*
Towards a Power Efficient Embedded DNN (Deep Neural Network) ASIP

2:12 pm Weihua Sheng, *Silexica, Germany.*
Embrace future supercomputers for autonomous vehicles

2:24 pm Koichiro Yamashita, *Fujitsu Laboratories LTD., Japan.*

2:36 pm Arnaud Grasset, *Thales Research & Tech., France.*
Reliable Embedded Systems for Critical Applications

2:48 pm Youn-Long Lin, *Professor at National Tsing Hua University, Taiwan.*
DRAM-Centric Accelerator Design for Large DNNs

3:00 pm Ittetsu Taniguchi, *Osaka University, Japan.*
An Efficient Parts Counting Method based on Intensity Distribution Analysis for Industrial Vision Systems

3:24 pm Break

8:00 pm Dinner

THURSDAY, AUGUST 2
HETEROGENEOUS MPSOC

SESSION 1: KEYNOTE

8:30 am Shuichi Yamane, *Socionext Inc., Japan.*
Hyper scale server

9:30 am Break

SESSION 2: MINI-KEYNOTES

10:00 am Nicolas Ventroux, *CEA-List, France*
Neural Computing in Embedded Systems

10:12 am Ran Ginosar, *Technion-Israel Institute of Technology, Israël.*
RC64—Energy Efficient Shared Memory Manycore

10:24 am Tsuyoshi Isshiki, *Tokyo Institute of Technology, Japan.*
C++ System-Level Synthesis/Verification of Wireless Sensor Networks on the C2RTL Framework

10:36 am Hiroki Matsutani, *Keio University, Japan.*
Accelerating Anomaly Detection Algorithms on FPGA-Based High-Speed NICs

THURSDAY, AUGUST 2
HETEROGENEOUS MPSOC

SESSION 3: KEYNOTE

10:48 am Kees van Berkel, *Ericsson, Eindhoven University of Technology, The Netherlands.*

11:00 am Panel discussion

12:15 pm Lunch

2:00 pm Shahar Kvatinsky, *Technion - Israel Institute of Technology, Israel.*
Real Processing-in-Memory with Memristive Memory Processing Unit

2:30 pm Pei-Lin Pai, *Winbond, Taiwan.*
Emerging Memory for Artificial Intelligence and IoT

3:00 pm Yoshinori Takeuchi, *Kindai University, Japan.*

3:12 pm Hiroyuki Tomiyama, *Ritsumeikan University, Japan.*
Malleable Task Scheduling for Multi-/Many-core Platforms

3:24 pm Break

SESSION 4: IN-DEPTH/MINI-KEYNOTES

4:00 pm Yuan Xie, *UCSB, USA.*

4:30 pm Yuichi Nakamura, *NEC Corp., Japan.*
SX-Aurora Tsubasa, HPC meets machine learning

5:00 pm Frédéric Rousseau, *TIMA Lab - Grenoble University, France.*
Communication Consistency for Hardware Context Switch on Heteroegeneous FPGAs

5:12 pm Panel discussion

8:00 pm Dinner

FRIDAY, AUGUST 3
DEEP LEARNING AND NEURAL NETWORK

SESSION 1: KEYNOTE

8:30 am Rob Aitken, *ARM, UK.*

9:30 am Break

SESSION 2: IN-DEPTH/MINI-KEYNOTES

10:00 am Peter van der Made, *BrainChip Inc., USA.*
Introducing the Akida Spiking Neural Network Reconfigurable NeuroSoC

10:30 am Masatoshi Ishii, *IBM Research - Tokyo, Japan.*
NVM neuromorphic core with on-chip learning capability

11:00 am Song Yao, *DeePhi Tech, China.*
The Evolution of Deep Learning Accelerators Upon Evolution of Deep Learning Algorithms

11:12 am Danilo Pau, *STMicroelectronics, Italy.*
The (Artificial Intelligent) Cyber-Physical Revolution: From Theory to Practice

11:36 am Jishen Zhao, *UCSD, USA.*

11:48 am Panel discussion

1:00 pm Lunch