

Sun 7 July	Welcome Reception				
Mon 8 July	9:00- Session 1	Keynote (60 min) Break Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Hideki Sugimoto Masaaki Kondo Eric Monchalain Andreas Herkersdorf Gerd Ascheid Yoshifumi Sakamoto		Architecture Challenge for Future Automotive or Embedded Compute SoC Are next Generation Architectures suitable? Near Memory Accelerators for Efficient Inter-Tile Communication in Distributed-Shared-Memory Architectures Scalability Aspects of a Many-Core ASIP Platform targeted at Convolutional Neural Networks
	12:30- Lunch				
	14:00- Session 2	In-depth (30 min) In-depth (30 min) In-depth (30 min) Break In-depth (30 min) In-depth (30 min) In-depth (30 min) Panel	Arnaud Grasset Timothée Levi K. Charles Janac Atsushi Hasegawa Shuichi Oikawa Kiyoung Choi		A Look at Computer Architectures for Mission-Critical Embedded Systems Biomimetic Spiking Neural Network and Neurohybrid systems for AI and biomedical GENESIS: AI Vision Processing Platform for Edge Computing Algorithms and Architectures for Efficient Neural Processing
Tue 9 July	9:00- Session 3	Keynote (60 min) Break Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Naim Ben-Hamida Marilyn Wolf Shuichi Yamane Masaki Gondo Wei Zhang Frederic Rousseau		Scalable ARM server for shared nothing DB SHIM 2.0 - an update to the new way to describe hardware for software tools Hi-ClockFlow: Multi-Clock Dataflow Automation and Throughput Optimization in High-Level Synthesis Locality: a Scalable Synchronization Lock for MPSoCs
	12:30- Lunch				
	14:00- Session 4	In-depth (30 min) In-depth (30 min) In-depth (30 min) Break In-depth (30 min) In-depth (30 min) In-depth (30 min) Panel	Sunghyun Lee Takashi Miyamori Ran Ginosar Ashkan Seyedi Benoit de Dinechin Gerhard P. Fettweis		Making difference in SoC with high performance memory subsystem IP DNN-Accelerated Multi-core SoC for Automotive Applications RC64: Space-ready high performance, low power manycore Recent advances on WDM Silicon Photonics Devices for HPC Applications A first step to building a 6G HW/SW platform
Wed 10 July	9:00- Session 5	Keynote (60 min) Break Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Hiroyuki Kitayama Victor Grimblatt Jiang Xu Yoshinori Takeuchi Ittetsu Taniguchi Norbert Wehn		Trend of advanced technologies such as AI, Blockchain, New Computing and applicability in the industry An SoC for IoT Applied to Smart Agriculture BOSIM: A Comprehensive Electro-Optical Model for Silicon Photonic Switches Challenges for online optimization of drone path planning (Tentative) Channel Coding for Tb/s Communications
	12:30- Lunch				
	14:00- Session 6	In-depth (30 min) In-depth (30 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Koji Inoue Tamon Sadasue Kees van Berkel Shinya Takamaeda Jishen Zhao		Scalable Logic Architecture for Accelerating Gradient Boosted Tree Learning Exascale Computing for Radio Astronomy, Using Dataflow
	16:30- Speaker's Meeting				
Thu 11 July	9:00- Session 7	Keynote (60 min) Break Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Masanao Yamaoka Pierre Paulin Kees Vissers Masahiro Murakami Youn-Long Lin Lorena Anghel Song Yao		Scaling Deep Neural Network Accelerator Performance Versal: The new Xilinx Adaptive Compute Acceleration Platforms (ACAP) in 7nm SOC Design of a Neural Network for Real-Time Semantic Segmentation of 2Kx1K@60fps Video On Dependability of Spiking Neural Networks
	12:30- Lunch				
	14:00- Session 8	In-depth (30 min) In-depth (30 min) Break Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Akihiko Shinya Yankin Tanurhan Gabriela Nicolescu Fumio Arakawa Tsuyoshi Isshiki Tohru Ishihara Hiroyuki Tomiyama Anca Molnos		Evolving Vision and Deep Neural Network Processors for Emerging Applications in the Edge CNN Training HW Architecture Design Using C2RTL SoC Synthesis/Verification Framework Near-Threshold Cache Architecture for Ultra-Low Energy Computing Static Scheduling of Parallel Tasks Towards embedding attack detection on IoT end-nodes
Fri 12 July	9:00- Session 9	In-depth (30 min) In-depth (30 min) Break Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Mini-keynote (12 min) Panel	Yuichi Nakamura Yukoh Matsumoto Masatoshi Ishii Sungjoo Yoo Yuko Hara-Azumi Hiroki Matsutani Frédéric Pétrou John Goodacre		Real Quantum Annealing, Architecture and Applications Challenges on Designing Parallel Processing for realizing Real-Time Applications On-chip trainable spike-based neuromorphic core using phase change memory as synapse Reinforcement learning-based optimization for solid state disks Bio-Inspired Highly-Parallelized SAT solver on FPGA An On-Device Learning Approach for Unsupervised Anomaly Detection A Scalable Sharing Set Management Approach for Large Scale MPSoC Reusable Arm computational chiplet with 128bit shared global address space access
	12:30- Lunch				