MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

CHIP DESIGN GERMANY

Open Source in Hardware Design – Opportunities, Challenges and Example

Norbert Wehn

RPTU Rheinland-Pfälzische Technische Universität Kaiserslautern Landau

Open-Source in Hardware !?

Basic Principles if Open-Source

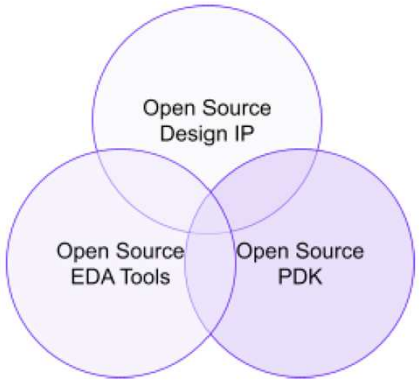
- Openness, Transparency, collaborative design
- Reduced cost, faster adaption, fosters innovation

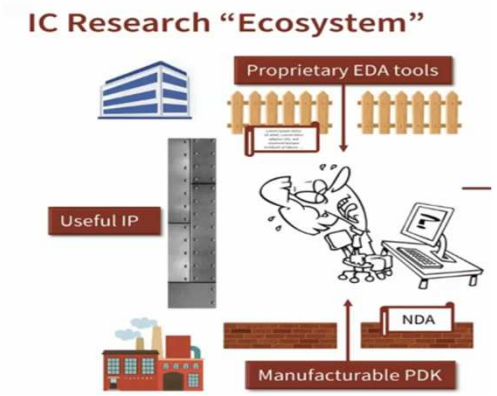
Open-Source Software

- Started about 30 years ago, successful and well established
- Large community, collaborative development, e.g. Linux
- Enterprises: SW-development cost 3,5 x larger than without OSS (Harvard Business School 2024)
- Concepts/experience transferable to chip design?

Open-Source Hardware – in the beginning

- RISC-V
- Technological Sovereignty
- Access: NDA, export regulations





Open-Source Activities

Many Activitities

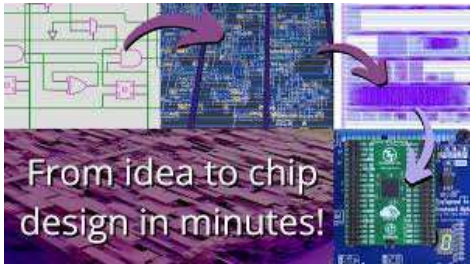
- BMBF projects DE:Sign, DE:Sign Challenge, acatech study, IHP….
- PULP platforms, OpenROAD initiative, Tiny tapeout/efabless
- EU Initiative: free and Open-Source Silicon Foundation (FOSSI): EU Roadmap

Different Views/Opinions

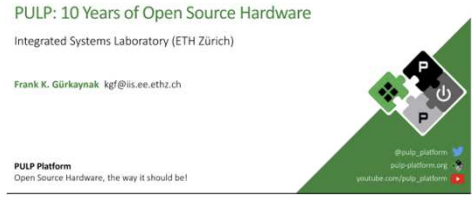
- EDA, beginners in design, skilled designers
- Research/Universities, StartUps/SMEs, large industry
- Technologynode: 130nm…7nm
- Type of circuit design: digital, Mixed-Signal, RF, sensor, optic, powerss., …

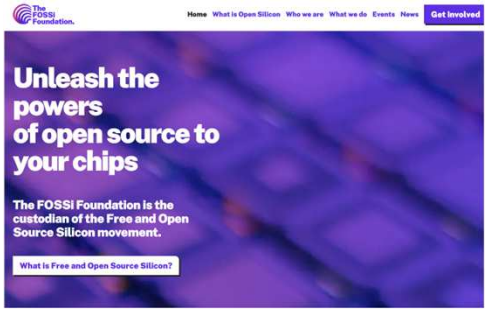
Challenges

- Maturity and PPA Quality
- Support, Business model
- Dependency on USA



ETH zürich





RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Open-Source Overview

Design Activity	Synopsys	Cadence	Siemens EDA	Open-Source
High-Level Synthesis	Symphony C	Stratus HLS	Catapult	XLS (Google)
RTL-Analysis	RTL-Architect, SpyGlass, Verdi	Joules, Litmus	Questa-Visualizer	Cocotb
RTL-Simulator	VCS, VC family, Zebu	Xcelium, Verisium, Palladium	ModelSim, Veloce	Verilator/GHDL/Icarus
Logic Synthesis	Design Compiler, FusionCompiler	Genus	Oasys	Yosys
Formal Equivalent	Formality, VCFormal	Japser, Conformal	OneSpin	Yosys
Static Timing Analysis	PrimeTime	Tempus	-	OpenSTA
Place and Route	ICC/ICC2, FusionCompiler	Encounter, Innovus	Aprisa	OpenROAD
Power Analysis, EM/IR	PrimePower, Redhawk	Voltus	PowerPro, mPower	OpenROAD (OpenSTA)
Physical Verification (DRC/LVS)	IC Validator	PVS, Pegasus	Calibre	MAGIC/Klayout
Parasitic Extraction	StarRC	Quantus	Calibre xRC/xACT	MAGIC/OpenRCX
ECO-Tools	Tweaker, PrimeTimeECO	Talus ECO	-	N/A
Analog, AMS, RF	CustomCompiler, HSPICE	Virtuoso, Spectre	Questa, Eldo, FastSPICE	Xsheme, ngspice, Xyce, OpenVAF
Library Characterization & Prediction	SiliconSmart, LibraryCompiler, NanoTime	Liberate	Solido, Kronos	N/A
Package, Co-Design	3DIC Compiler	Silicon-Package-Board Co-Design	Xpedition	N/A

Yosys, Klayout, und ngspice are from Europe!

Source: updated table from David Thanh

Open Source – OpenRoad

Yosys (YosysHQ)

- Logic Synthesis

Klayout (Matthias Köfferlein)

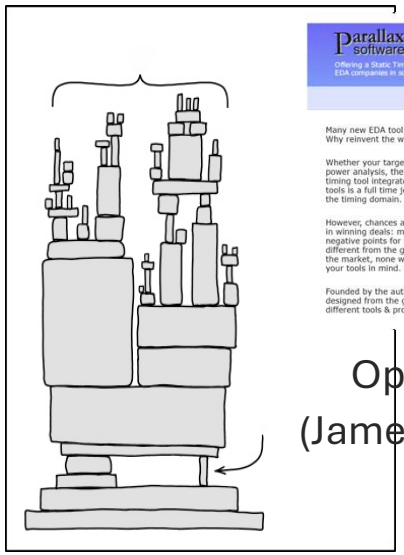
- GDS merge
- DRC/LVS

itonRoute (UC San Diego)

Routing

penRCX (UC San Diego)

Parasitics Extraction



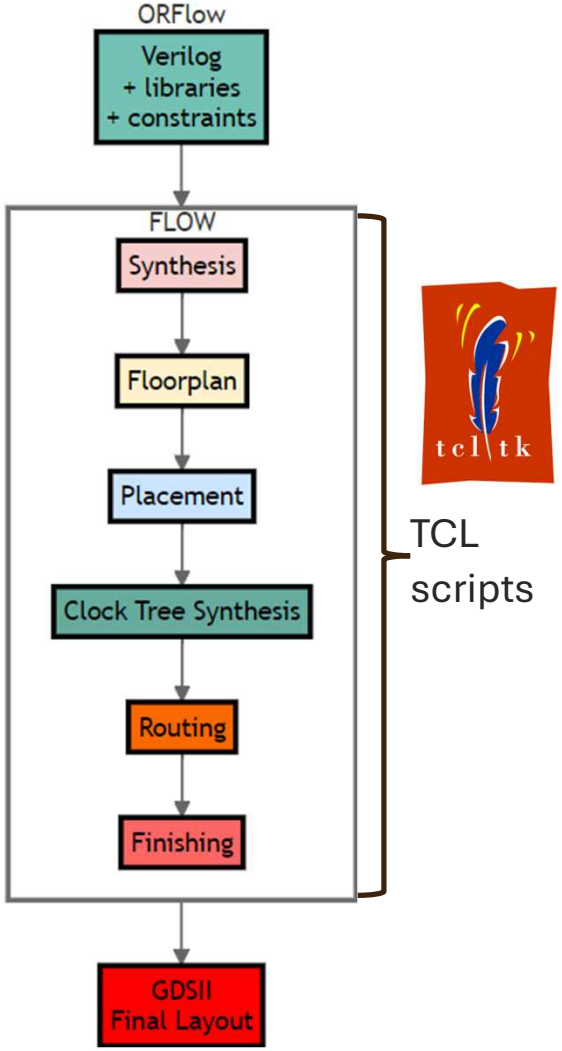
OpenSTA

(James Cherry)

penSTA (James Cherry)

Static Timing Analysis

- Power



Open-Source Digital Benchmark – Example

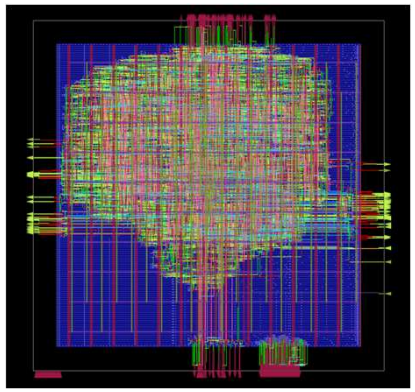
CHIP DESIGN GERMANY

Open-Source PicoRV32 RISC-V Core

- STD-Lib from ARM, 9-Track SLVT, **12nm** GF12LPP für kommerziellen Flow und OpenROAD Flow

	Commercial	OpenRoad
Performance		
Clock Constrain [ps]	2000	2000
WC Delay [ps]	**1935**	**631 (-67%)**
Power		
Switching [μW]	2122	3830 (80.5%)
Internal [μW]	3459	4760 (37.6%)
Leakage [μW]	123	-66.8 (-154%)
Total [μW]	**5704**	**8523 (49.4%)**
Area		
Cell [μm^2]	2205	5688 (61.2%)
Total [μm^2]	**3593**	**11664 (69.2%)**
Run-Time		
CPU Cores Used	8 (Licences!)	96
Time [min]	**130**	**5 (-96%)**

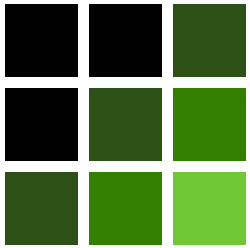
	Commercial	OpenRoad
Performance		
Clock Constrain [ps]	650	650
WC Delay [ps]	**650**	**646 (-0.62%)**
Power		
Switching [μW]	2769	14200 (330%)
Internal [μW]	3302	9780 (196%)
Leakage [μW]	141	-66.8 (-147%)
Total [μW]	**6212**	**23913 (285%)**
Area		
Cell [μm^2]	2328	5471 (57.4%)
Total [μm^2]	**4113**	**11664 (64.7%)**
Run-Time		
CPU Cores Used	8 (Licences!)	96
Time [min]	**130**	**5 (-96%)**



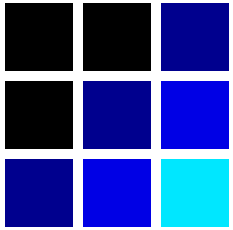
- Results independent of timing constraints: no trade-off area, power and timing for relaxed timing constraints
- Leakage power estimations are wrong
- But fast run times!

RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Open-Source Tools



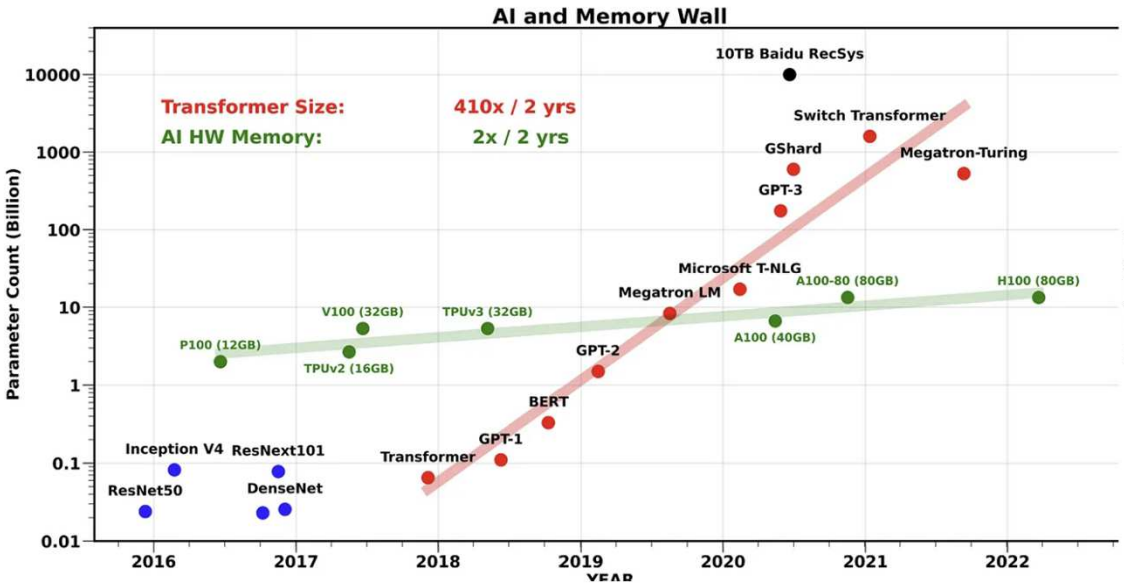
DRAMSys



DRAMPower

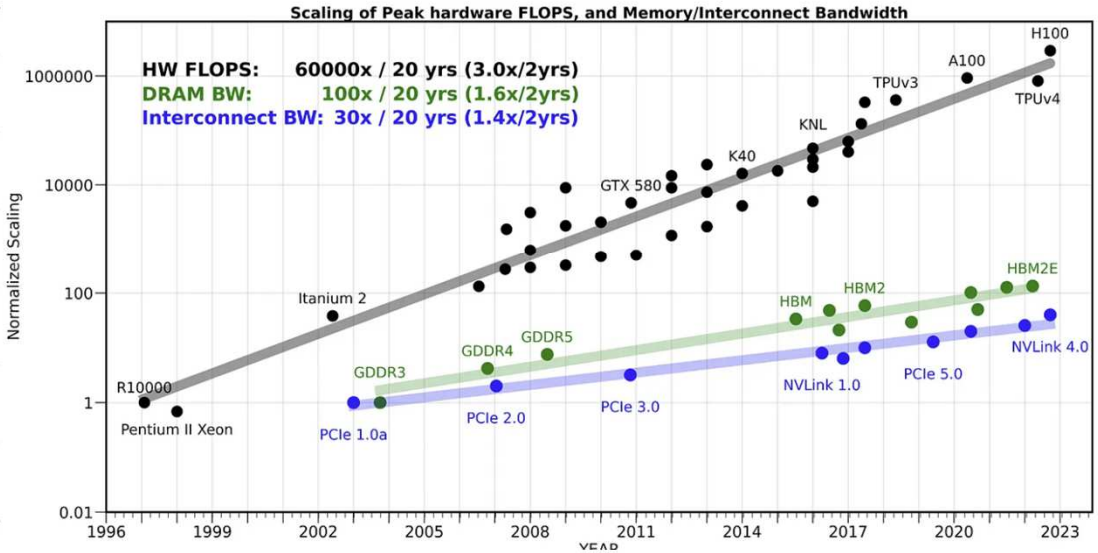
Importance of DRAM Memories – AI Challenges

Model Size versus AI accelerator Memory Capacity

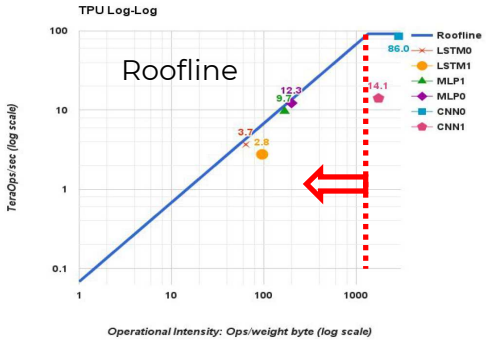


Source: AI and Memory Wall/Medium Post

Memory Bandwidth



Source: AI and Memory Wall/Medium Post

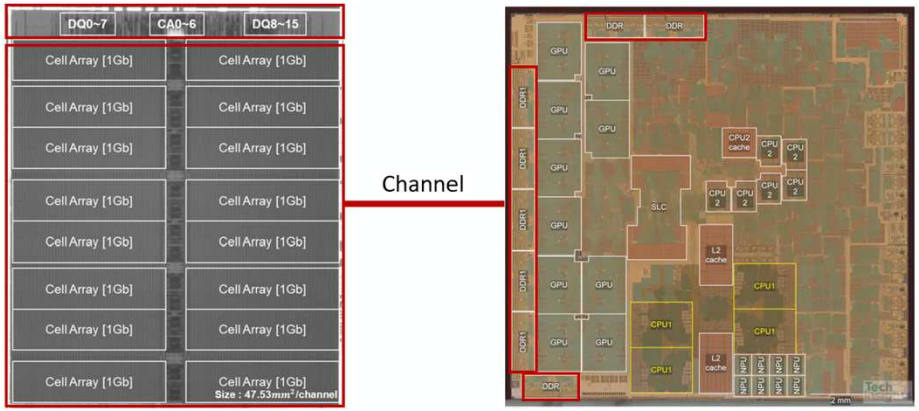


Google TPU v1: 8GB DDR3, 34GB/s
Google TPU v2: 16GB HBM, 600GB/s
Google TPU v4: 32GB HBM, 1200GB/s

NVIDIA A100: 80GB HBM2E, 2000GB/s
NVIDIA H200: 140GB HBM3E, 4800GB/s

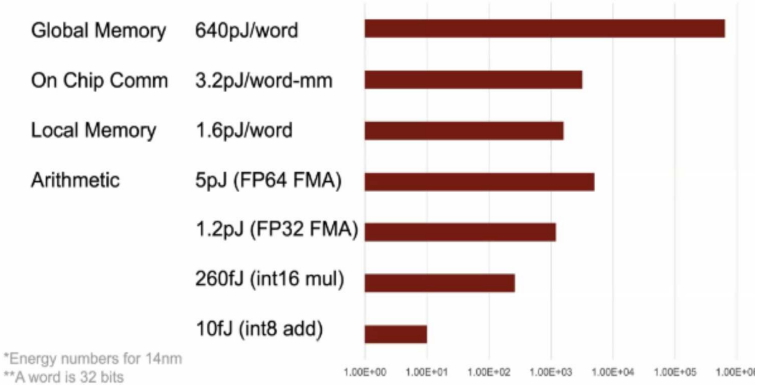
RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

AI Memory Challenges – Energy

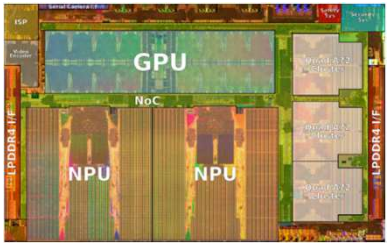


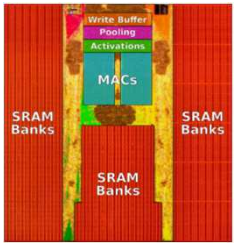
Source: *A 16Gb 9.5Gb/s/pin LPDDR5X SDRAM with Low-Power Schemes Exploiting Dynamic Voltage-Frequency Scaling and Offset-Calibrated Readout Sense Amplifiers in a Fourth Generation 10nm DRAM Process*, https://doi.org/10.1109/ISSCC42614.2022.9731537

Source: https://www.heise.de/news/Apple-M4-TSMCs-FinFlex-hilft-den-Performance-Rechenkernen-9766547.html

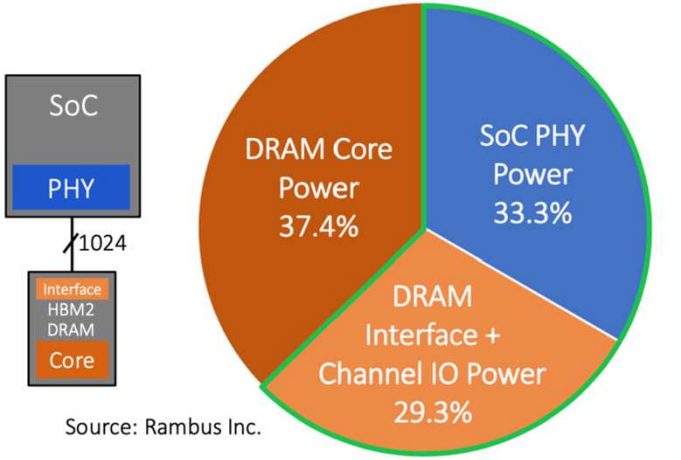


Source: TSMC



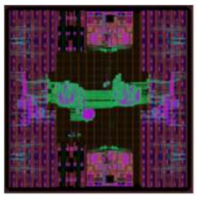


Source: Tesla /FSD 3

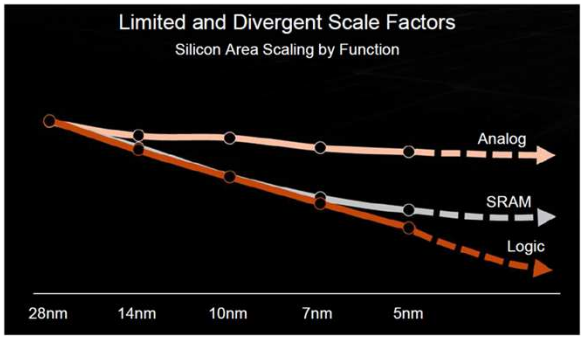


Source: Rambus Inc.

Data Movement: 62.6% of Power

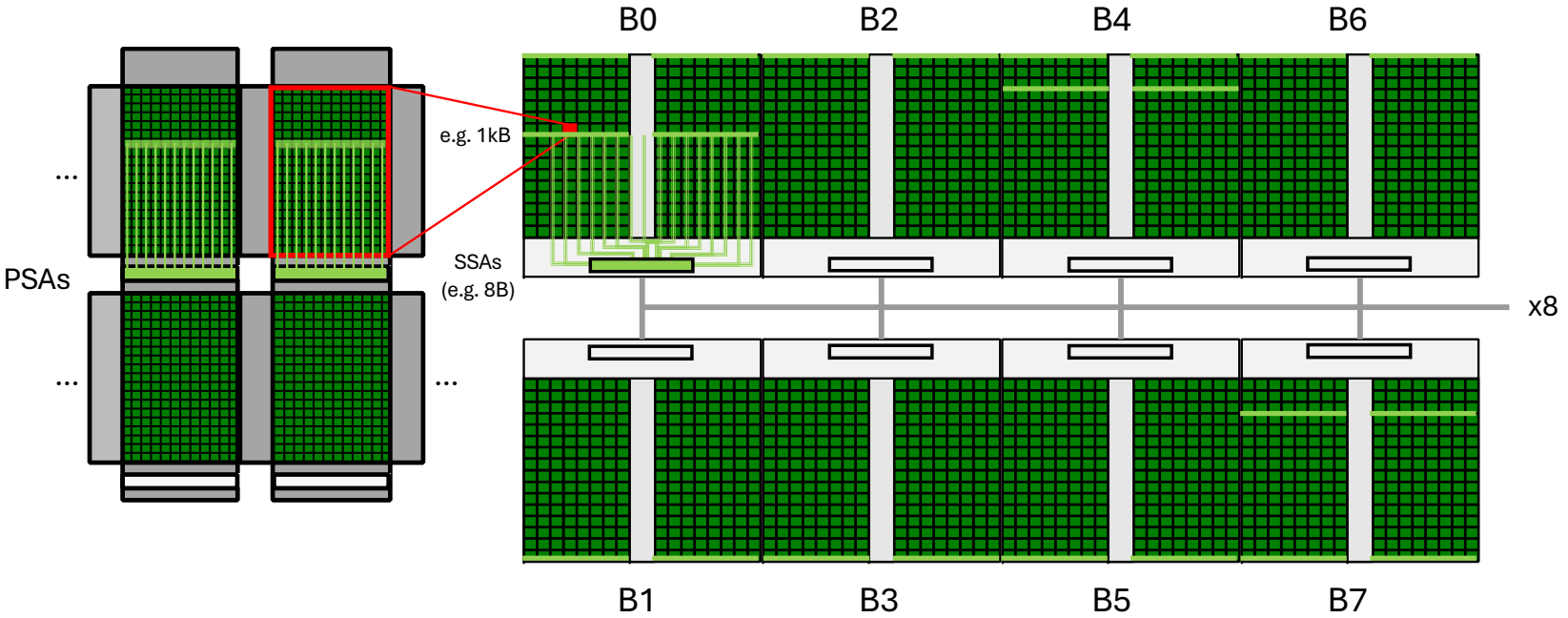


RPTU EMS LPDDR4 Phy
12nm FinFET



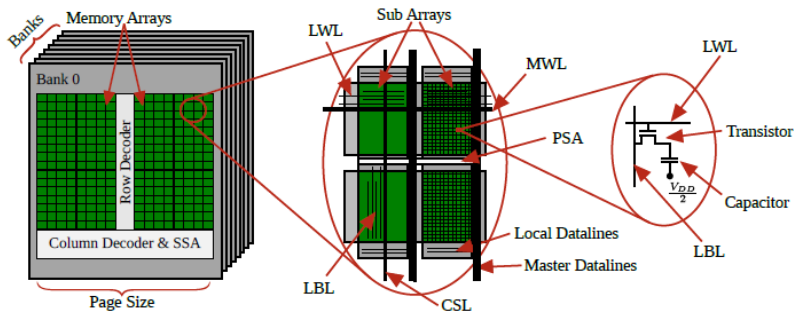
RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

DRAM Basics



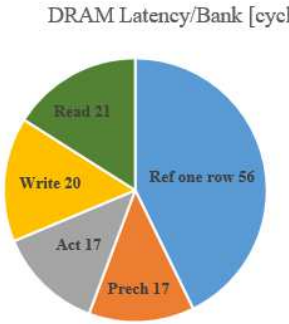
DRAM Commands

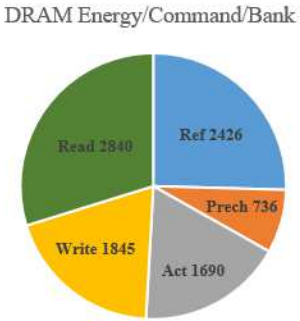
- ACT: Activates a specific row in a specific bank (sensing into PSA)
- RD: Read from activated row (prefetch from PSA to SSA and burst out)
- PRE: Precharges set LWL=0 set LBL=VDD/2
- REFA: DRAM cells are leaky and have to be refreshed



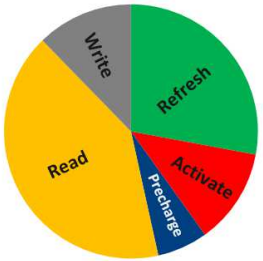
DRAM Behavior

- Latency and energy breakdown e.g. DDR4, 4Gbit, 1200MHz, 64 bits burst read/write

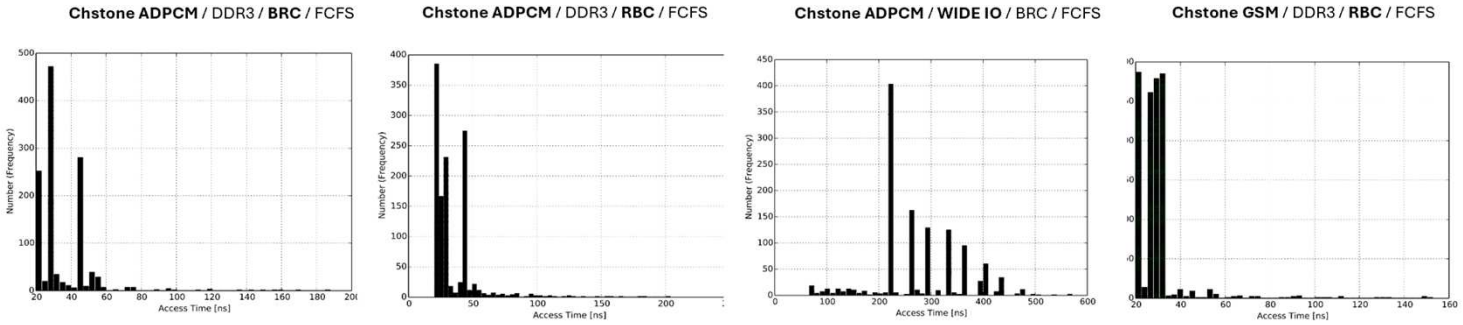




Energy in Twitter memchached Application 2GB DDR3



- DRAM latency/energy) largely varies: access pattern, address mapping, scheduling….



Up to 10x variance in access times → row change in the same bank worst case: 42 clock cycles

Modelling of accurate DRAM timing and DRAM power are essential to assess the overall SoC performance and power/energy consumption

Open Source – DRAMSys/DRAMPower

DRAMSys

DRAM timing modelling tools

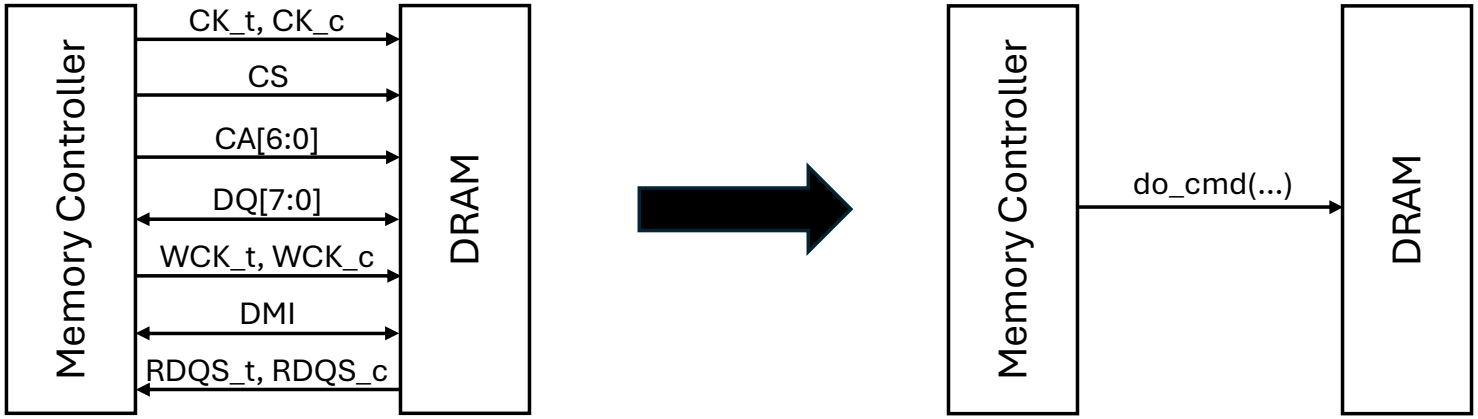
- Big EDA vendors: no commercial interest/small market
- CPU/SoC vendors: internal modelling tools, not public
- Memory vendors: data/excel sheets, don’t disclose internal details
- Academic tools
  - DRAMsim (University of Maryland), 2005
  - Gem5, 2011
  - DRAMSys + DRAMPower (RPTU, Fraunhofer IESE, JMU Würzburg), 2013
  - Ramulator (CMU/ETH) + VAMPIRE (CMU/ETH), 2015

RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

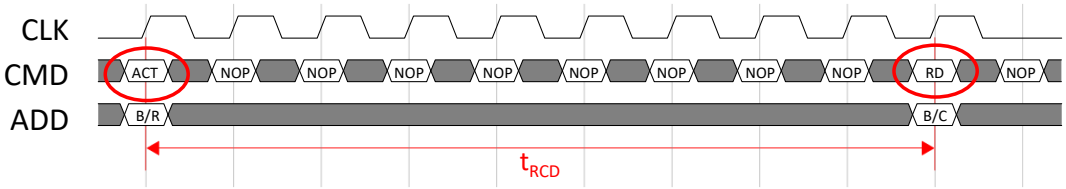
Simulation Speed vs. Simulation Accuracy

How can you accelerate simulation without losing accuracy?

- Replace individual signals with function calls (concept of TLM)

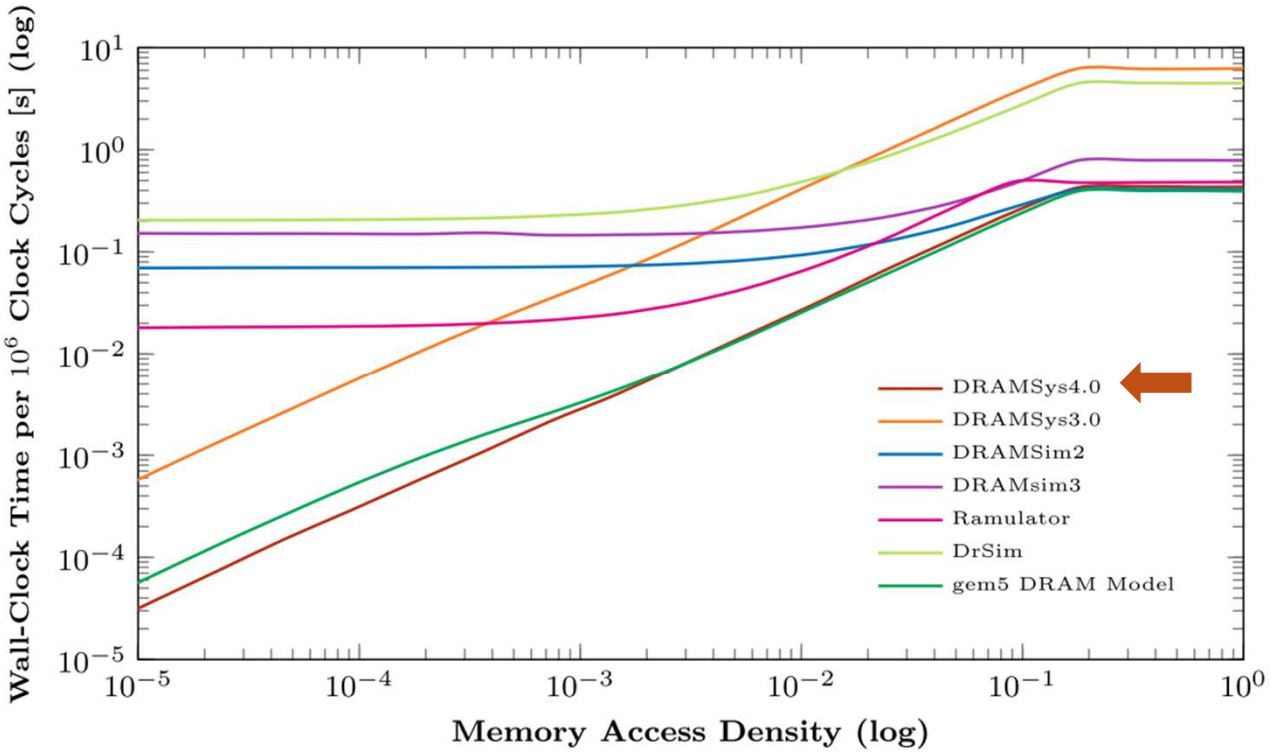


- Simulate only the clock cycles (events) where “something” happens



Simulation Speed vs. Simulation Accuracy

- gem5's DRAM model: simplified model, does not fulfill JEDEC cycle accuracy
- DRAMsim, Ramulator, DRAMSys: clock cycle accuracy according to JEDEC protocol
- DRAMsim, Ramulator: based on clock cycle events



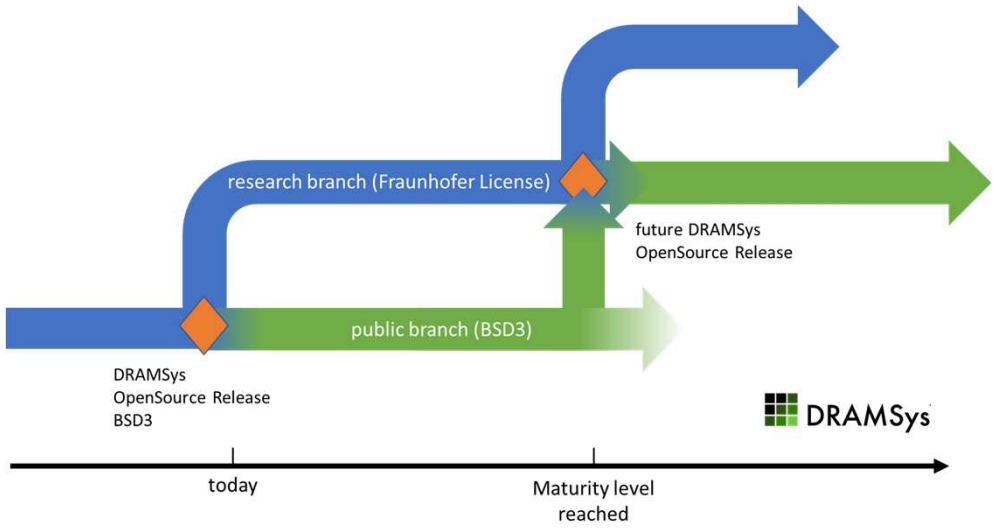
History of DRAMSys

DRAMSys

- Large DRAM knowledge within the group (DRAM industry background)
- First publication in 2013: *“TLM modelling of 3D stacked wide I/O DRAM subsystems: a virtual platform for memory controller design space exploration”, M Jung, C Weis, N Wehn, K Chandraseka*
- Extended to DDR3, DDR4, LPDDR3 and HMC
- PhD students, master students, HiWi’s -> Too many cooks spoil the broth…
- Completely rewritten
  - Software architecture: enables easy integration of new standards and features
  - Support latest standards e.g. LPDDR4, GDDR6, HBM2
- Open-sourced in 2020 (BSD3): https://github.com/tukl-msd/DRAMSys

DRAMSys Freemium Business Model

- Established DRAM standards (DDR3/4, LPDDR4/4x, GDDR5/5x/6, HBM2) are open-sourced on GitHub
- Emerging DRAM standards (DDR5, LPDDR5, HBM3…) can be licensed via Fraunhofer IESE
  - Free academic licenses for research
  - Paid industrial licenses including support, consulting and custom modifications



DRAMSys Facts and Figures

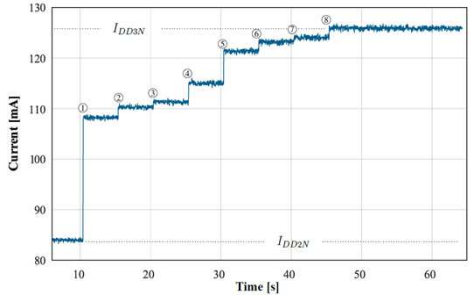
- DRAMSys
  - 4 key papers ~ 170 citations
  - contributed to more than 20 further publications of the chair(s)
- Funding from DFG/BMBF/chair…
- More than 20 contributors and 2700 commits in master branch
- 240 stars and 60 forks on GitHub
- Large user community

…

History of DRAMPower

DRAMPower

- Power model originally developed by TU Delft/TU Eindhoven in 2011
  - Goal: improve the accuracy of Micron's DRAM power calculators (Excel spreadsheets)
- RPTU-EMS
  - Validated and improved the model with circuit-level simulations
  - Took over management and further development
- First publication 2012: "*DRAMPower Open-source DRAM power & energy estimation tool*" *K. Chandrasekar, C. Weis, Y. Li, B. Akesson, N. Wehn, K. Goossens*
- First Open-Sourced in 2013
- Introduction of new features, e.g., a bank-sensitive power model

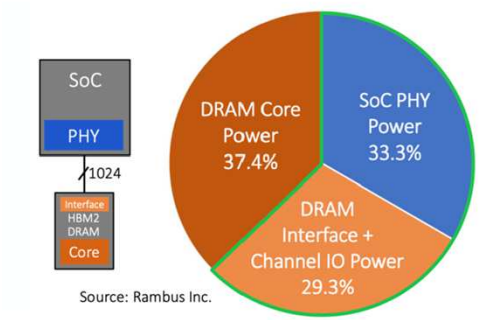


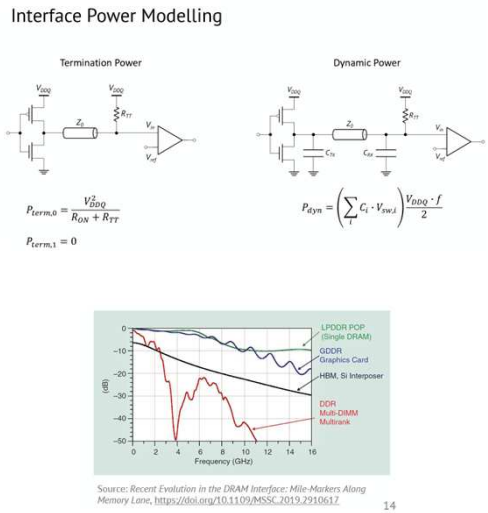
RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

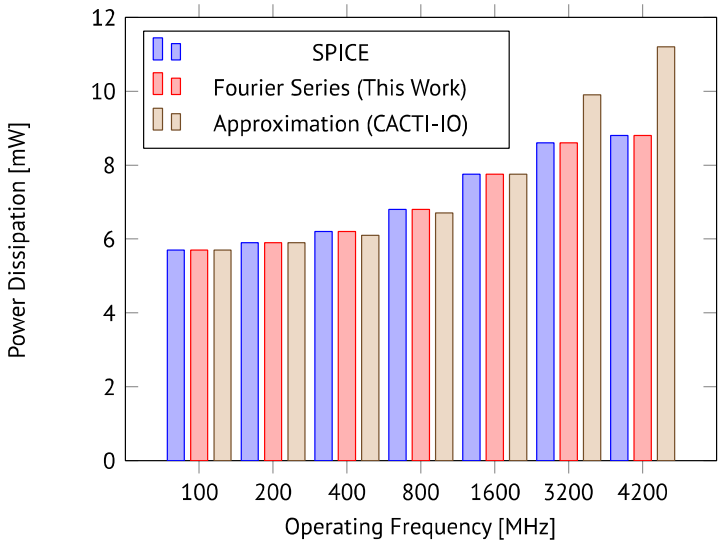
DRAMPower 5 – 2024

DRAMPower

- Major updates in context of BMBF project DI-DERAMSys
- Improved software architecture
- Support for current DRAM standards (DDR5, LPDDR5, …)
- Accurate interface power modelling







RPTU MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

DRAMPower Facts and Figures

- State-of-the-art tool for DRAM power modelling
- Part of gem5
- 12 contributors and 400 commits on master branch
- DRAMpower papers ~ 300 citations
- 150 stars and 50 forks on GitHub
- DRAM Power 5.0 released 2024: https://github.com/tukl-msd/DRAMPower

Conclusion

Open-Source in Hardware Design: Hype or important new direction?

- Can ease technology access and contribute to technological sovereignty (for older technology nodes)
- Can complement/fill gaps that are not (yet) supported by commercial vendors, e.g. niche or new technologies
- Can broaden chip design community, education
- Many open challenges
  - PPA quality, maturity
  - Support, business model
  - ……

Thank You


CHIP
HAPPENS
www.chipdesign-germany.de
CHIP
DESIGN
GERMANY