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ENGINEERED SUBSTRATES FOR SECURE, RESILIENT EDGE AI, IOT & AUTOMOTIVE SOCS

MPSoC, Megeve | 16.06.25

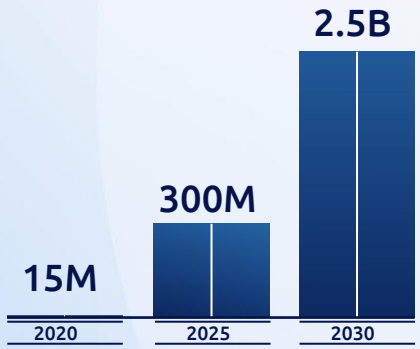
EMERGING SOC DEMANDS ACROSS EDGE AI, IOT & AUTOMOTIVE

COMPUTE MOVES CLOSER TO THE EDGE: SECURITY, RELIABILITY, POWER EFFICIENCY

Edge AI

IoT

EDGE AI CHIPSET MARKET (UNITS)



Source: ABI research 2021

Trust
Secure Processing

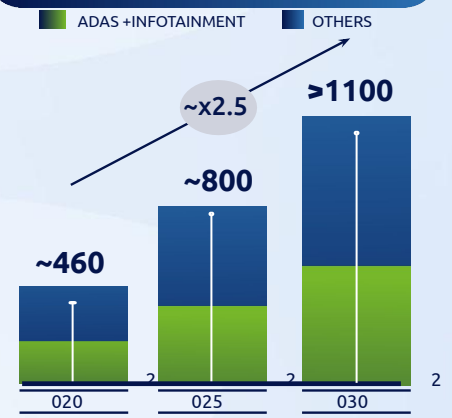
Latency/ Local AI

AI

Resilience
Harsh Environment Operation

Efficiency
Local Power / High Integration

SEMICONDUCTOR CONTENT PER CAR ($)



Source: UBS, Soitec estimates

- LOW POWER CONSUMPTION - ALWAYS ON
- PERFORMANCE ON DEMAND
- TAMPER PROOF - SECURE PROCESSING

- HIGH ROBUSTNESS & FUSA
- HIGH INTEGRATION
- HIGH EFFICIENCY & LIFETIME

ENGINEERED SUBSTRATES: FOUNDATION FOR SECURE, RESILIENT SOCS

Security, Efficiency, And Resilience—Engineered From The Substrate Up

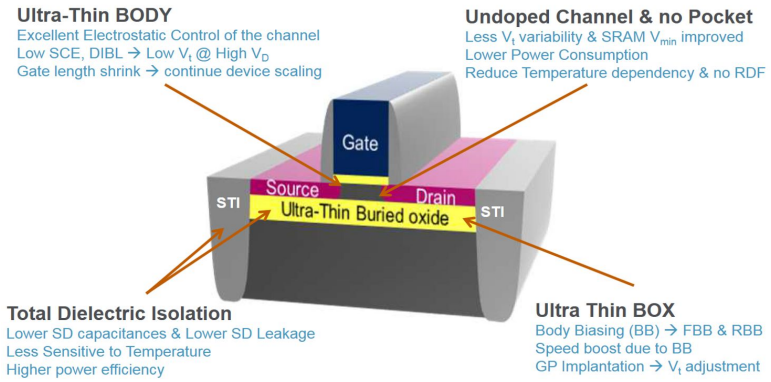
The physical layer plays an important role in

- Soft error susceptibility
- Leakage and variability
- Thermal instability
- Crosstalk/ interference

Start at the bottom: Trust begins in silicon

ADVANTAGE FD-SOI

Thin, undoped fully depleted channel with simple, planar structure giving good electrostatic control and low parasitic



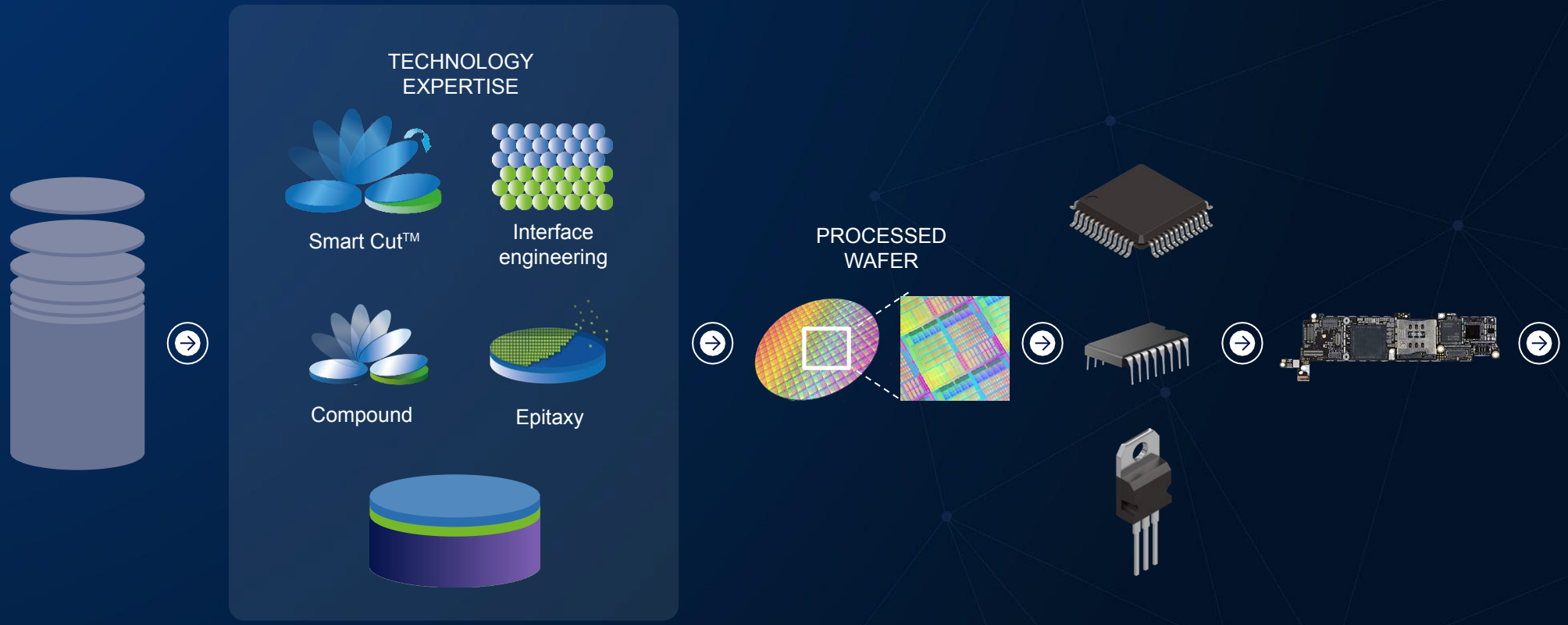
- Improved SER
- Improved mismatch
- Latch-up free
- Body bias: performance on demand
- Low leakage/Low power
- Low noise

Soitec in numbers

IN OUR SOIL GROWS AN AMAZING FUTURE

1992	530+	~4,300	11%	>2300	891M€
Soitec is founded	Patents filed worldwide in FY25	Active patents	of revenue dedicated to gross R&D	Employees (35% women) industry average 20-25%)	Revenue (Fiscal year 2025)

ENGINEERED SUBSTRATES
ARE A CRITICAL COMPONENT OF THE SEMICONDUCTOR INDUSTRY

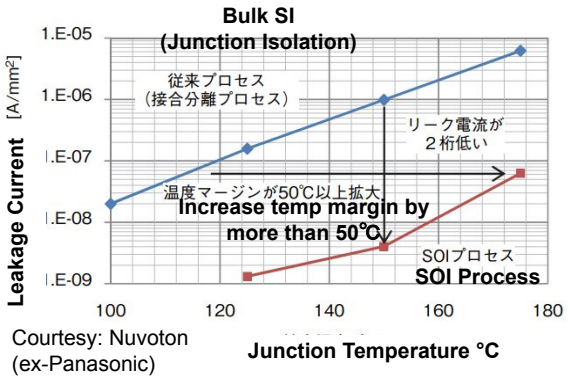


RESILIENCE UNDER STRESS: SUBSTRATE-ENABLED RELIABILITY

ENABLING RESILIENT SOCS FOR AUTOMOTIVE AND INDUSTRIAL

High temperature operation

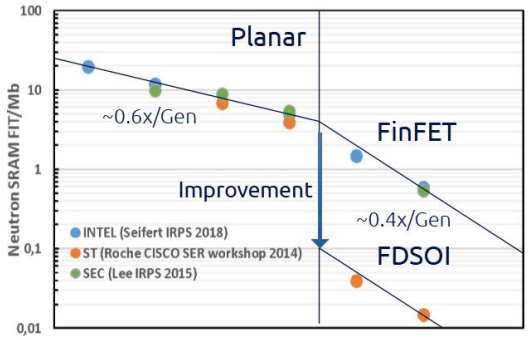
Meeting AEC-Q100C Grade 0 (150-175℃)
Lower leakage currents



Courtesy: Nuvoton
(ex-Panasonic)

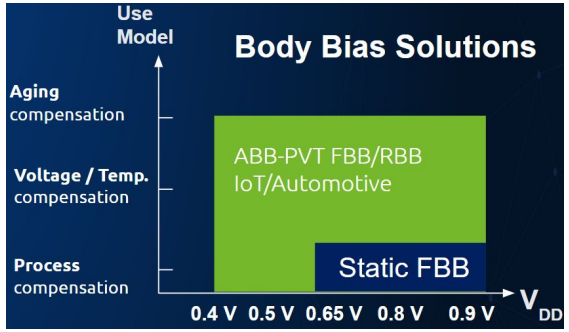
Radiation exposure

SEU, SER in automotive, avionics, industrial
BOx reduces charge diffusion
No latch up



Aging and variability

Body bias to dynamically compensate aging and PVT variations



Power/voltage noise sensitivity

Better isolation, reduced substrate coupling

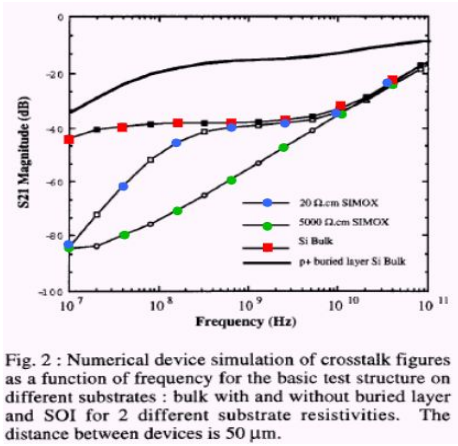


Fig. 2 : Numerical device simulation of crosstalk figures as a function of frequency for the basic test structure on different substrates : bulk with and without buried layer and SOI for 2 different substrate resistivities. The distance between devices is 50 µm.

SECURING SOCS FROM THE SUBSTRATE UP

Security isn't just an IP problem. It starts with the silicon foundation

FD-SOI: INHERENTLY SECURE

ERROR FREE MEM/LOGIC

10x lower SER [1]

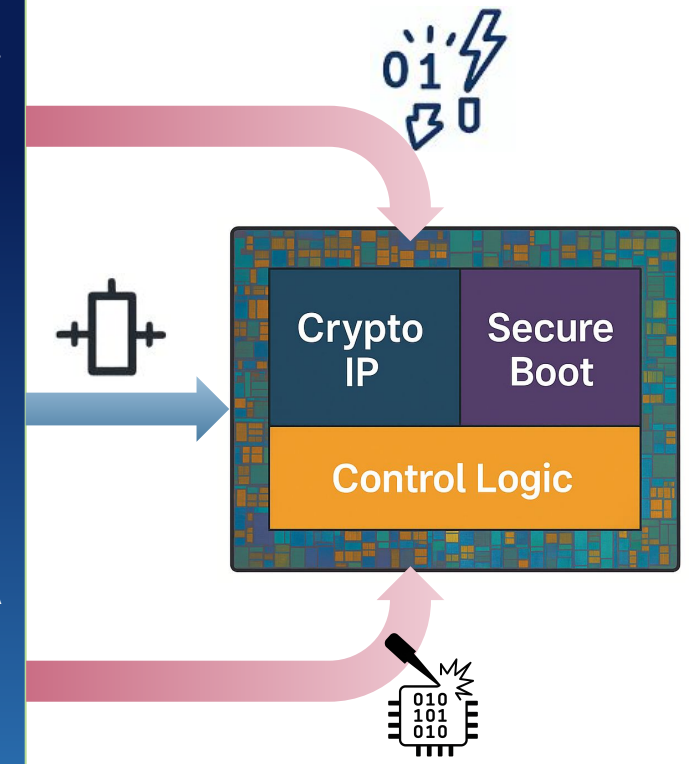
SIDE CHANNEL ATTACK IMMUNITY

5-10x lower leakage [2]

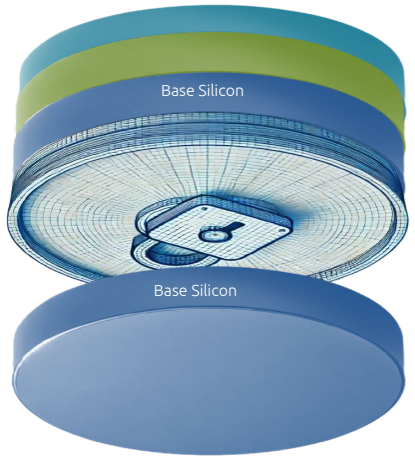
NO BACKDOOR VIA BACKSIDE

3-7x higher LFI* resistance [3]

*Laser fault injection



A GLIMPSE INTO THE FUTURE: CYBER-SUBSTRATE



A secure layer within the base Silicon

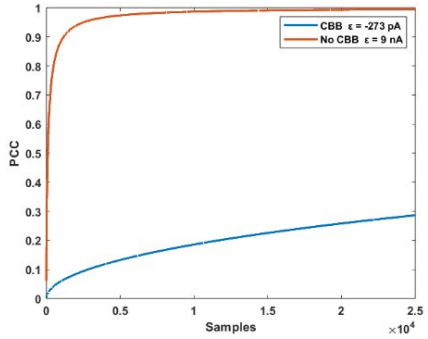
[1] Nguyen, Bich-Yen, et al. "A path to energy efficiency and reliability for ICs: Fully depleted silicon-on-insulator (FD-SOI) devices offer many advantages." IEEE Solid-State Circuits Magazine 10.4 (2018): 24-33.
[2] Planes, Nicolas, et al. "28nm FDSOI technology platform for high-speed low-voltage digital applications." 2012 Symposium on VLSI technology (VLSIT). IEEE, 2012.
[3] Dutertre, Jean-Max, et al. "Sensitivity to laser fault injection: Cmos fd-soi vs. cmos bulk." IEEE Transactions on Device and Materials Reliability 19.1 (2018): 6-15.

ENABLING SECURE IP IN FD-SOI WITH BACK BIAS (BB)

FROM CRYPTO RESILIENCE TO TRNGs

Back bias as a means to mask the leakage in secure IP[1]

Current Balancing Body Bias – using back bias to automatically balance the leakage currents.



COSOI: COSO TRNG using FDSOI[2]

BB as a very simple and efficient technique for the ring oscillator frequency calibration needed for the coherent sampling method.

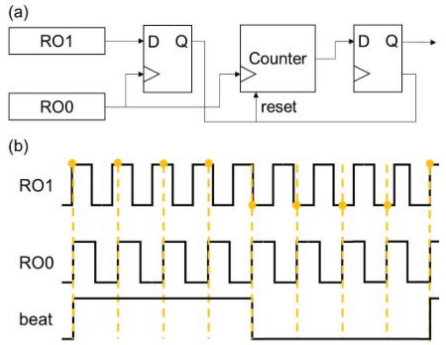
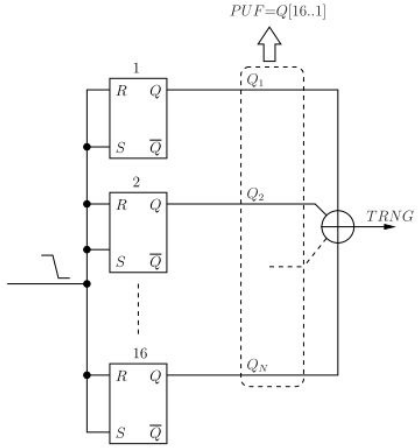


Fig. 2. Architecture of the COSO-TRNG (a) and schematic representations of the signals (b)

PUF-TRNG circuit based on as set of SR latches[3]

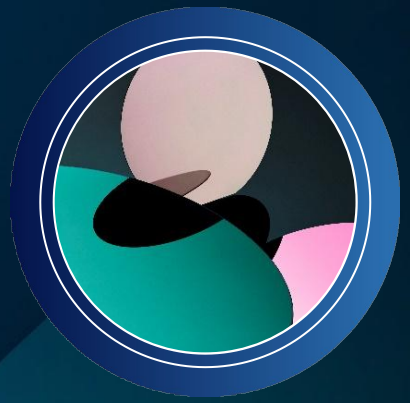
An optimal state is obtained for both TRNG and PUF by controlling the latches by the BB of the FD-SOI technology.



[1] Palma Carmona, Kenneth. "Exploration of FDSOI back-biasing techniques to hinder cryptographic attacks based on leakage current." (2023).
[2] Benea, Licinius, et al. "COSOI: True Random Number Generator Based on Coherent Sampling using the FD-SOI technology." *WiPiEC Journal-Works in Progress in Embedded Computing Journal* 10.2 (2024).
[3] Danger, Jean-Luc, et al. "Analysis of mixed PUF-TRNG circuit based on SR-latches in FD-SOI technology." *2018 21st Euromicro Conference on Digital System Design (DSD)*. IEEE, 2018.

Advancing Secure Frontier

SECURITY, RELIABILITY, POWER EFFICIENCY are increasingly demanded by the connected INTELLIGENT world



Engineered substrates build resilience and security bottom up in AUTOMOTIVE to EDGE AI

FDSOI: Inherently resilient and secure with BB as an extra leverage in secure IP

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