Reinventing the architectures for next generation 3D micro/nano systems

XENOMORPH IC

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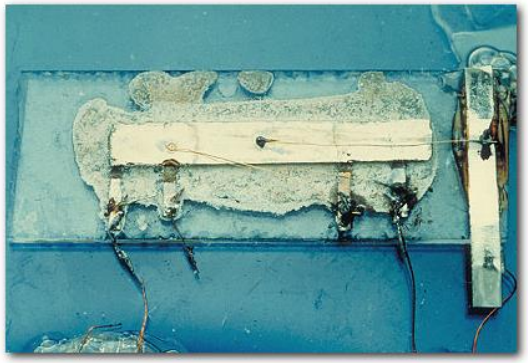
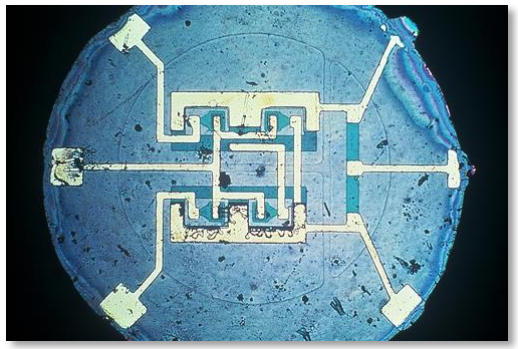
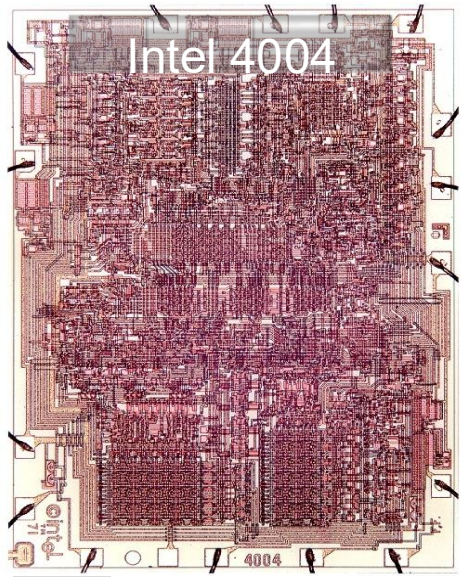
Integrated planar architectures

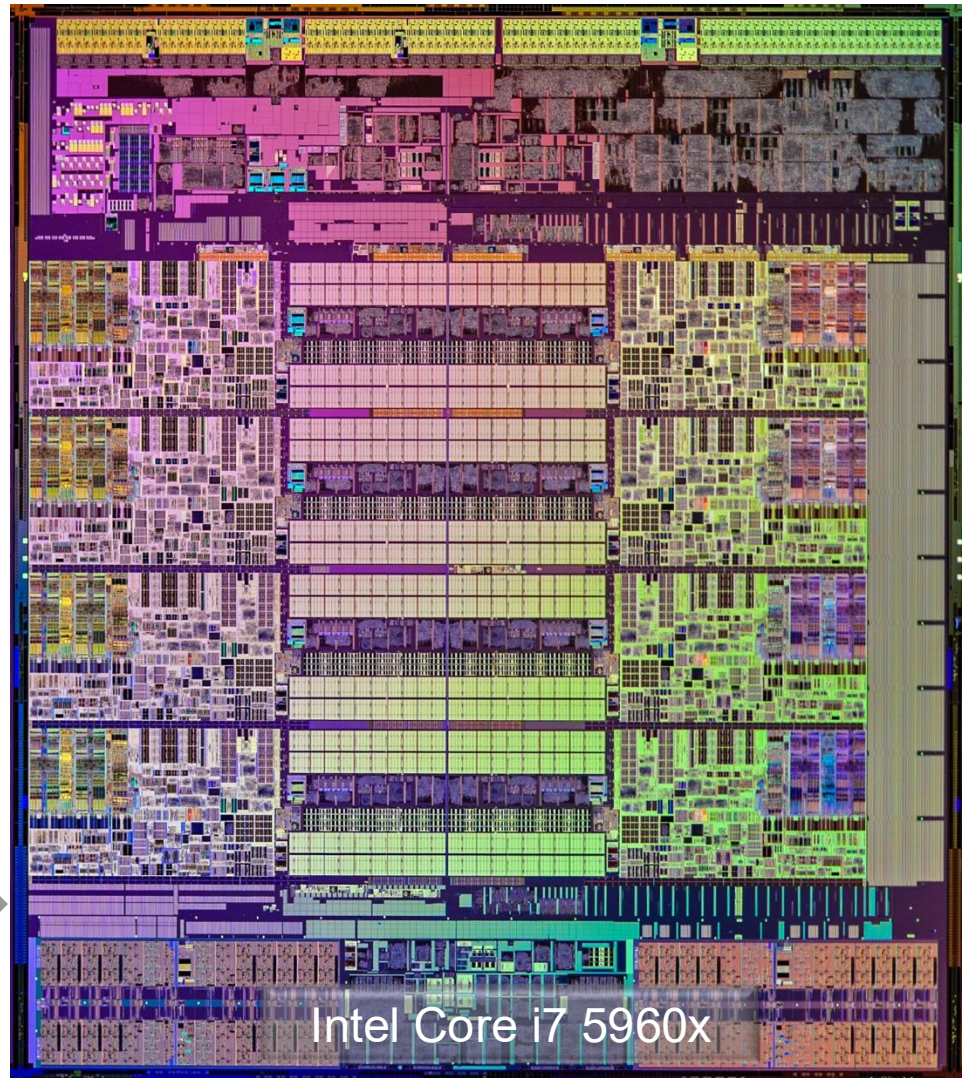




Making things smaller ➔ more and faster transistors on chip



Cost scaling
Performance



Planar process – why ?

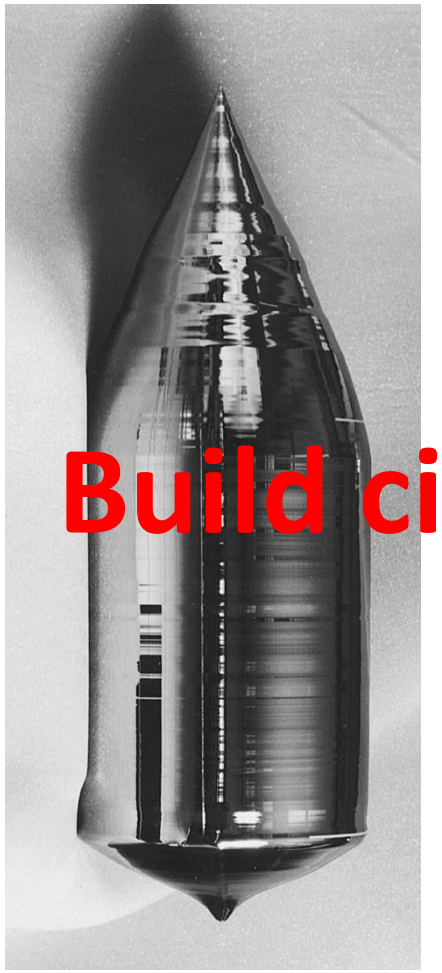
From left to right: Gordon Moore, C. Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni and Jay Last (1960)

- The **planar process** is a manufacturing pro
  semiconductor industry to build individua
  transistor, and in turn, connect those trans
  primary process by which silicon integrate
  process utilizes the surface passivation an
  methods.
- The planar process was
  by Jean Hoerni, who ac
  methods originally deve
  1957. Hoerni's planar p
  invention of the monol
  1959.

The eight who left Shockley Semiconductor were Julius Blank, Victor Grinich, Jean Hoerni, Eugene Kleiner, Jay Last, Gordon Moore, Robert Noyce, and Sheldon Roberts.
In August 1957, they reached an agreement with Sherman Fairchild, and on September 18, 1957, they formed Fairchild Semiconductor.
The newly founded Fairchild Semiconductor soon grew into a leader of the semiconductor industry. In 1960, it became an incubator of Silicon Valley and was directly or indirectly involved in the creation of dozens of corporations, including Intel and AMD.
These many spin-off companies came to be known as "Fairchildren".

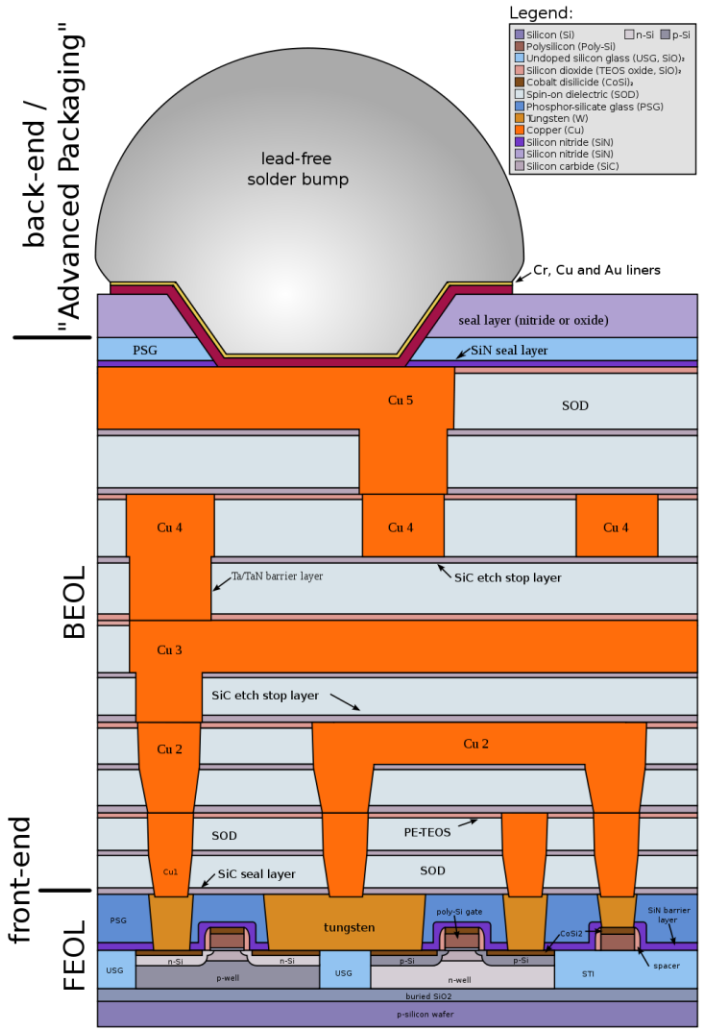
- The key concept is to view a circuit in its two-dimensional projection (a plane), thus allowing the use of photographic processing concepts such as film negatives to mask the projection of light exposed chemicals. This allows the use of a series of exposures on a substrate (silicon) to create silicon oxide (insulators) or doped regions (conductors). Together with the use of metallization, and the concepts of p–n junction isolation and surface passivation, it makes it possible to create circuits on a single silicon crystal slice (a wafer) from a monocrystalline silicon boule.
- The process involves the basic procedures of silicon dioxide (SiO_2) oxidation, SiO_2 etching and heat diffusion. The final steps involves oxidizing the entire wafer with an SiO_2 layer, etching contact vias to the transistors, and depositing a covering metal layer over the oxide, thus connecting the transistors without manually wiring them together.

Si wafers



Build circuits on a flat Surface !!

Silicon crystal grown by the Czochralski method. This large single-crystal ingot provides 300 mm (12-in.) diameter wafers when sliced using a saw. The ingot is about 1.5 m long (excluding the tapered regions), and weighs about 275 kg.
(Photograph courtesy of MEMC Electronics Intl.)



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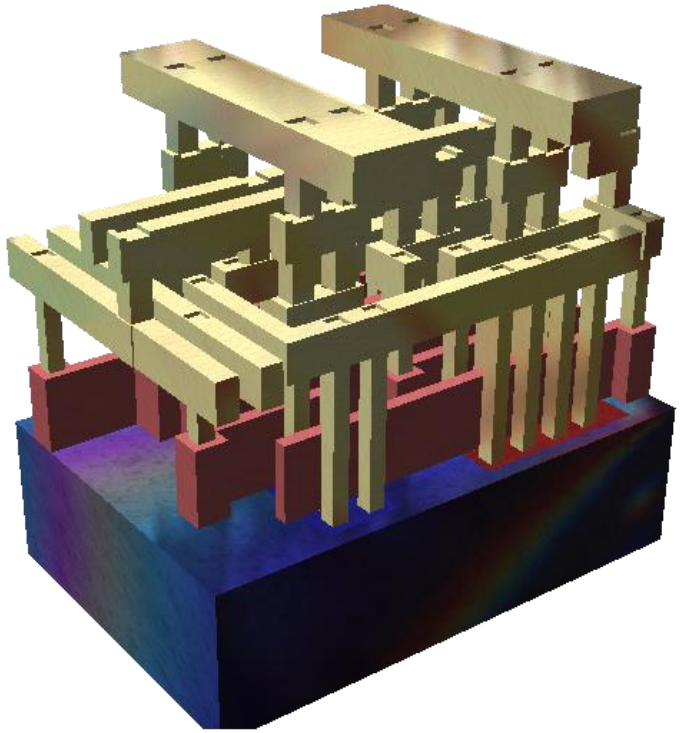

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Electrodeposition, diffusion, ion implantations, passivation, oxidation, etching, photolitography

ALL

Are processes developed for

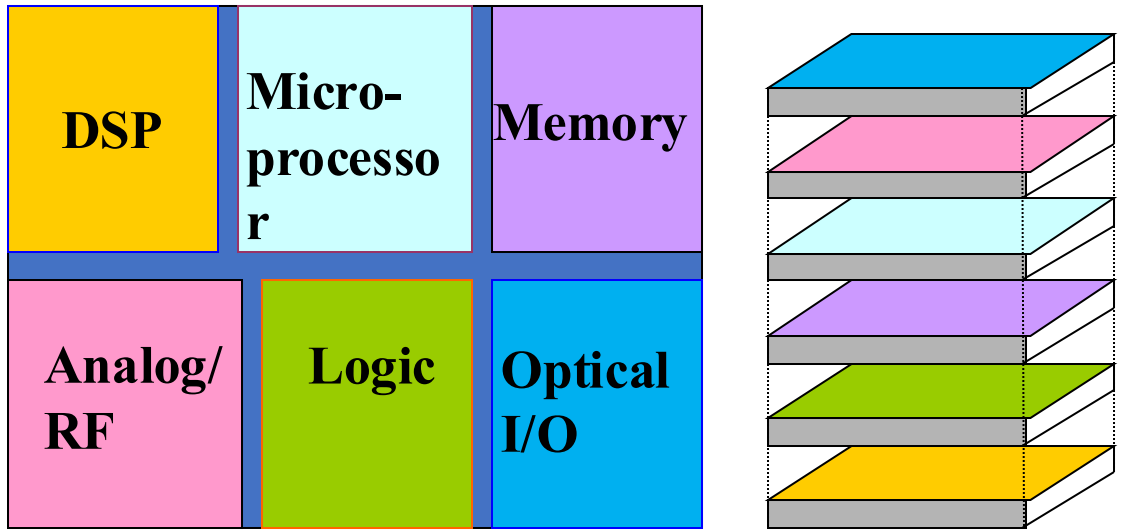
1. Application using equipment from outside the circuit
2. Well suited and developed as „planar” processes – similar to „slide projection”

Current technologies are approaching their limits!

- Size of circuit footprint (500mm^2) – yield becomes low
- Chip area limits – cost grows exponentially
- Feature size for transistor fabrication -14nm, 10nm, 7nm, 3nm what is next …?
- Width of interconnect paths + wire pitch constraint
- Signal transfer delay limits (gate delay vs. wire delay)
- Power dissipation on the chip – power consumption explosion, power efficiency bottleneck
- Extremely complicated internal geometry of buiding blocks and interconnects

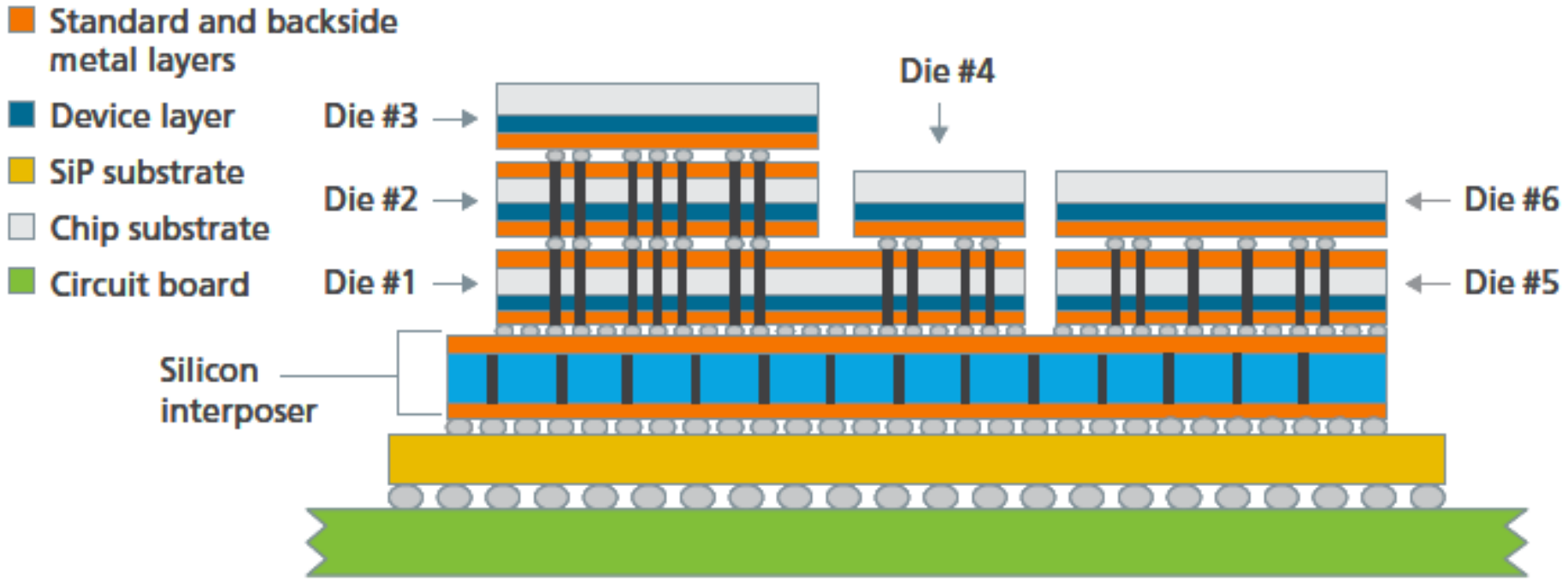
From 2D towards 3D ICs

- Multiple device layers.
- Heterogeneous integration
- Reduced wirelength
- Reduced power

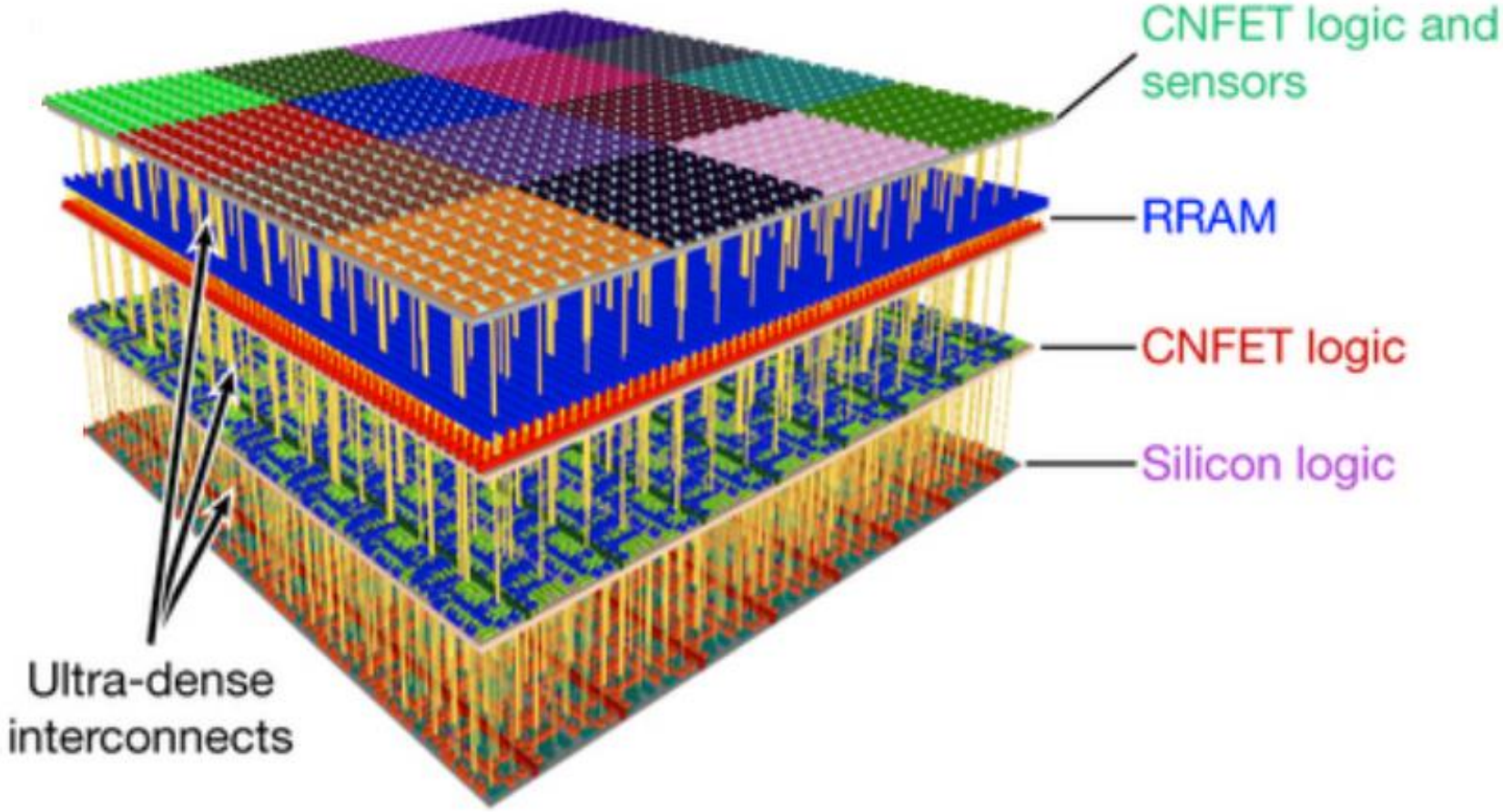


Building blocks on flat surfaces !!

Complex 3D design with multiple dies and TSVs



Advanced 3D chip construction (source Cadence: 3D ICs with TSVs—Design Challenges and Requirements)



Four vertical layers in new 3D nanosystem chip. Top (fourth layer): sensors and more than one million carbon-nanotube field-effect transistor (CNFET) logic inverters; third layer, on-chip non-volatile RRAM (1 Mbit memory); second layer, CNFET logic with classification accelerator (to identify sensor inputs); first (bottom) layer, silicon FET logic. (credit: Max M. Shulaker et al./Nature)

Important observations of the state-of-the-art:

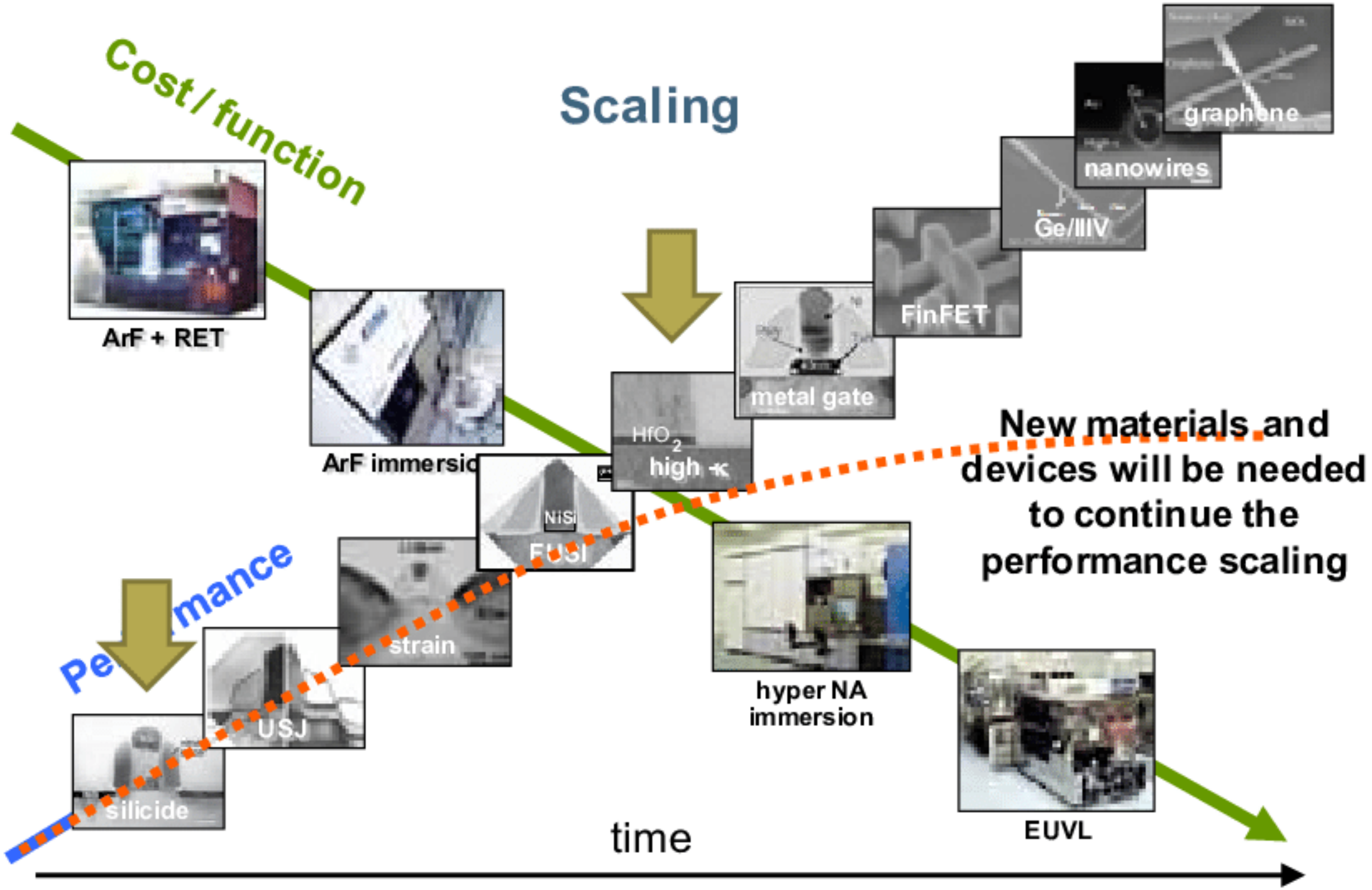
Analysis of many laboratory and industrial developments indicates that ALMOST ALL fabricated and tested chips show common features:

- **System architecture is based on flat surfaces. Going into 3D the "multi-level" architecture of superimposed flat layers is used.**
- **All building blocks are rectangular or cuboidal. Also the outer shape of the 3D chip is cuboidal.**
- **Almost all interconnects are rectilinear Manhattan-type crossing at 90deg. Even most advanced architectures offer limited interconnectivity between the building blocks in most cases limited to nearest neighbors. Small "fan-out" remains a major problem.**

Most processes are still planar !!

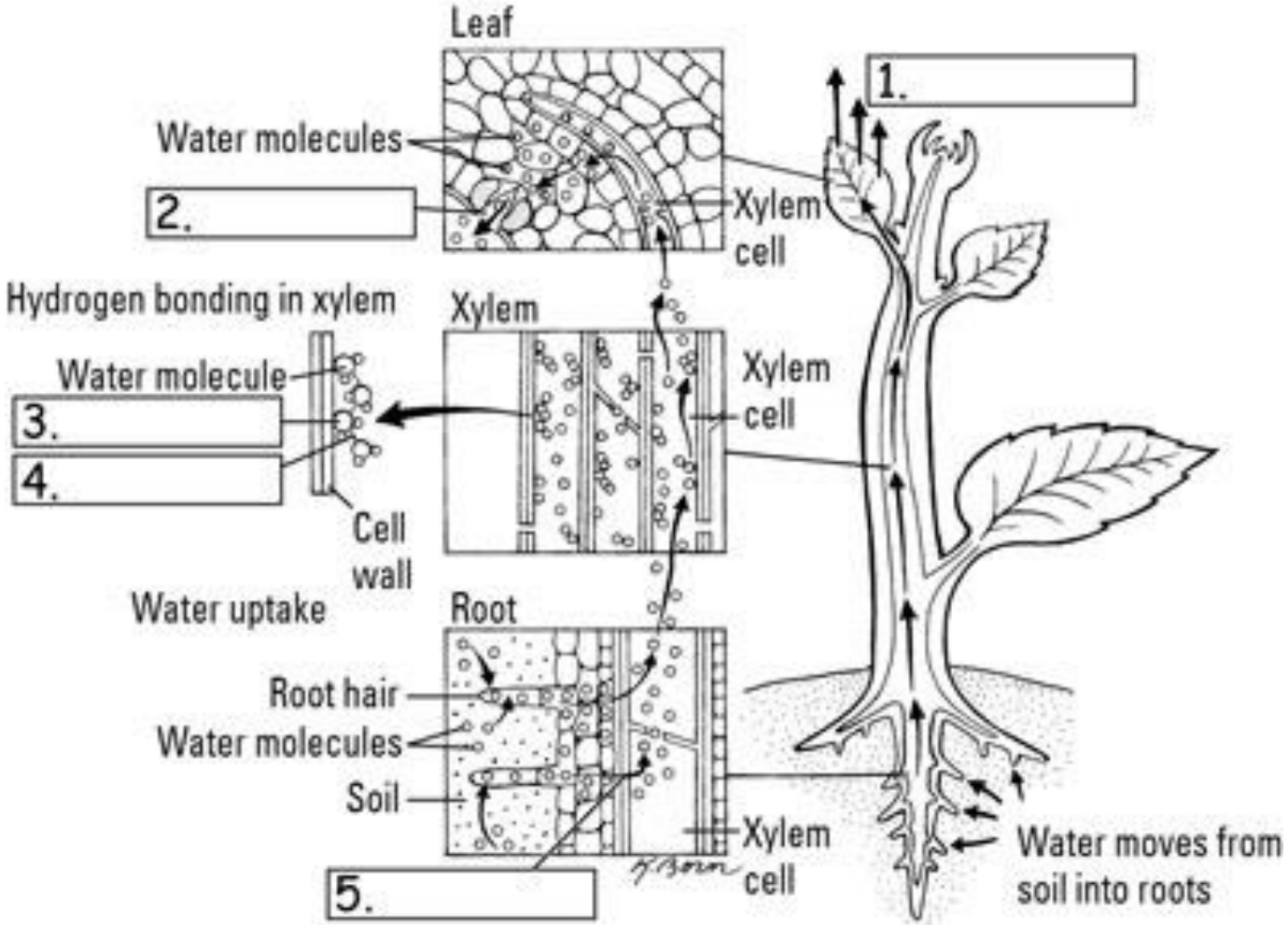
Circuits built as layered structures

- What is good about layered structures?
- What is bad in layered structures ?


Cost / function
Scaling
ArF + RET
ArF immersio
silicide
USJ
strain
NiSi
FUSI
HfO2
high-κ
metal gate
FinFET
Ge/IIIV
nanowires
graphene
hyper NA
immersion
EUVL
New materials and
devices will be needed
to continue the
performance scaling
time

What happens if we drop the planar design requirements and constraints ?

BTW> None of Nature designs is planar …



1-d.Transpiration
2-e. Stomata
3-c. Adhesion
4-a. Cohesion
5-b. Osmosis.

What happens if we drop the planar design constraints ?

- Can we design the chip structure in free 3D ?
  YES – AI can help!
- Can we optimize the layout and interconnect?
  YES – again AI can help!
- Are there technologies that could support free 3D fabrication?
  Several are ine the picture !
    - Self-assembly,
    - Nanoprinting
    - modlified “classic” technologies
    - New or even yet unknown

XENOMORPH
Concept

Academy Award for the visual design of Ridley Scott's 1979 sci-fi horror film Alien, and **was responsible for creating the xenomorph alien itself**. His work is on permanent display at the H. R. Giger Museum in Gruyères, Switzerland.

XENOS – strange, alien

MORPH – shape

Can we make a XENOMORPH CHIP ?

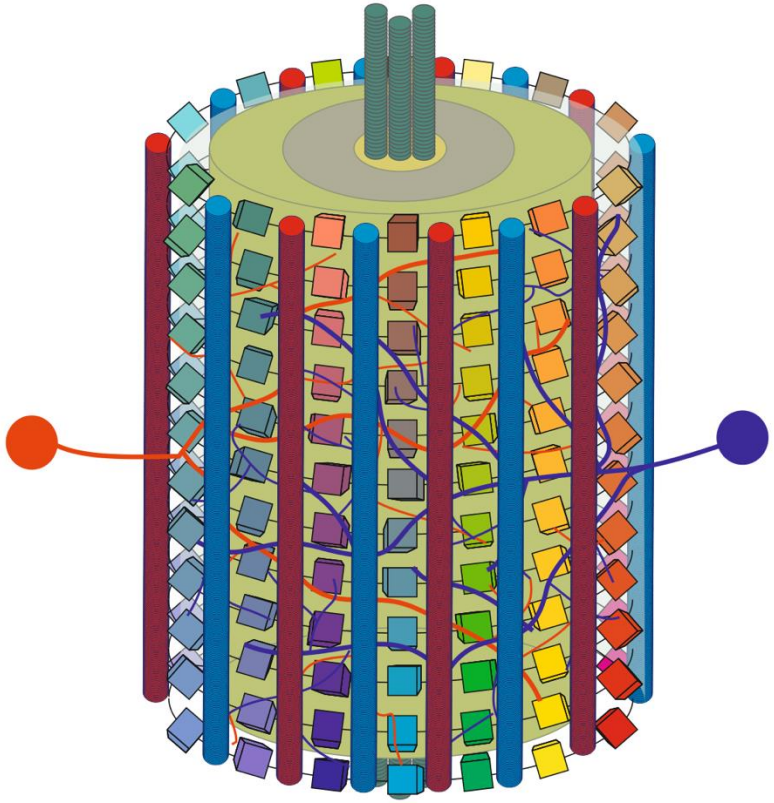
Main ideas of the XENOMOPRPH chip

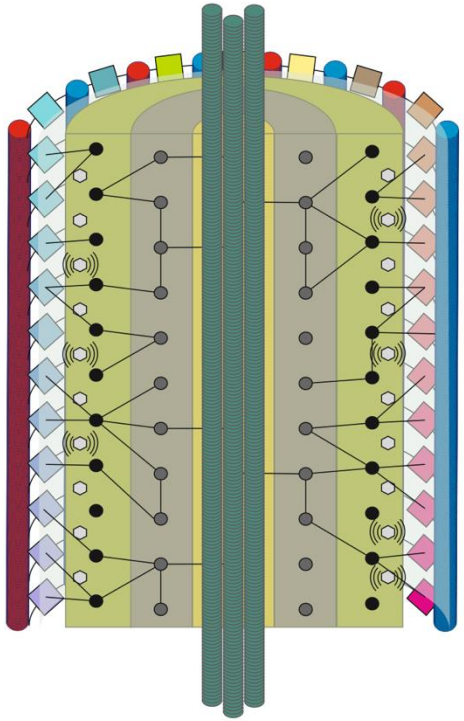
- put aside all the standing assumptions coming from earlier stages of the history of integration technologies, namely:
  - Drop the assumption of the flat footprint on which the micro-nano system has to be built;
  - Step aside from the planar process assumptions;
  - Drop the requirements for rectilinear interconnects and crossing at 90deg;
  - Allow for any reasonable shapes of building blocks.

As a consequence

- Propose a new architecture called XENOMORPH, free in the 3D space, which will offer flexibility in design and possible new optimal solutions for the designed systems.
- Propose new intelligent design strategies for systems with such properties

Explanation of the concept of XENOMORPH structure





Simple example a cylindrical architecture is used. All the building blocks and processing units are distributed on the surface of the cylinder. All power lines and clock lines (red) are connected on the surface. Blue vertical lines indicate possible cooling structure also distributed on the surface. The green-grey inner core of the XENOMORPH is used for signal interconnect/data/communication with possible high-speed optical central core. In the inner structure we propose a “smart” communication structure having also RF possibilities.

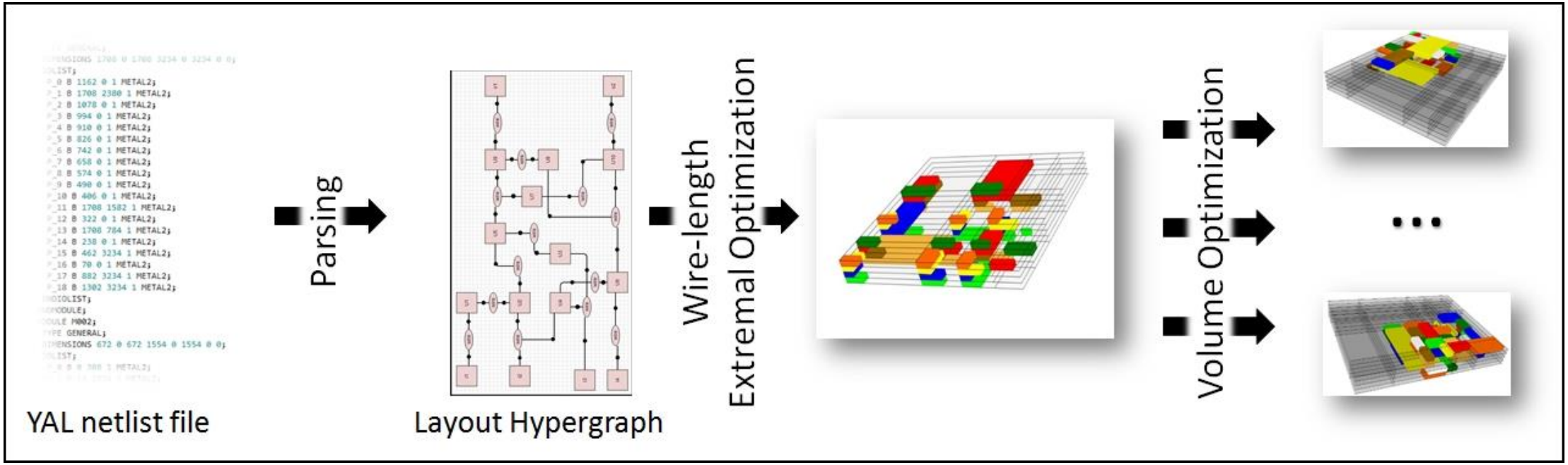
Completely new design paradigm

- optimal functionality oriented and self-organizing design process will evolve the system geometry which will be no longer constrained by the planar circuit requirement. Given an embryonic form for XENOMORPH structure, functionality description, goals to fulfill and requirements to meet, intelligent design process will morph and evolve its structure toward very specific geometry in 3D or 2D.
- XENOMORPH structure representation in form of hypergraphs: definition, properties, advantages and disadvantages of the proposed solution, embryonic form description.
- Design knowledge representation: independent from design structure knowledge definition.

XENO-morphing – intelligent design of a XENOMORPH

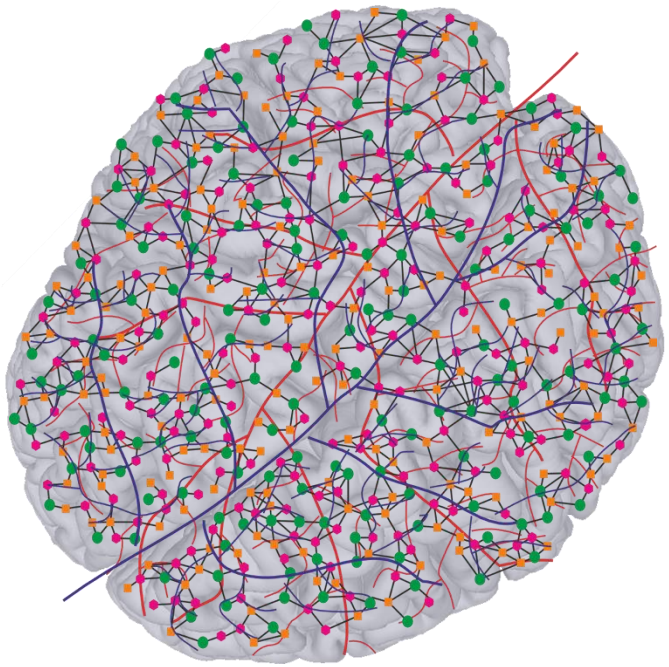
- The first approach is a **generative approach**. It uses the shape grammar as a tool to generate potential layout designs. The procedure can start from any starting block configuration, usually very simple one. The shape grammar is used by the derivation controller which directs the course of generation. The derivation controller drives the execution according to the design knowledge given by the designer in a form of goals and constraints, and its internal guidelines. The designer can interact with all the framework elements during the ongoing process of searching by freely modifying available parameters. A derivation controller (Computational Intelligence) is responsible for conducting visual computations and directing the execution.

The flow of a typical intelligent generation/optimization approach



- The second intelligent design approach concentrates on intelligent wire-length optimization for a given design structure – it is the **evolution approach**. We start from any arrangement of all components and let it **evolve** towards the optimal/acceptable solution.
- The third approach is based on a **behavior-oriented** 3D layout design optimization game where the final solution is the result of the game played by a designer. It is inspired by swarm intelligence algorithms and steering behaviors for autonomous agents in animation and computer games. The chip components are treated as autonomous agents that navigate around their world in order to find a globally near-optimal solution. Combinations of steering behaviors are used to achieve both goals and constraints of a specific layout design task.

What we expect ?



Artist’s interpretation …