

# How we design AI accelerator SoC for Data Center Network

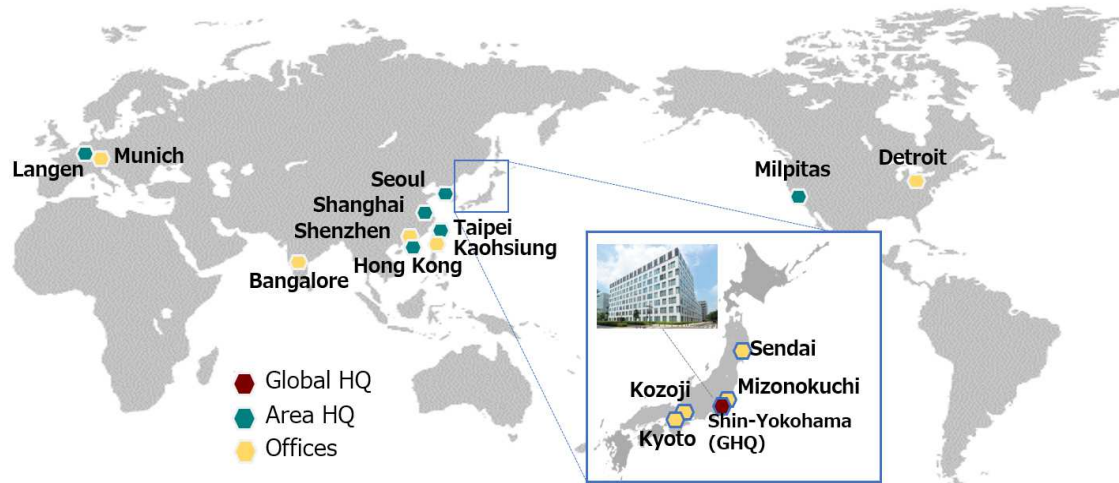
MPSoC2024  
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Socionext

Founded in 2015

IPO in 2022

1900+ Engineers, many of 20+ years experts

Offices Japan(HQ)/US/EU/China/Taiwan/India/Korea



# Focus segment

## Data Center & Networking

### Multi Core CPU



### AI Accelerator



### 5G Wireless



### Wired Network



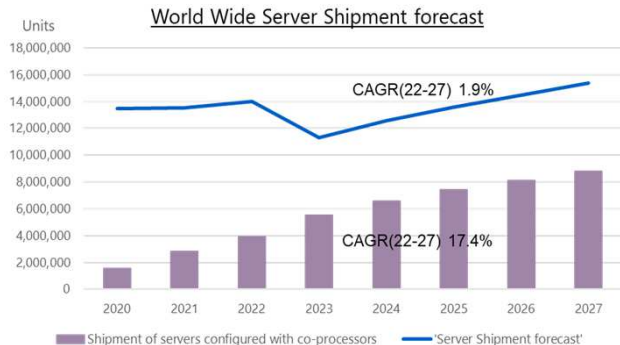
### Storage



### Optical Transporter

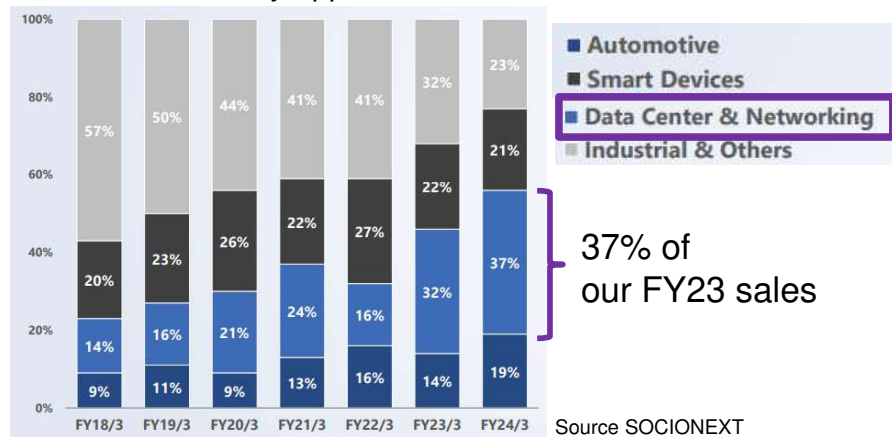


The market of server with co-processor is a growing market for CAGR(22-27) 17.4%

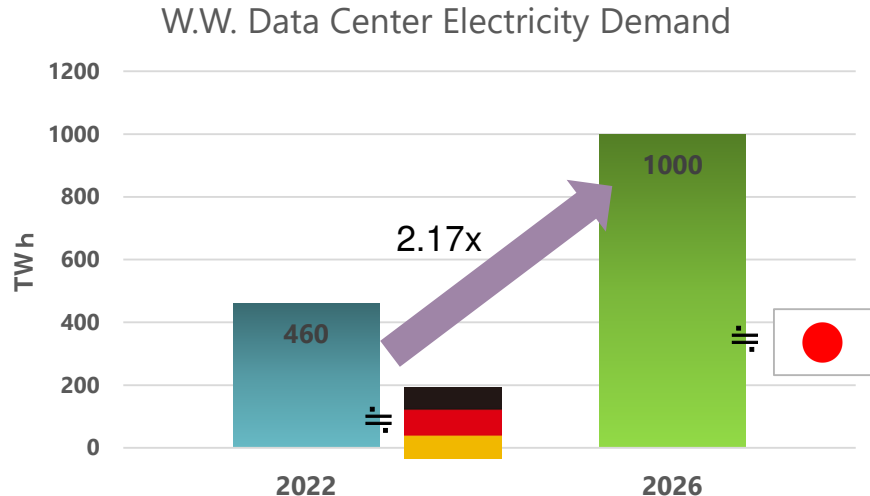
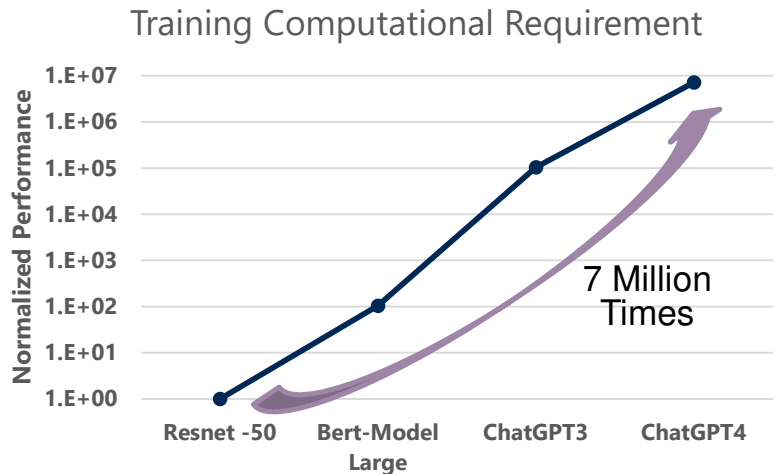
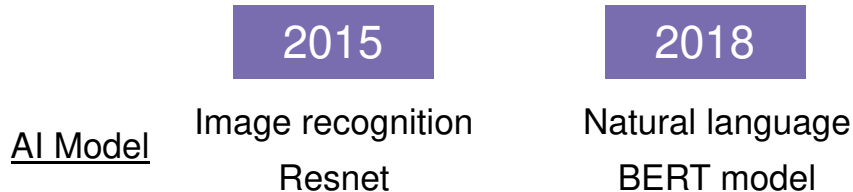


Created by SOCIONEXT based on OMDIA Long range server forecast -2H23

### Net Sales by Application



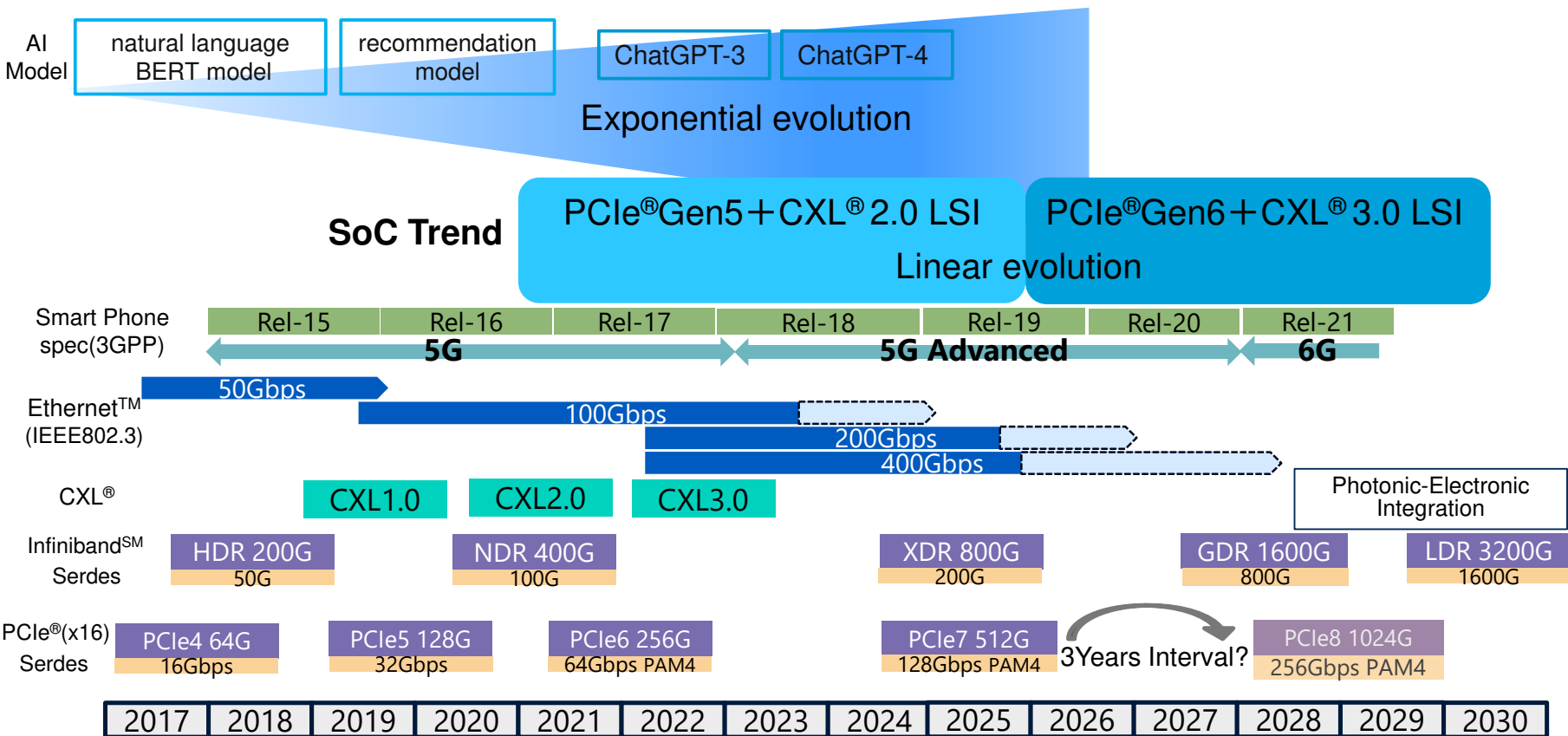
# Power consumption issues due to the spread of AI



Created by SOCIONEXT based on  
 1 Tom B. Brown et al. [2005.14165] Language Models are Few-Shot Learners (arxiv.org)  
 2 Shreyas Saxena et al. [2303.11525] Sparse-IFT: Sparse Iso-FLOP Transformations for Maximizing Training Efficiency (arxiv.org)  
 3 <https://lambdalabs.com/blog/demystifying-gpt-3>

Created by SOCIONEXT based on  
 IEA "Electricity 2024 Analysis and forecast to 2026"

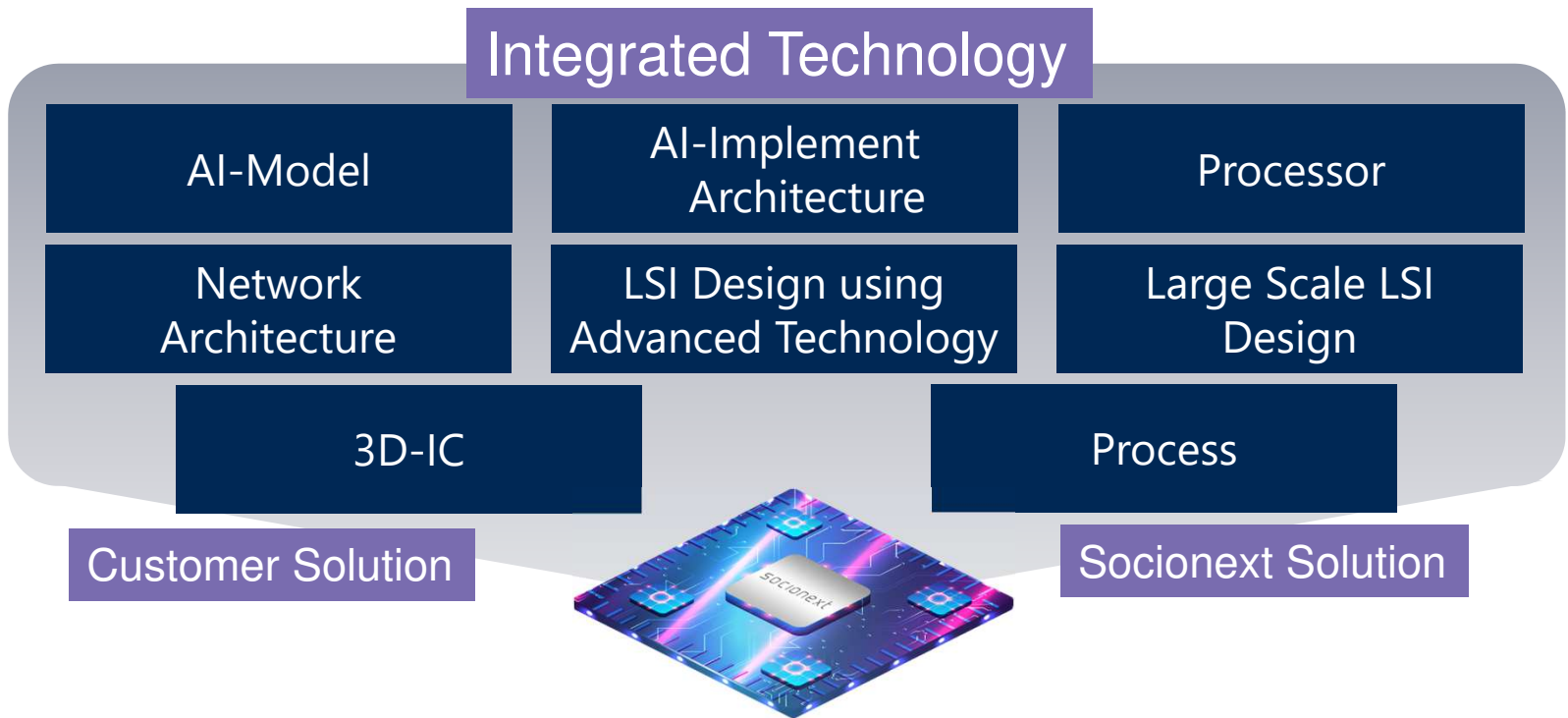
# AI & Network Trend



Source SOCIONEXT Estimate

# Integrated Technology for AI accelerator

## Symphony of technological breakthroughs



# Socionext Integrated Technology

## Integrated Technology

Large Scale LSI  
Design

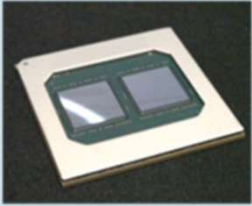
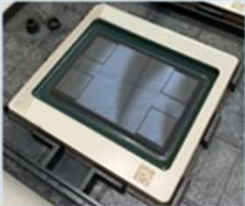

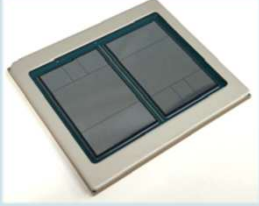
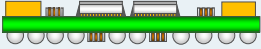
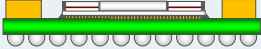
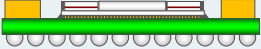
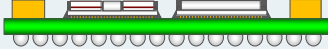
Processor

LSI Design using  
Advanced Technology

## Socionext Solution

- ✓ Advanced Package Solution
- ✓ Chiplet Design
- ✓ Multi-Core CPU
- ✓ Clock latency reduction structure

## Chiplet Package Experiences

	Device-1	Device-2	Device-3	Device-4
Appearance				
Structure	 2x SoC Die Capacitor	 1x SoC Die 4x HBM2E Si interposer w/ capacitor	 1x SoC Die 4x HBM2E Si interposer	 4x SoC Die 4x HBM3 Bridge/RDL interposer
Package	MCM-FCBGA	2.5D-FCBGA	2.5D-FCBGA	2.5D-FCBGA



## - Collaboration with Arm and TSMC on 2nm Multi-Core CPU Chiplet

  
for better quality of experience

PR20231018\_01\_207

Press Release

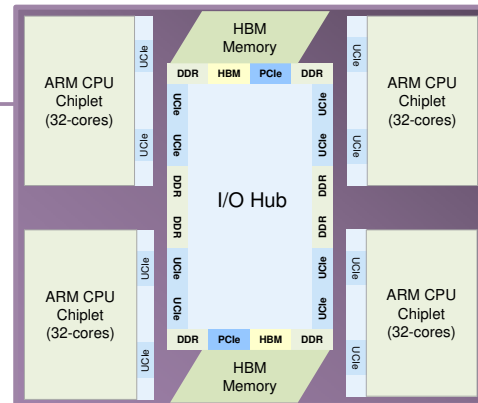
**Socionext Announces Collaboration with Arm and TSMC on 2nm Multi-Core Leading CPU Chiplet Development**

*Next-Generation Compute Chiplet-based Proof-of-Concept Leverages Arm Neoverse CSS Technology and TSMC Silicon Process Along with Advanced Packaging Technology*

**[Yokohama, Japan October 18, 2023]** --- Socionext today announced a collaboration with Arm and TSMC for the development of an innovative power-optimized 32-core CPU chiplet in TSMC's 2nm silicon technology, delivering scalable performance for hyperscale data center server, 5/6G infrastructure, DPU and edge-of-network markets.

This advanced CPU chiplet proof-of-concept using Arm® Neoverse™ CSS technology is designed for single or multiple instantiations within a single package, along with IO and application-specific custom chiplets to optimize performance for a variety of end applications.

Leveraging CPU chiplets, and customized application-specific chiplets, multiple target applications can be supported. When new chiplets become available, a cost-effective package level upgrade path can be supported.



128 CPU core HPC Soc(Image)

# Clock latency reduction structure

Minimize latency and skew by using three different clock structures

Explore the best clock structure

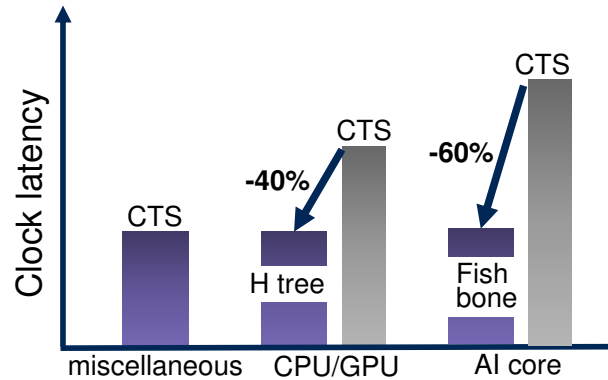
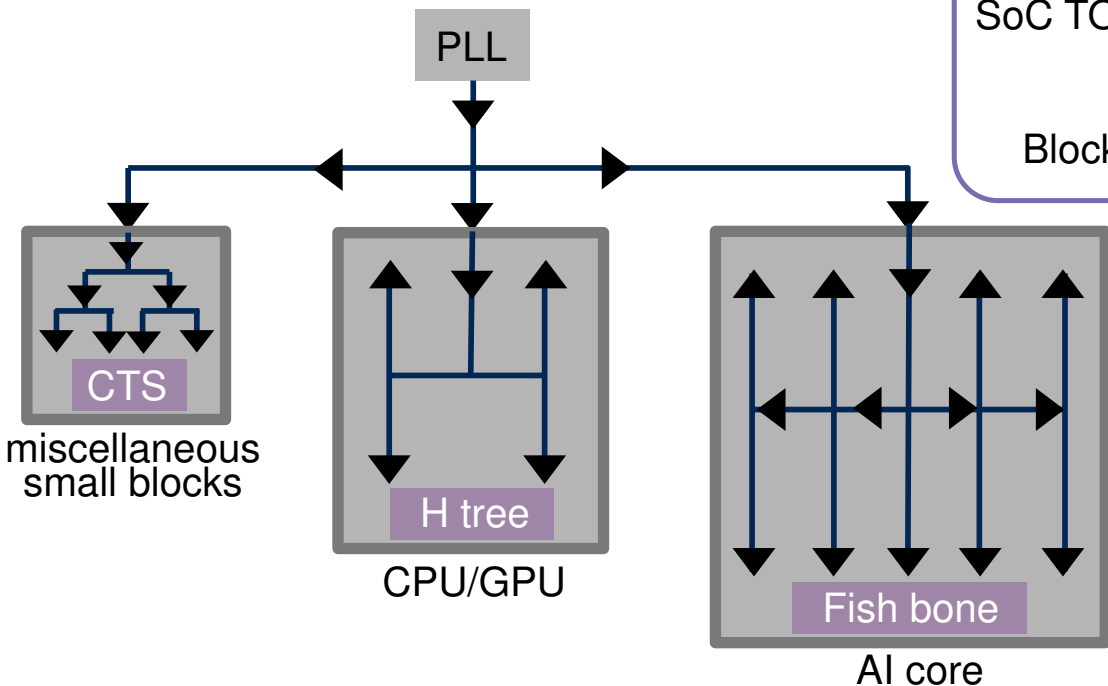
SoC TOP

- ✓ Search for clock distribution path
- ✓ Evaluate on chip variation



Block

- ✓ Analyze clock skew and latency
- ✓ Determine clock structure



# Summary

- ✓ Data center semiconductors will continue to drive technology.
- ✓ On the other hand, it is also a factor contributing to the global power challenge.
- ✓ Socionext aims to balance technology evolution and power challenges with Integrated Technology.

