How Can SFQ Technology Contribute to Quantum Computing?

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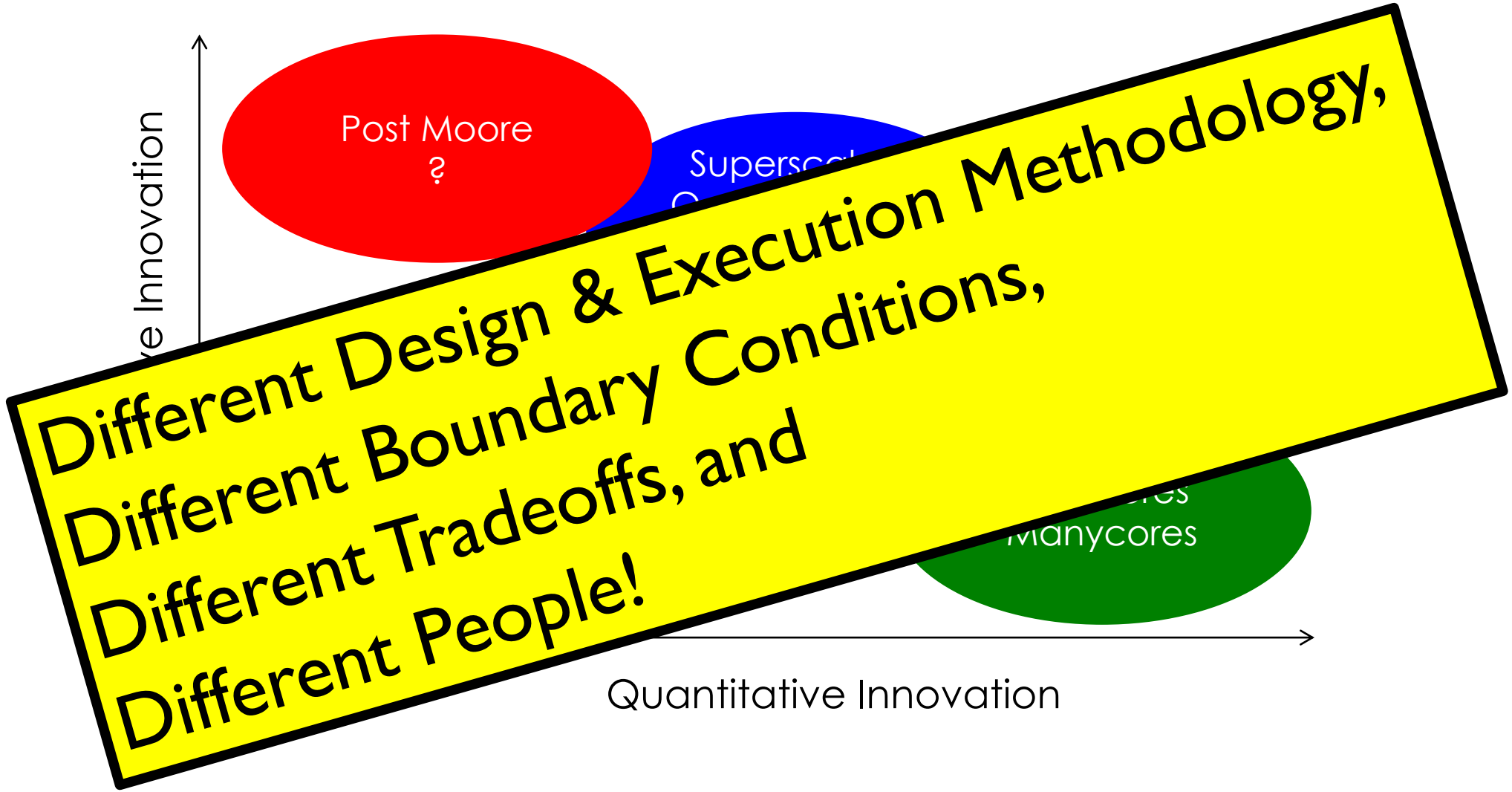
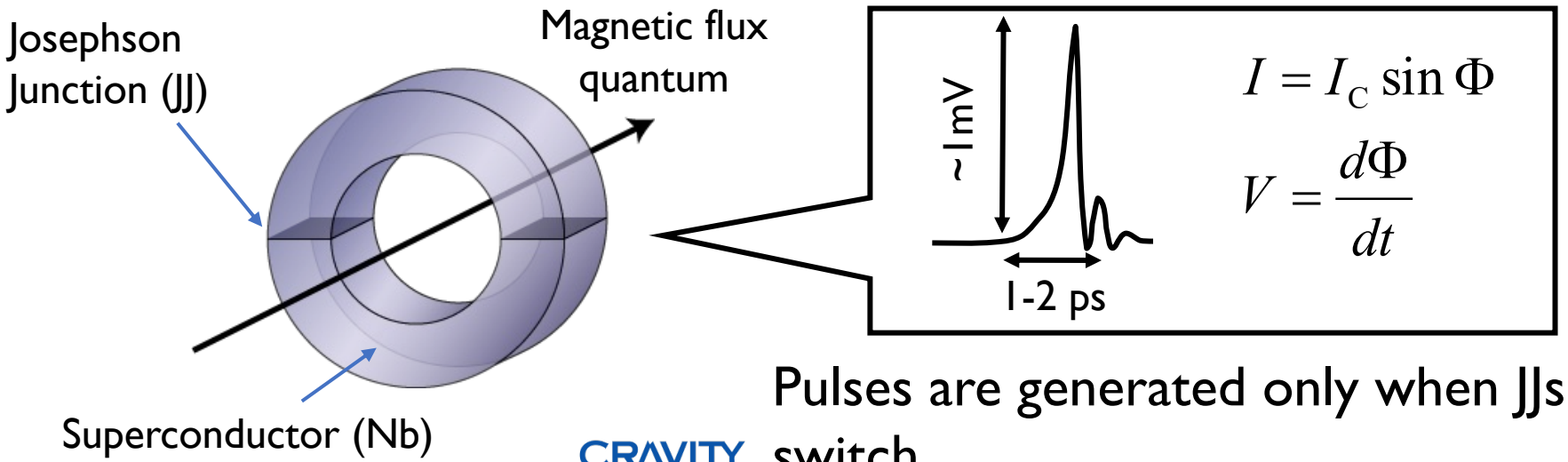
(Collaborated research w/ Nagoya Univ. and SNU)

What is the Architectural Challenge in Post-Moore's Era?

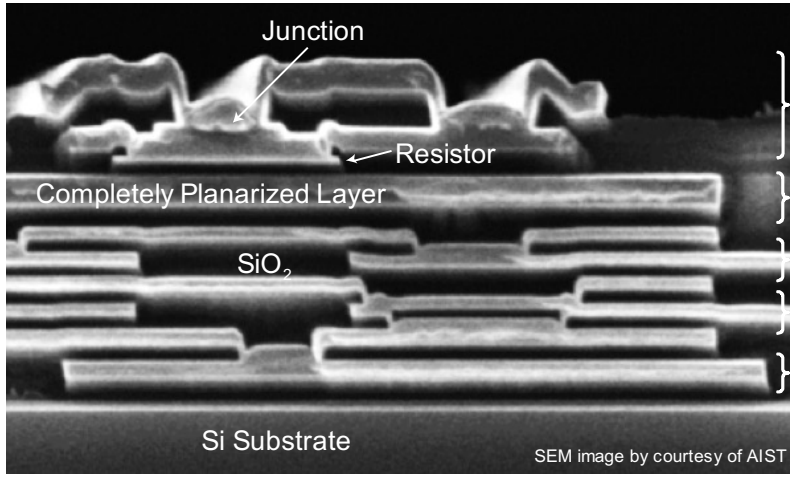


Single-Flux-Quantum (SFQ) Logic

SFQ Device & Circuit



Pulses are generated only when JJs switch.

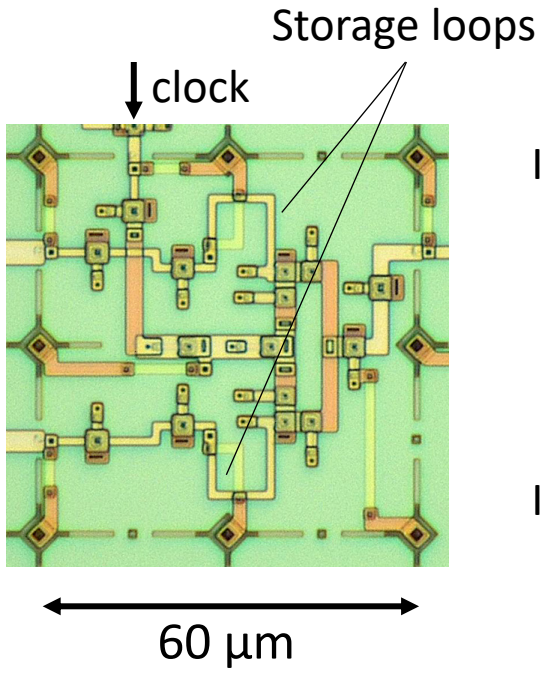


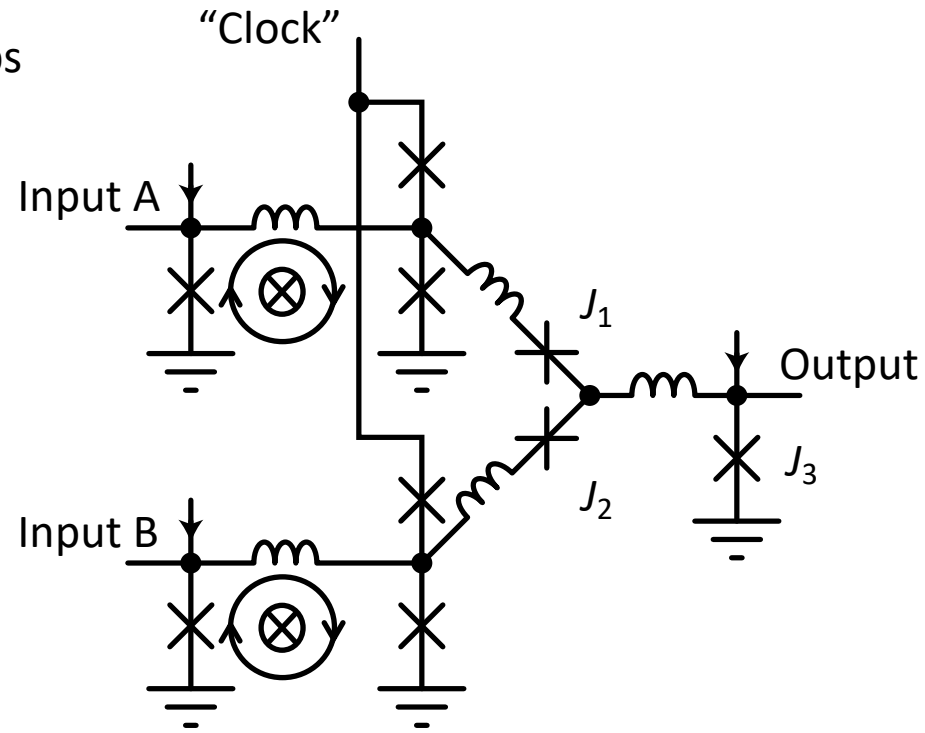
S. Nagasawa et al. *IEICE Trans. Electron.* **E97-C** (2014) 132–140.

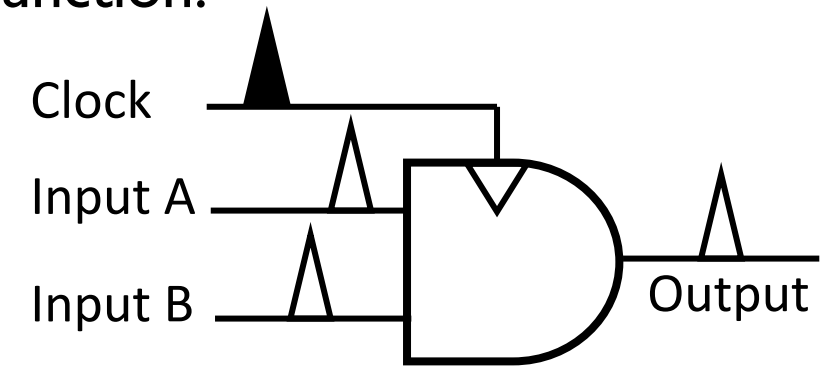
- **Extremely low power**
  ~1 μW gates operating at 100 GHz
- **High-speed operation**
  >100 GHz demonstrations, etc.
- **Ultrafast interconnects**
  Signal transmission at the speed of light (SFQ has no mass)

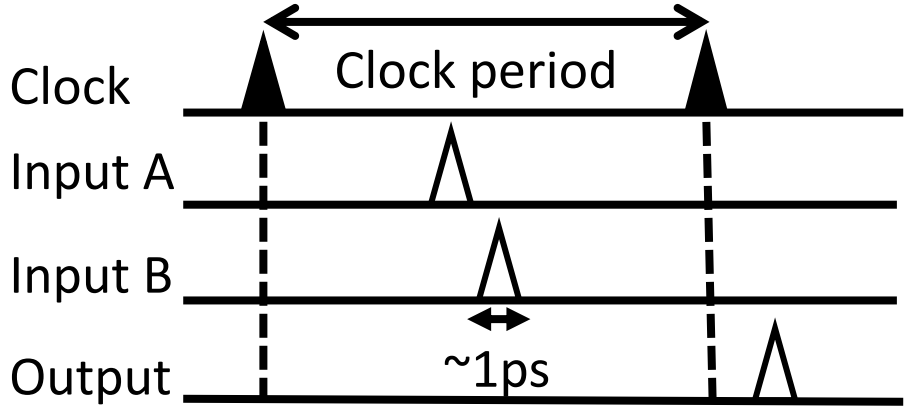
SFQ Logic Gate (AND)

- Use "Clock" as a timing reference for synchronization.
- Every logic gate is clocked gate and has the latch function.







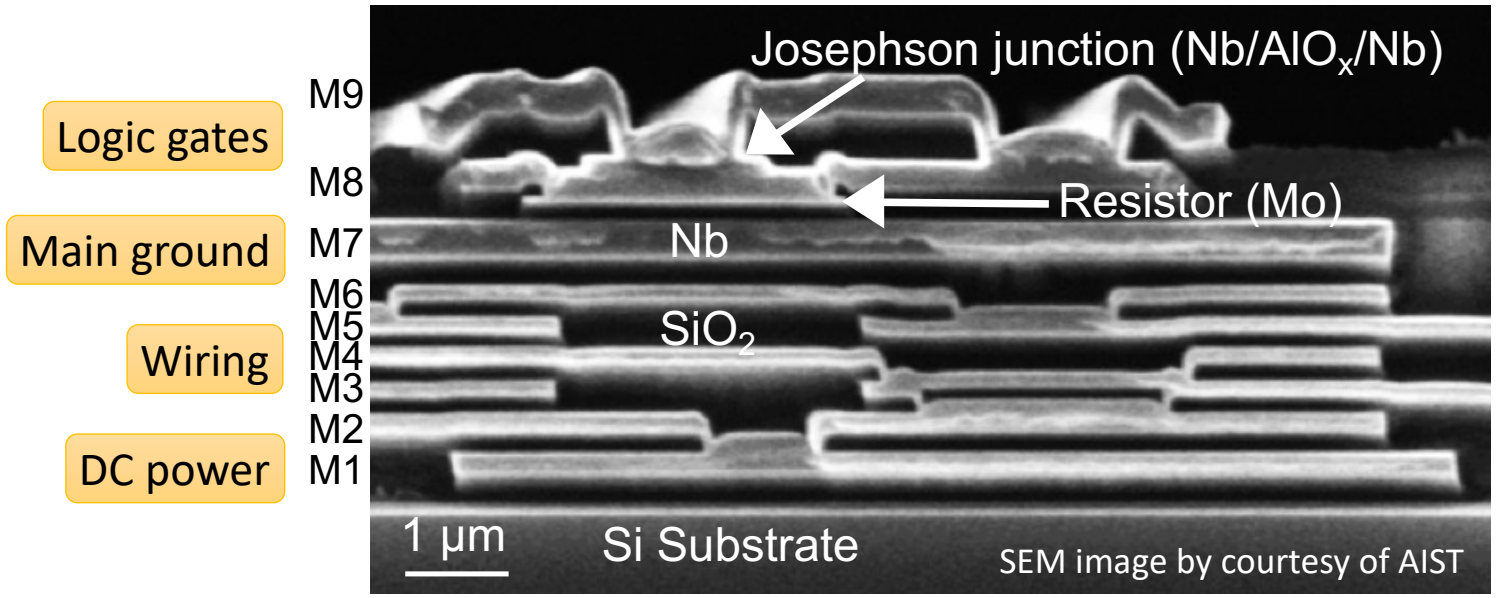


Fabrication Process

- 3–10 layer process is under development in Japan, US, and China.

AIST Advanced Process, Japan

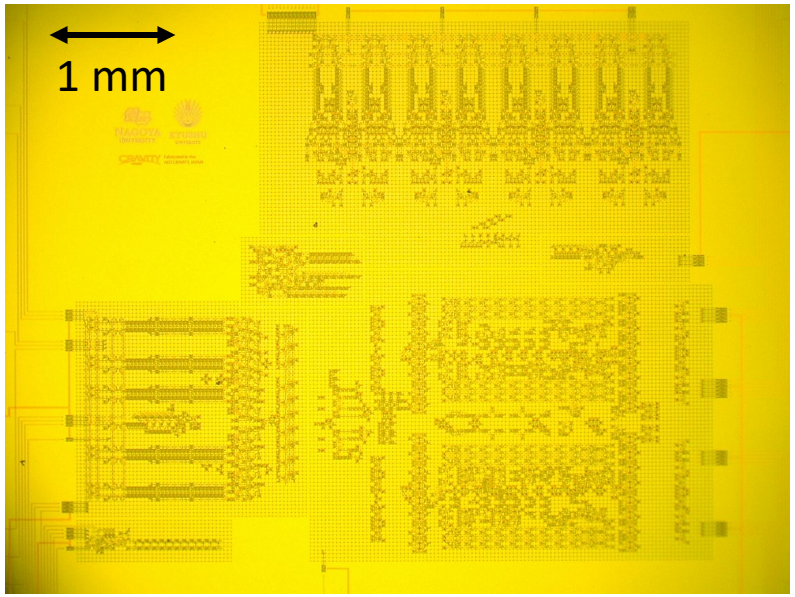
1-μm sq. JJ, Nb 9-layer + Mo



S. Nagasawa et al. *IEICE* **E97-C** (2014) 132-140.

32-GHz, 6.5-mW SFQ MPU

25,403 JJs, 4.1 x 5.3 mm^2

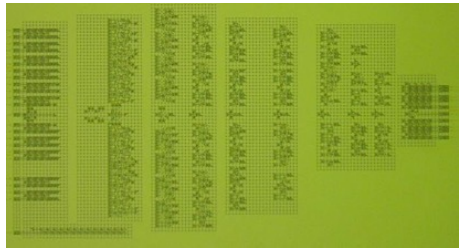


K. Ishida et al., VLSI 2020

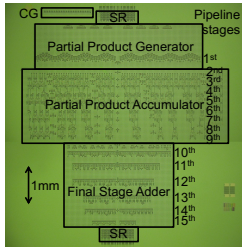
Our Approach & Outcome

Device/Circuit Optimization

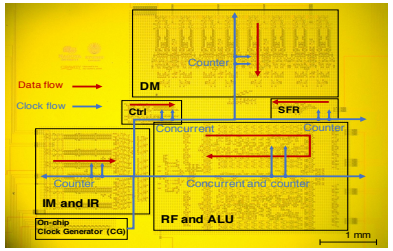
Architectural Optimization



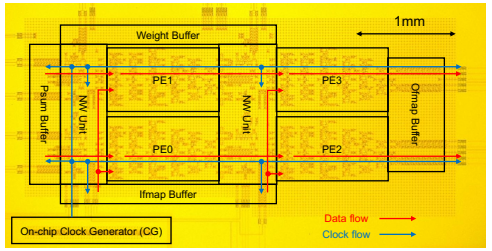
56GHz 1.6mW ALU
ISLPED'17 Design Contest
Honorable Mention



48GHz 5.6mW Multiplier
ISSCC'19
SilkRoad Award

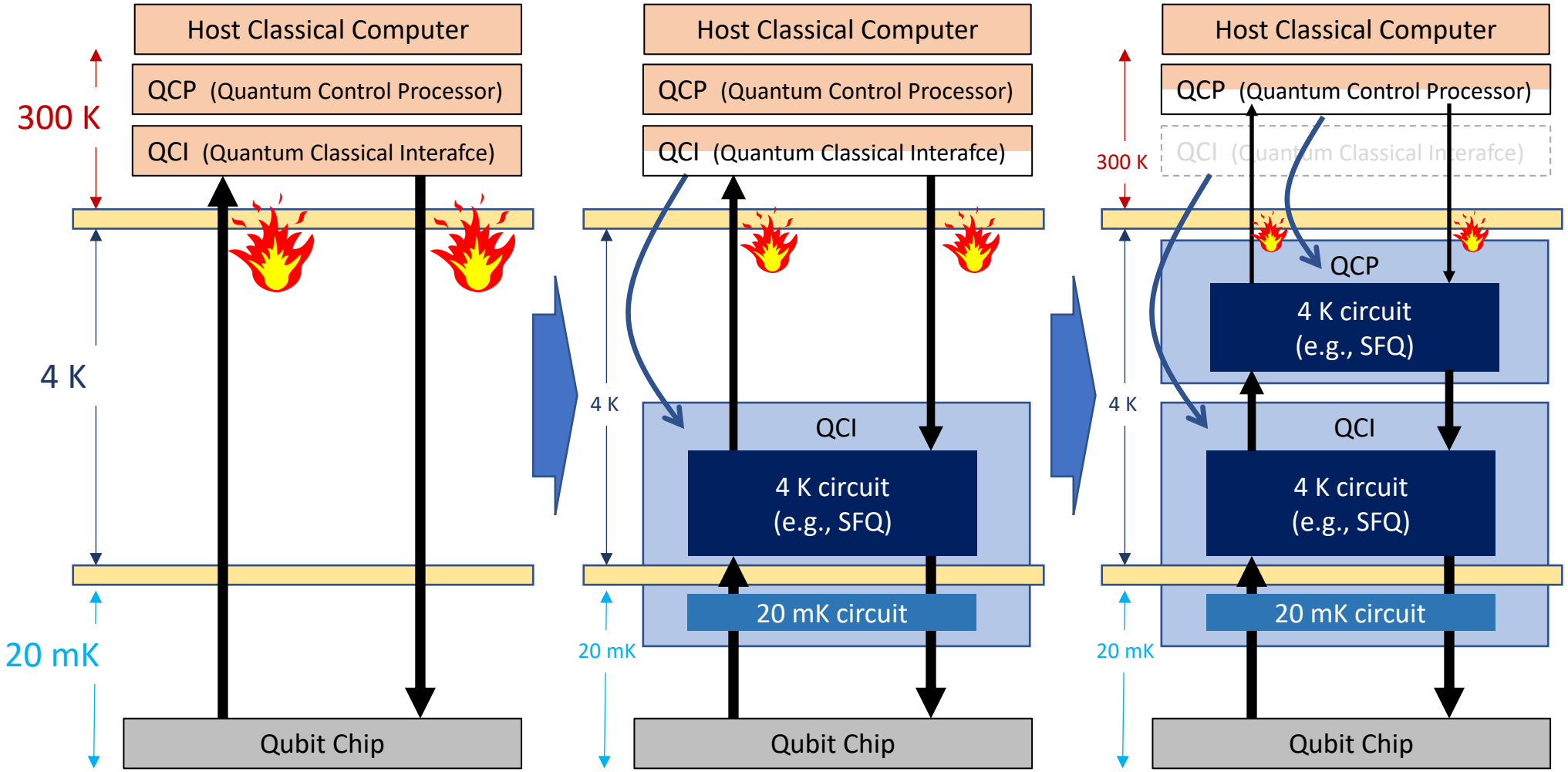


32GHz 6.2mW Processor
VLSI Symposium'20
Selected as a featured paper



50GHz AI Accelerator
MICRO'20

How can SFQ Technology Contribute to Superconducting Quantum Computers?

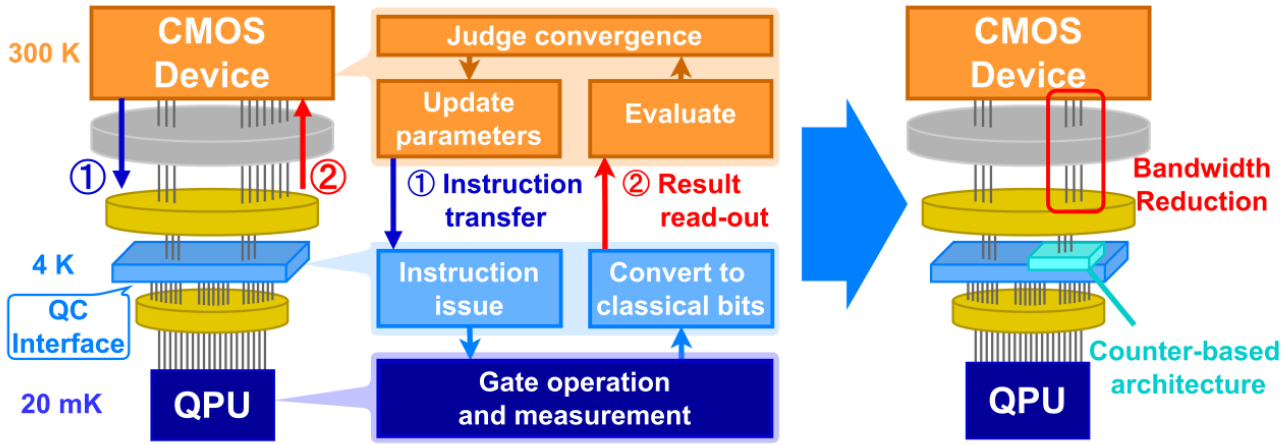


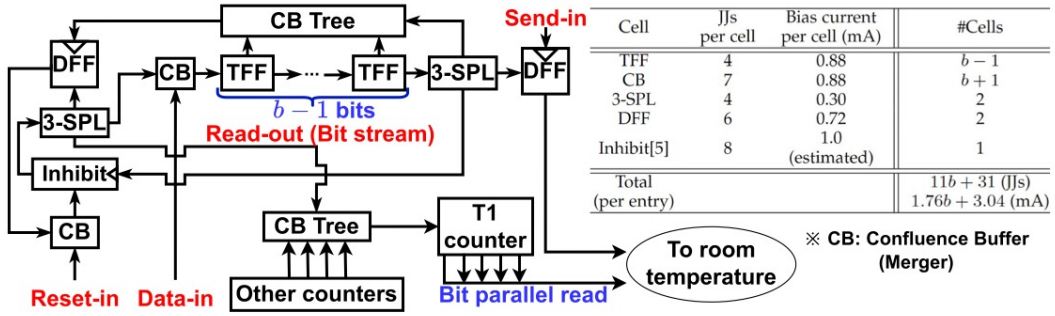
A Case for NISQ Machine

Computer Architecture Letter'24

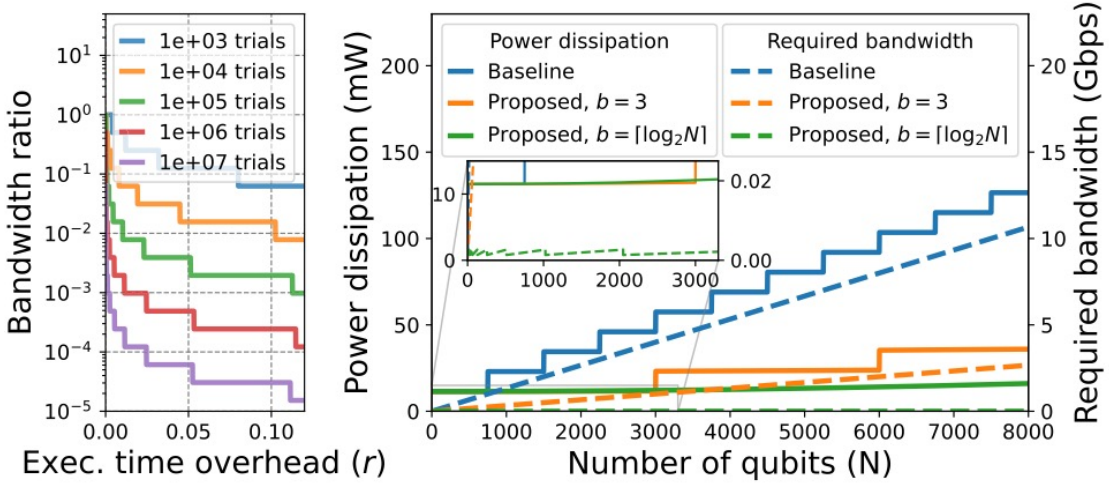
Ueno et al., "Inter-Temperature Bandwidth Reduction in Cryogenic QAOA Machines," IEEE CAL, Jan.-Jul. 2024.
Ueno et al., "SFQ counter-based precomputation for large-scale cryogenic VQE machines," DAC WIP Poster, July 2024.

System Level Architecture Optimization





Cell	JJs per cell	Bias current per cell (mA)	#Cells
TFF	4	0.88	$b-1$
CB	7	0.88	$b+1$
3-SPL	4	0.30	2
DFF	6	0.72	2
Inhibit[5]	8	1.0 (estimated)	1
Total (per entry)			$11b+31$ (JJs) $1.76b+3.04$ (mA)

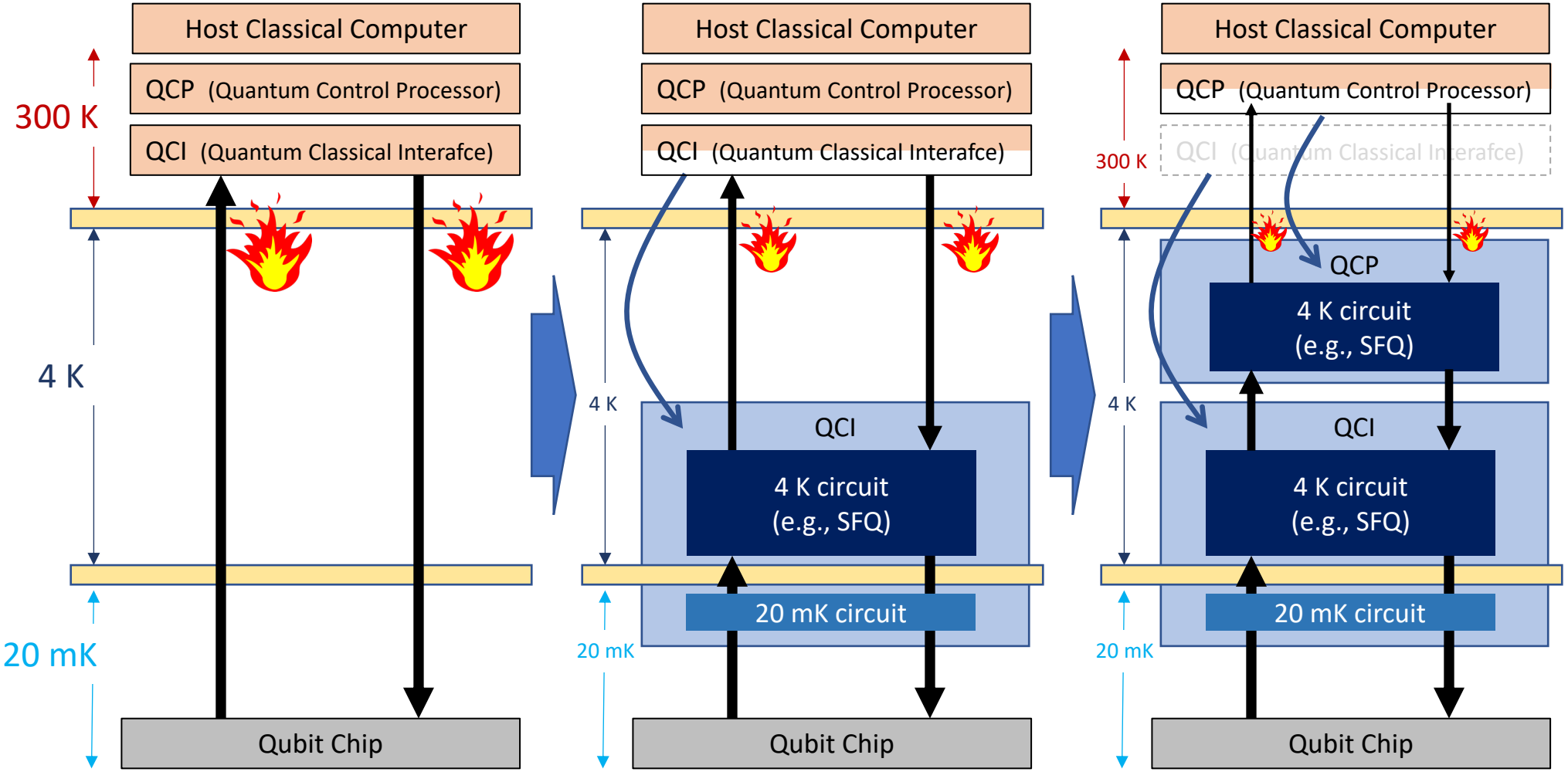


- Superconducting quantum computer requires many inter-temperature cables
  - Hardware complexity, heat inflow, peripheral power, etc.
- For QAOA, qubit measurement readout communication is the dominant
- Counter-based SFQ architecture reduces meas. Bandwidth

Towards Fault-Tolerant Quantum Computing

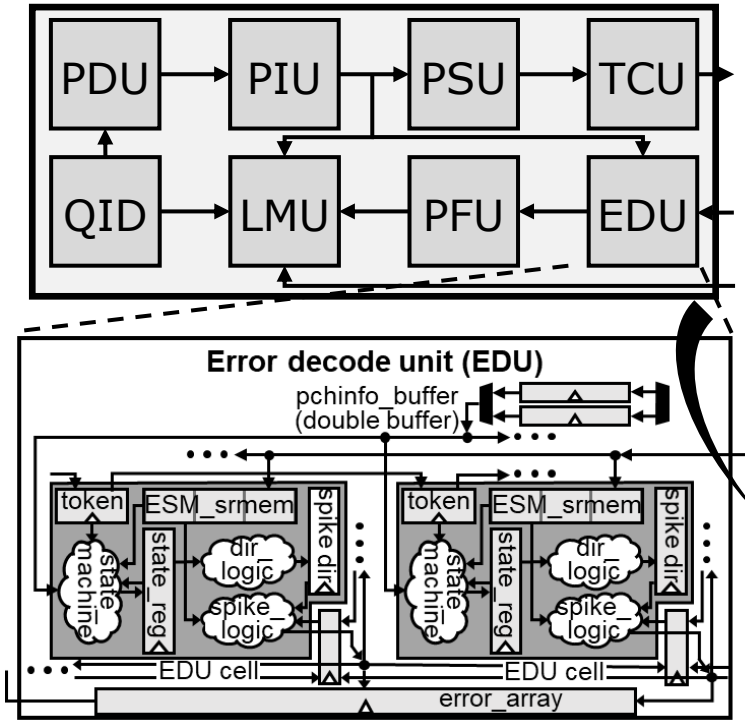
ISCA'22&ISCA'23

How SFQ Technology Contribute to Superconducting Quantum Computers?



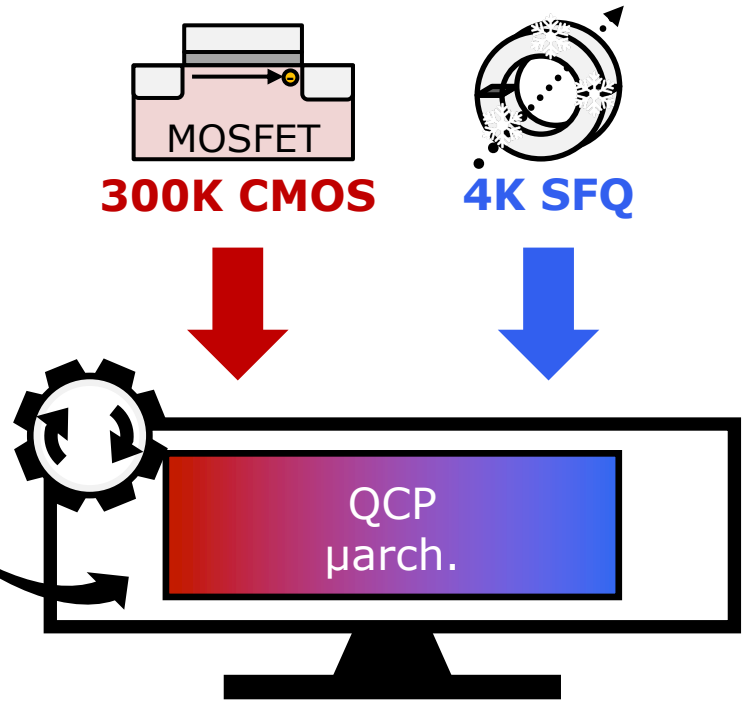
XQsim: Research Overview

Full QCP μarchitecture



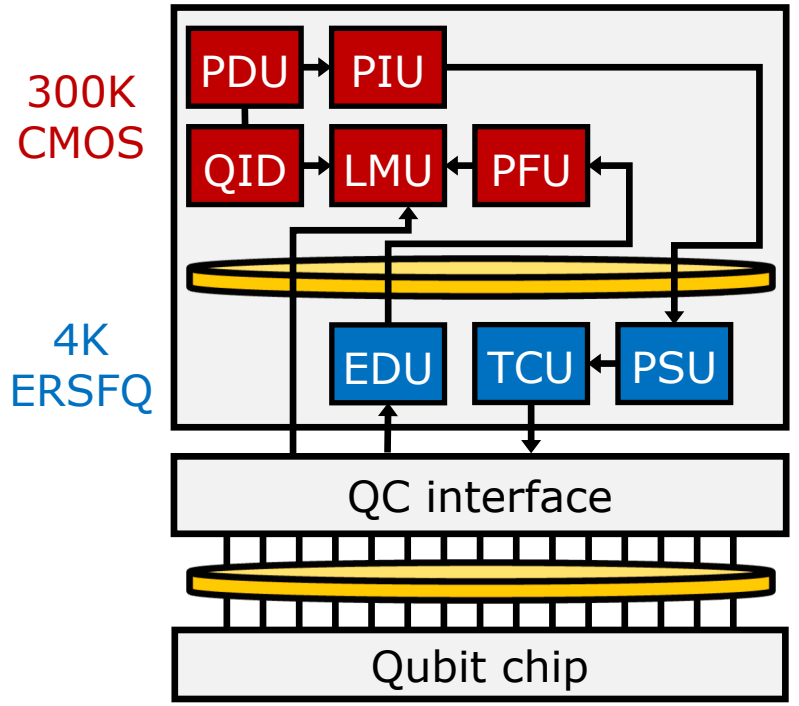
Detailed RTL impl. & validation

QCP modeling tool



Cross-technology modeling & simulation

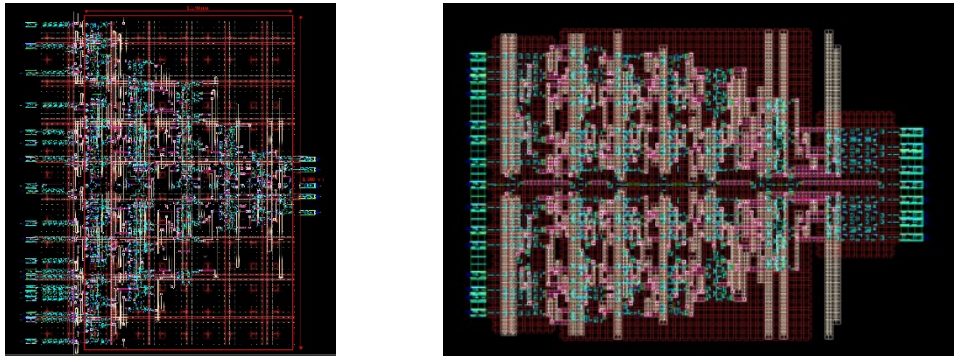
10+K qubit QCP arch.



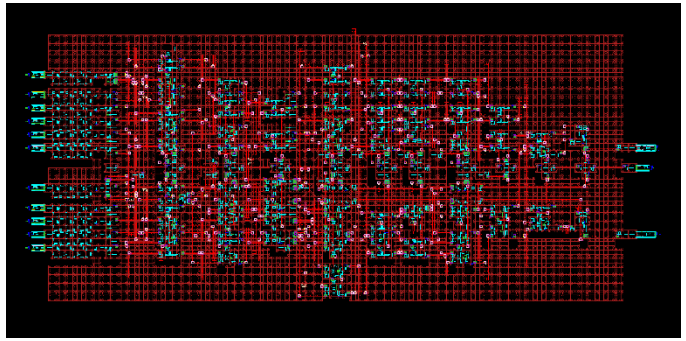
Temp. & Tech. & Arch. optimizations

XQ-estimator: Validation

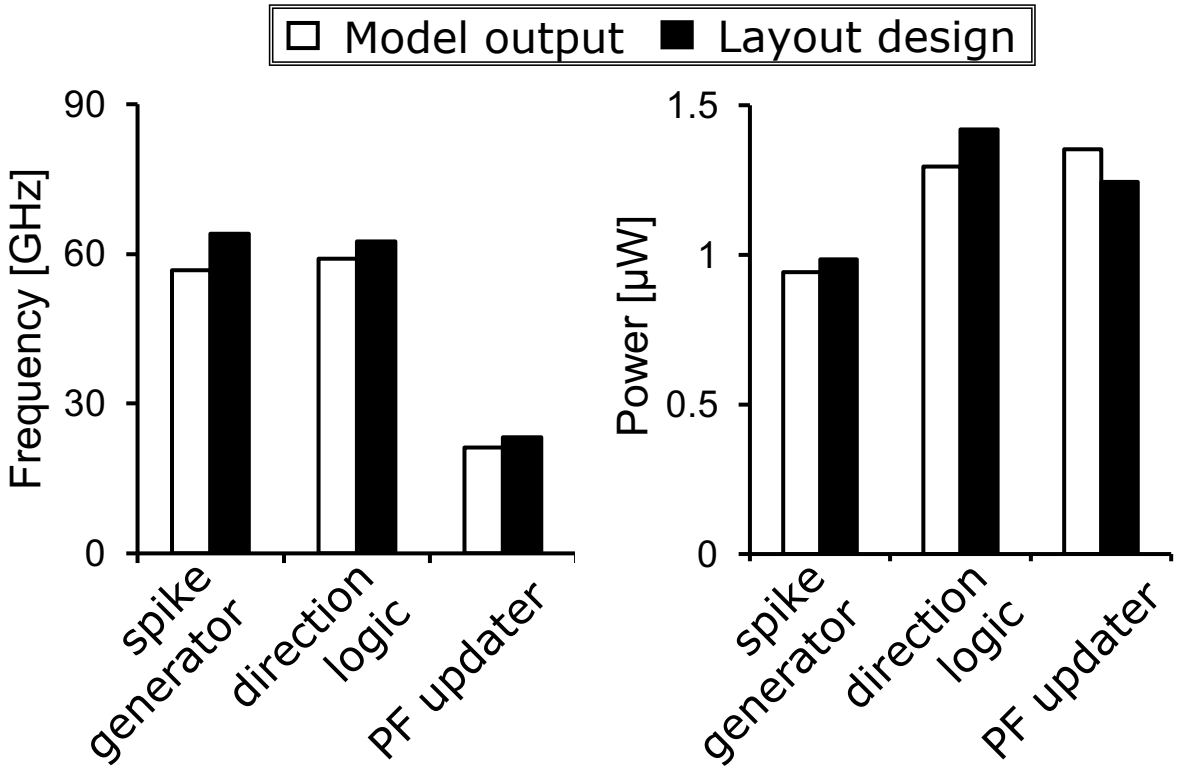
- **SFQ model accurately predicts the frequency and power**
  - Compared with the post-layout analysis using AIST 1.0μm process library
  - Validated with the circuits in various QCP units (e.g., EDU, PFU)



Layout of spike generator and direction logic inside EDU

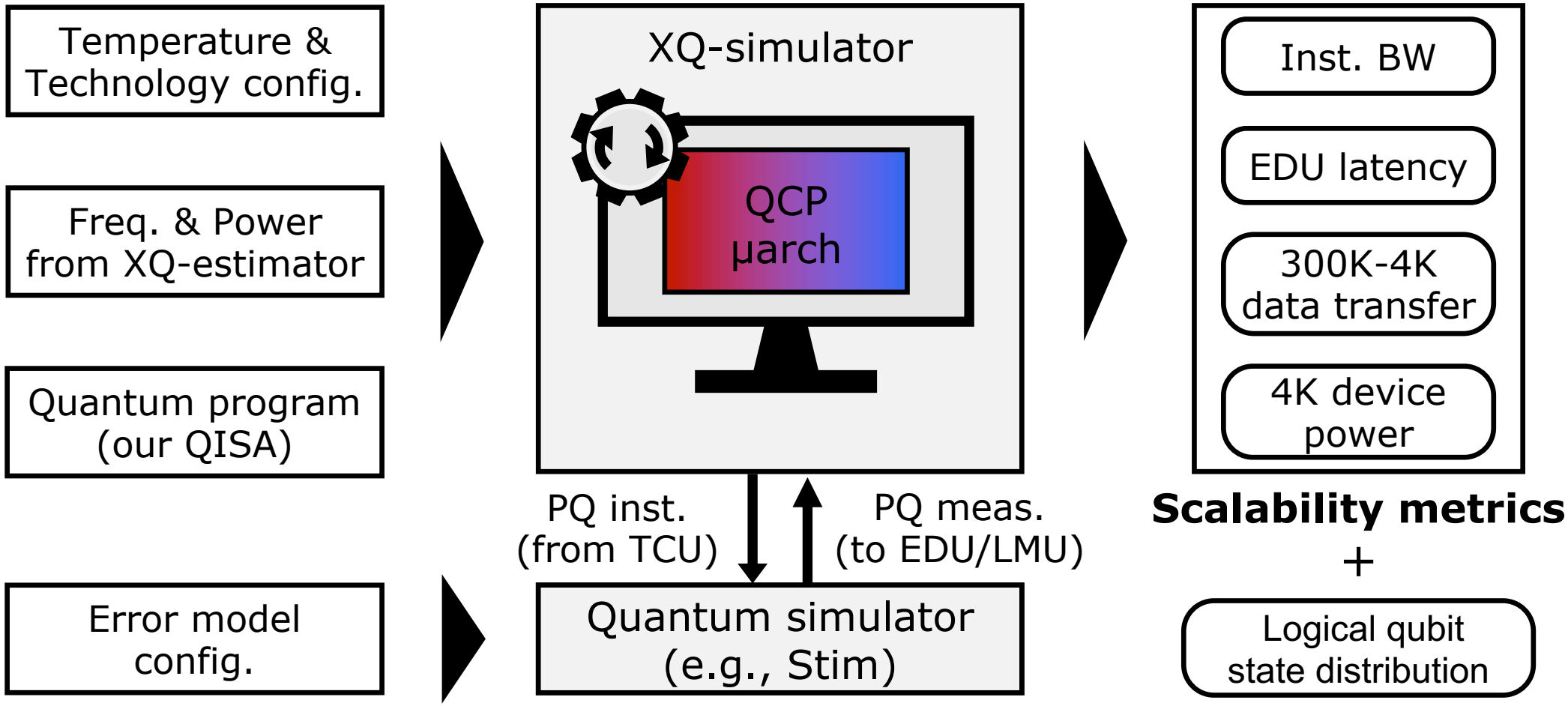


Layout of PF updater inside PFU



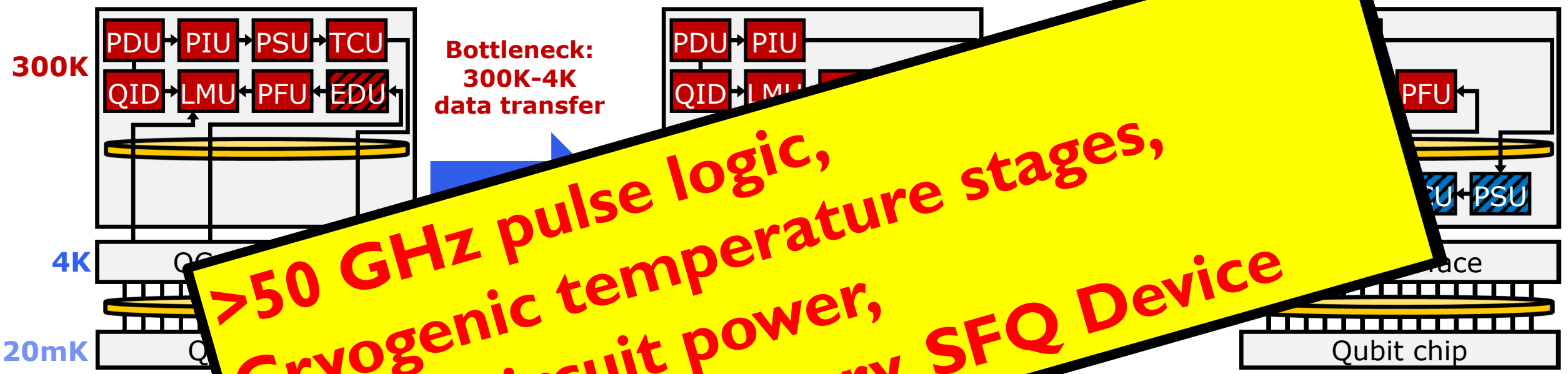
XQ-simulator: Overview

- **Run simulation to report scalability metrics and manageable qubit scale**
- **Integrate a quantum simulator for the functionally correct simulation**



Ilkwon Byun, et al., "XQsim: Modeling Cross-Technology Control Processors for 10+K Qubit Quantum Computers," ISCA, June 2022.

10+K qubit QCP design: Summary

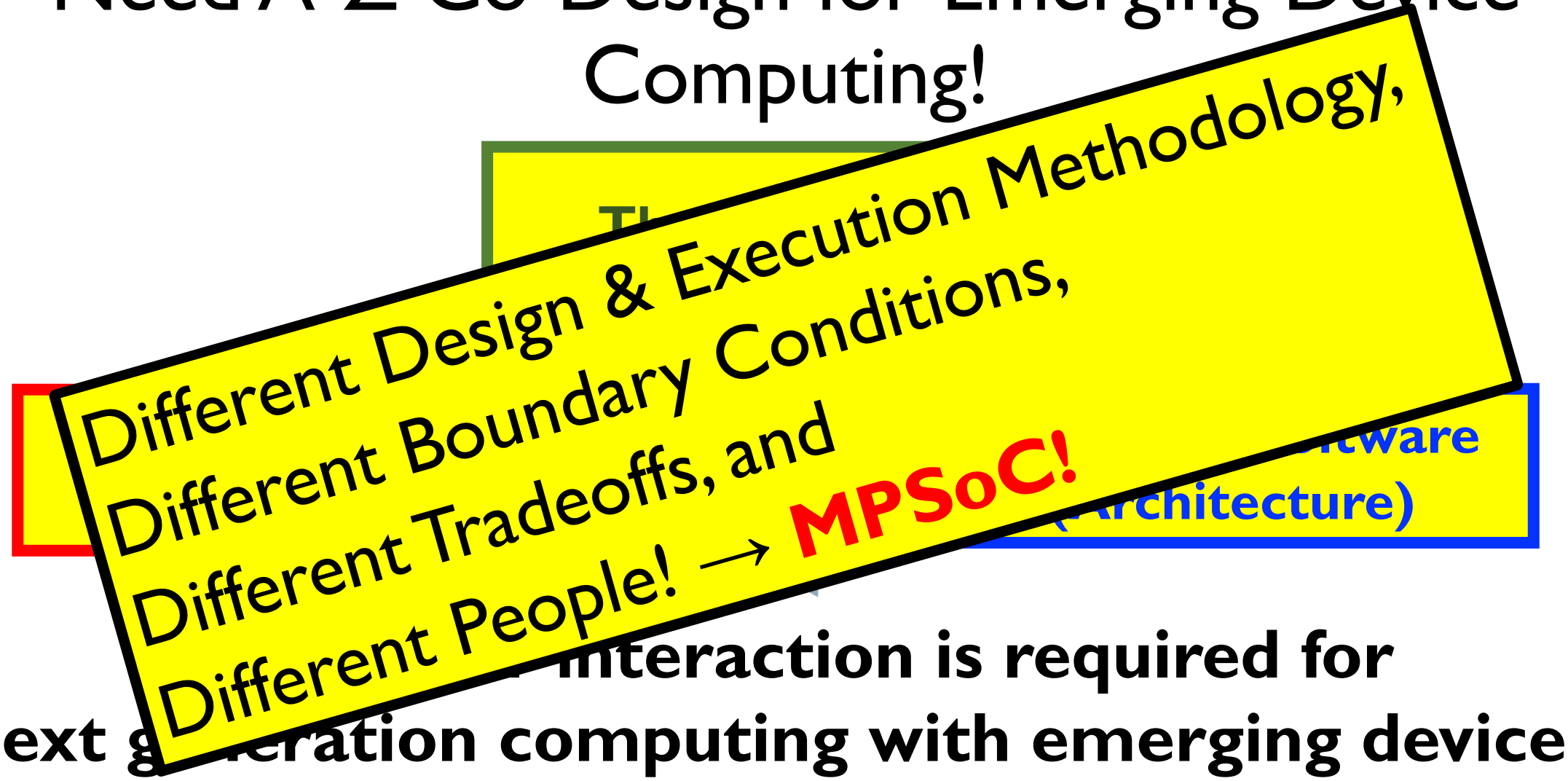


>50 GHz pulse logic,
Cryogenic temperature stages,
Inflow/Circuit power,
Architecture, Theory, SFQ Device

With thorough analyses using XQsim, we could provide directions for designing a 10+K qubit QCP using SFQ technology!

Message

Need A-Z Co-Design for Emerging Device Computing!



interaction is required for next g eration computing with emerging devices!