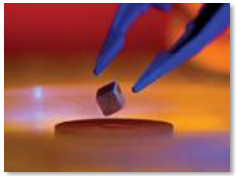

aqualab
EPFL
The Hardware of Quantum Computing
Edoardo Charbon
MPSoC'25
Megève, Jun 16th, 2025

Acknowledgements

Swiss National Science Foundation
European Commission, STW/NOW
Global Foundries, Canon, and many others.

A Bit of Background

Why Quantum Computing?



Energy
Room-temperature superconductivity

Health
Quantum chemistry

Internet Security

Source: L. Vandersypen, ISSCC 2017

Quantum Computing

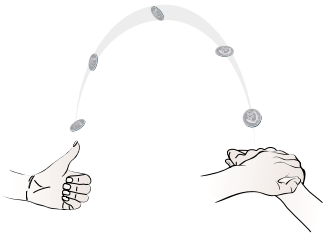
- Spearheaded by many, *in primis* Richard Feynman
- Proposal to use of **entanglement** and **superposition** for computation
- Fundamentals and theory developed in the 1980-2000

There is plenty of space at the bottom

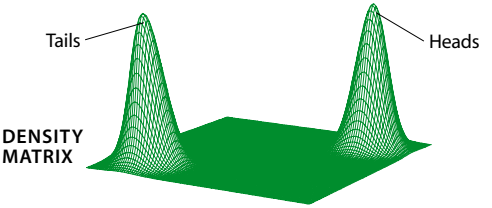
- Richard Feynman

Superposition

CLASSICAL UNCERTAINTY

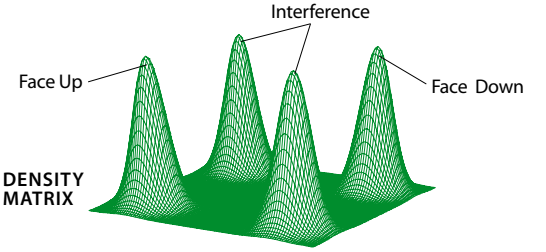


COIN TOSS



QUANTUM UNCERTAINTY

COHERENT SUPERPOSITION



M. Tegmark & J.A. Wheeler, 2001

The Power of Superposition

1 qubit.....2 states
2 qubits.....4 states

N qubits.....2^N states

40 qubits: 10^{12} parallel operations
300 qubits: more than the atoms in the universe

Entanglement

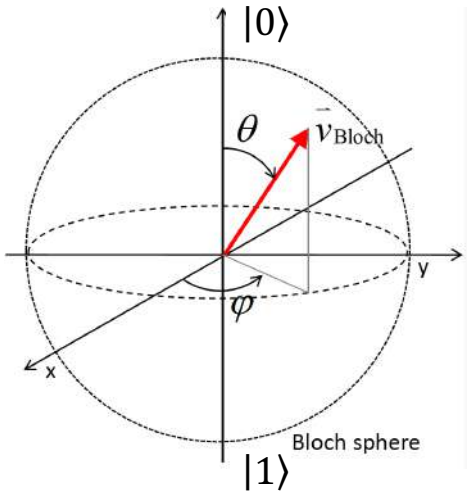
Definition: two particles are entangled if the quantum state of one particle cannot be described independently from the quantum state of the other particle.

Intuition: measuring the quantum state of one particle implies knowledge of the quantum state (e.g. momentum, spin, polarization, etc.) of the other entangled particle using the same projection.

The Qubit

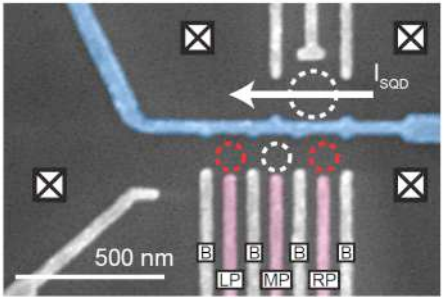
$$|\psi\rangle = \alpha_0|0\rangle + \alpha_1|1\rangle$$

α_0 , α_1 : complex numbers

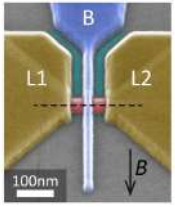


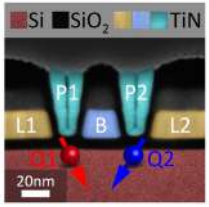
θ: polar angle
φ: azimuth
δ: global phase (ignored in the Bloch sphere)

Solid-State Qubits: Spin and Superconductive

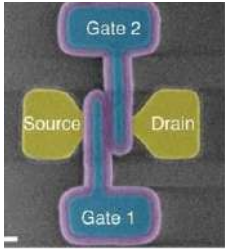


Semiconductor quantum dots (TU Delft / Vandersypen)

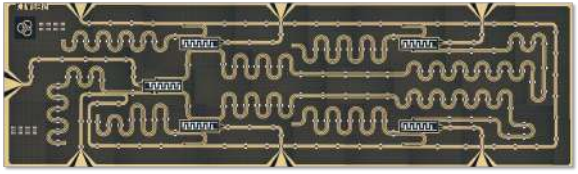




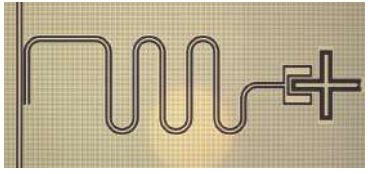
Si Hole-spin qubits (Uni Basel)



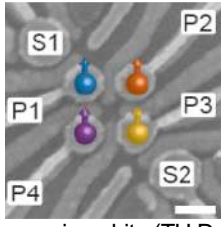
FD-SOI spin qubits (CEA-LETI)



Superconducting circuits (TU Delft / DiCarlo)



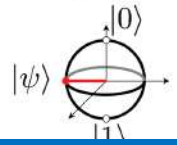
Superconducting qubit (EPFL)

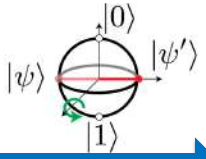


Ge e-spin qubits (TU Delft / Velthorst, Scappucci)

Classical vs. Quantum Computing: 1 (Qu)bit

	Information	Processing	Extract Information
Classical	Bit "0" or "1"	Boolean Logic D Q D Q 1 0	Deterministic Bit "0" or "1"
Quantum	Qubit (Quantum state) $\|\psi\rangle = \alpha_0 \|0\rangle + \alpha_1 \|1\rangle$	Unitary Transform (Rotation) $\|\psi'\rangle = \underbrace{\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}}_{\hat{U}} \underbrace{\begin{bmatrix} \alpha_0 \\ \alpha_1 \end{bmatrix}}_{\|\psi\rangle}$	Probabilistic State Collapse $\|\alpha_0\|^2 \to \|0\rangle$ $\|\psi\rangle$ or $\|\alpha_1\|^2 \to \|1\rangle$





DETERMINISTIC

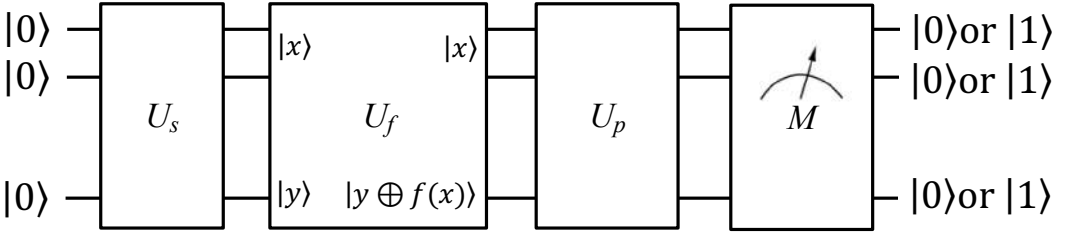
DETERMINISTIC

PROBABILISTIC

Courtesy: Joseph Bardin, ISSCC 2022

Multi-qubit Quantum Algorithm

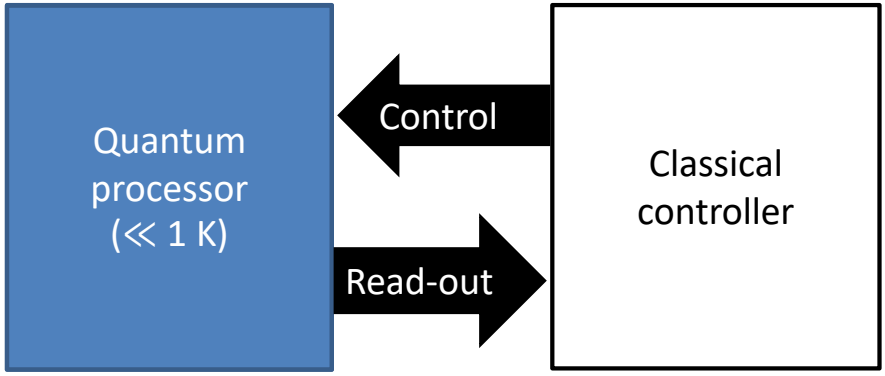
- Initialize qubits
- Create superposition
- Encode function in unitary
- Process
- Measure



Maintain quantum coherence

The Role of Cryogenic Electronics

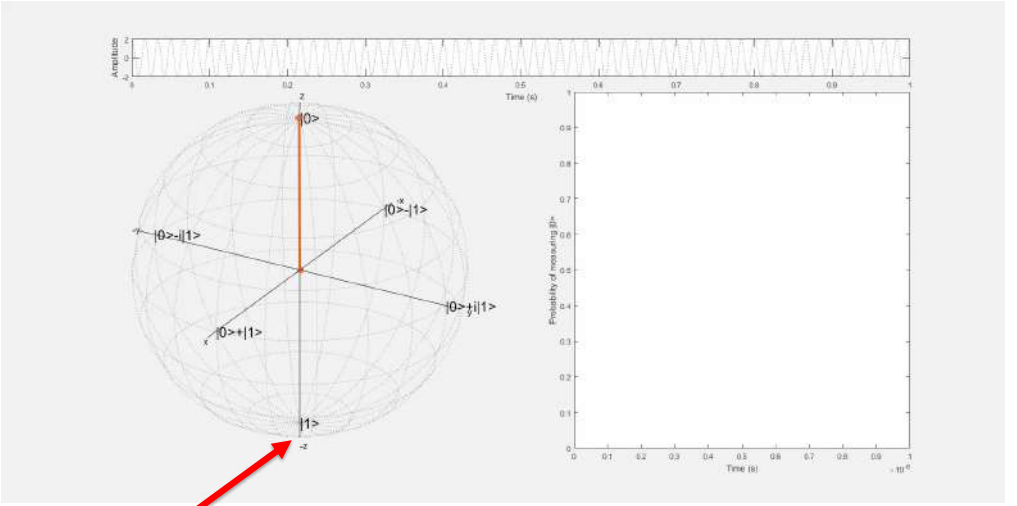
Interfacing Qubits with the Classical World



- Carrier frequency: 2 – 20 GHz
- Pulses: 10 – 100 ns
- Readout techniques for spin qubits: **ESR, EDSR**

ESR: Electron spin resonance – EDSR: Electric dipole spin resonance

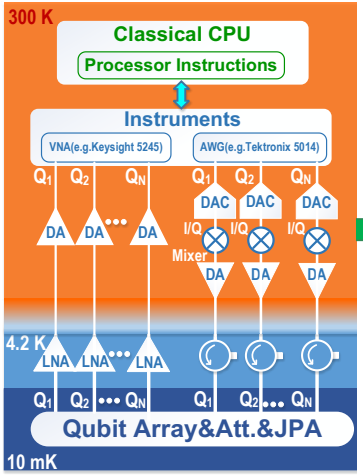
Qubit Transition from $|0\rangle$ to $|1\rangle$

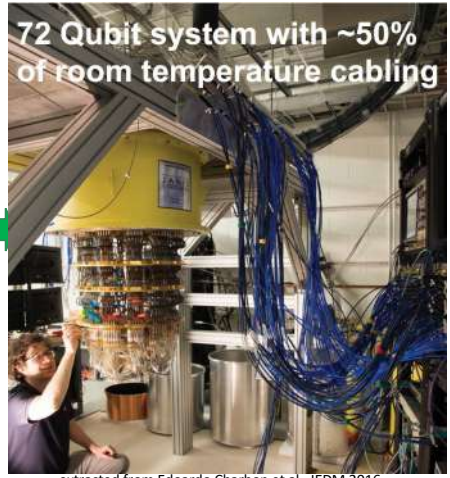


Fidelity

© Jeroen van Dijk

Moving Qubit Interface to 4K

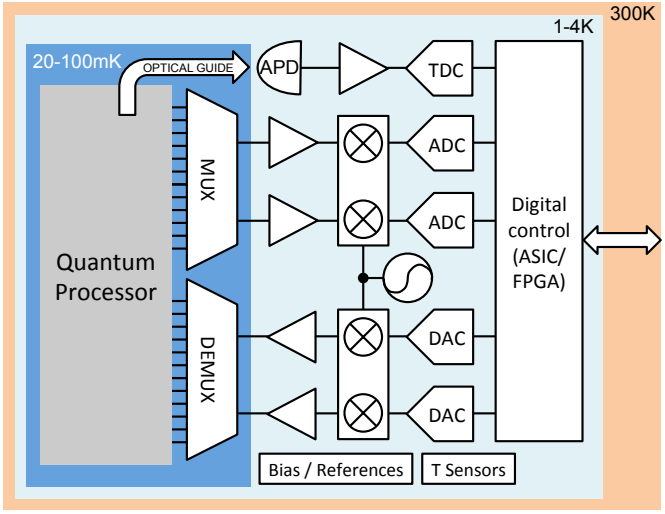




extracted from Edoardo Charbon et al., IEDM 2016

- Compact
- Low latency
- Scalable

Cryo-CMOS SOC for Interfacing Qubits



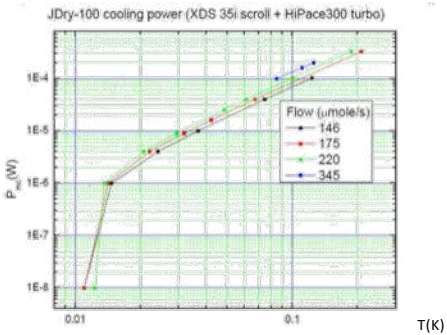
E. Charbon *et al.*, *IEDM* 2016

The Right Technology

Device	Lowest useable temperature	Limit
Si BJT	100 K	Low gain
Ge BJT	20 K	Carrier freeze-out
SiGe HBT	4 K (or lower)	
Si JFET	40 K	Carrier freeze-out
III-V MESFET	4K (or lower)	Lower freeze-out?
CMOS (>160nm)	4 K	Non-idealities
CMOS (<40nm)	40 mK	Power dissipation

Most used

Cooling Power Issue



Dilution refrigerator

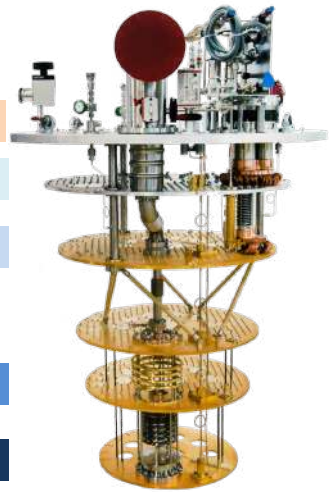
300 K

70 K

4 K

100 mK

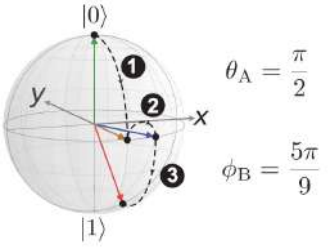
20 mK



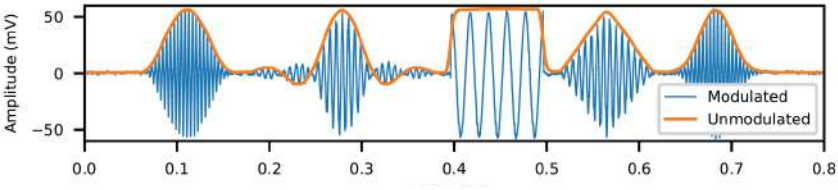
Courtesy: Oxford instruments

Designing Cryogenic *Scalable* Systems

Qubit Control in a Nutshell



J. Bardin et al., BCICTS 2024

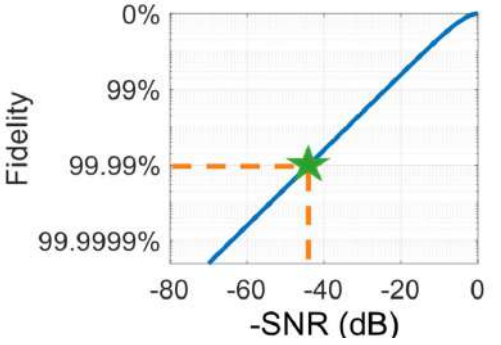


J. van Dijk et al., *JSSC* 2020

- The qubit control pulse (amplitude and phase) should be well defined.
- The Spurious-Free Dynamic range (**SFDR**) should be maximized.
- Fidelity is key

From Qubit Fidelity to Electrical Specs

- State-of-the-art spin qubits: fidelity < 99.9%
- Target: 99.99% (four 9's)
  - This translates to a SNR > 44 dB for a bandwidth of 25 MHz

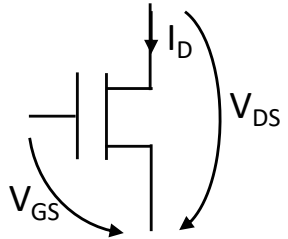


J. v.Dijk et al., *PRA* 2019

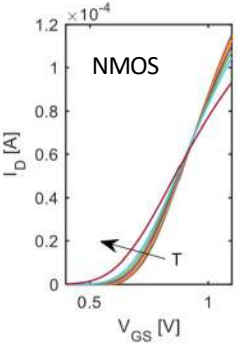
Scalability Issue

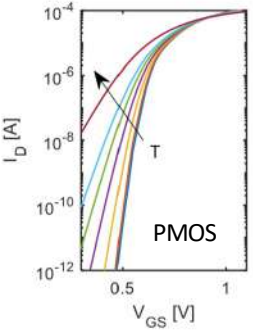
- Noise budget…….< 0.1nV/√Hz
- Power budget (for scalability)……. << 2mW/qubit
- Physical dimensions (for scalability)……. 30nm
- Bandwidth (for multiplexing)……. 1-12GHz
- Kick-back avoidance

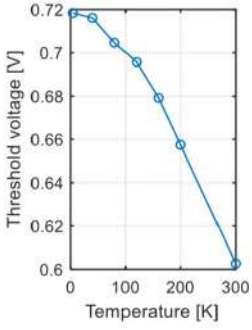
Cryogenic Effects

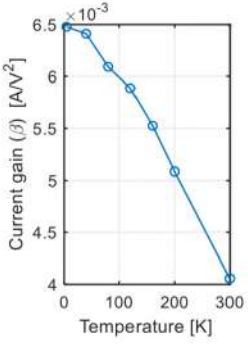


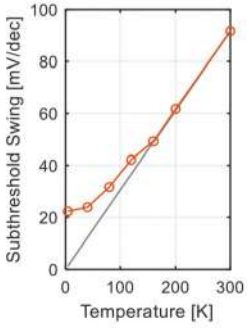
- Mismatch increases
- Leakage drastically reduces
- Substrate become floating







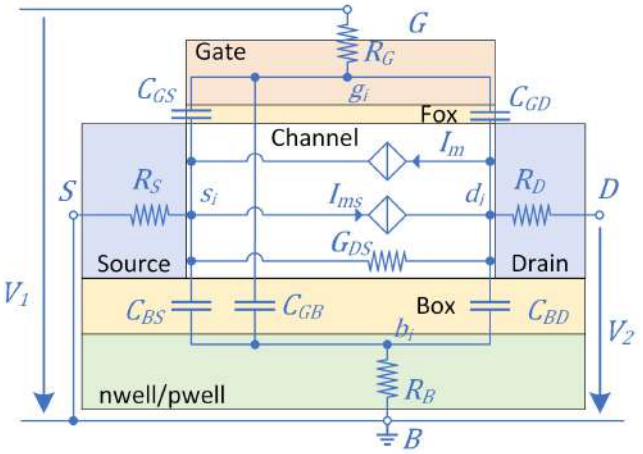




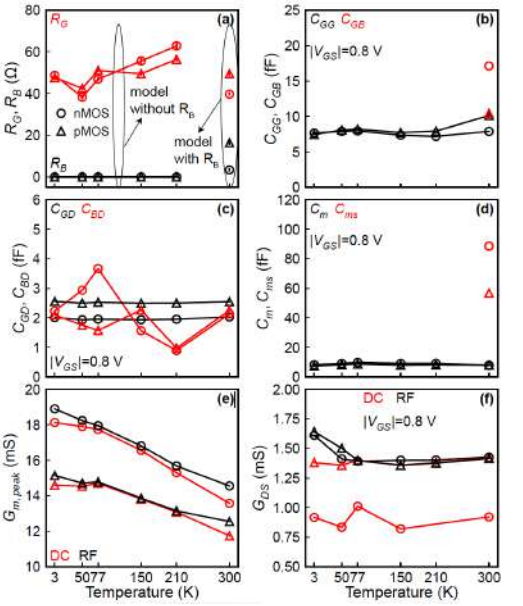
Extensive Modeling Campaigns

- CMOS 0.16µm STMicroelectronics
- CMOS 40nm TSMC
- CMOS 28nm STMicroelectronics bulk/FDSOI
- CMOS 22nm FDSOI Global Foundries
- CMOS 16nm FinFET TSMC

RF Modeling of CMOS 22nm FDSOI

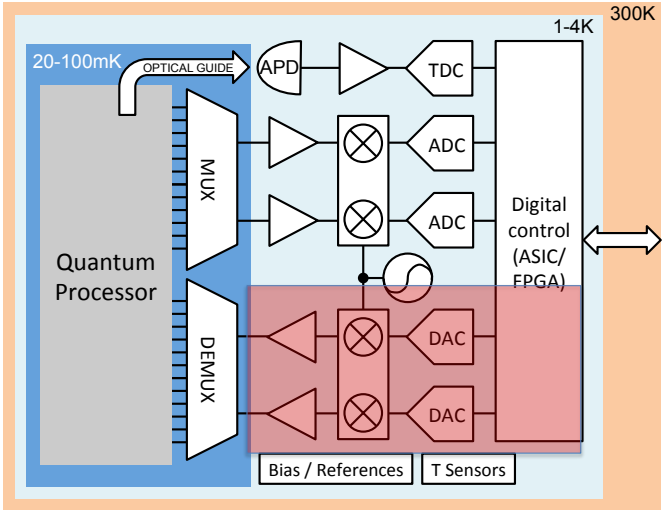


H.C. Han et al., *ESSDERC* 2022



Qubit Controller Design:
The Brévine Chip

Qubit Controller Design



E. Charbon *et al.*, *IEDM* 2016

High-level Specifications

- Target fidelity: 99.9% for 1…10 MHz operation

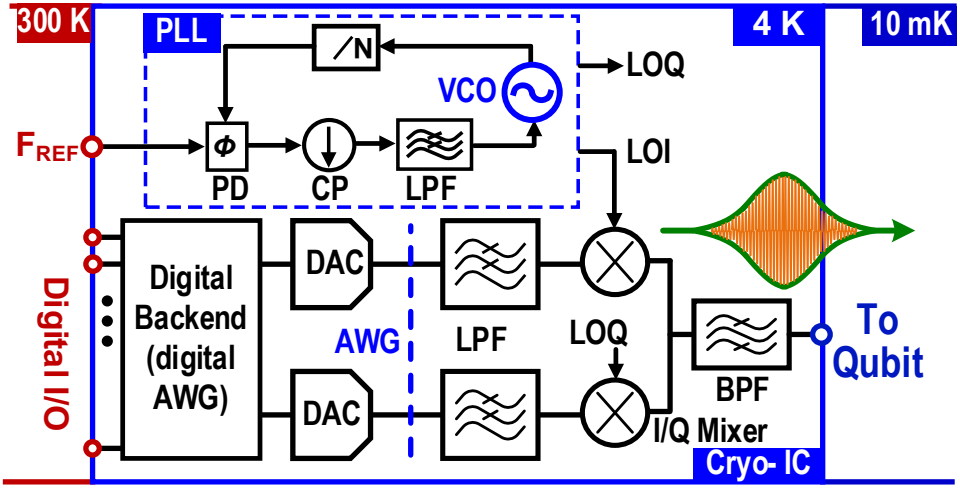
	Value	Infidelity contribution to an operation	to idling
Frequency			
nominal	10 GHz	0.64×10^{-9} [a]	
spacing	1 GHz		1×10^{-6} [b]
inaccuracy	11 kHz	125×10^{-6}	308×10^{-6}
oscillator noise	11 kHz$_{rms}$	125×10^{-6}	308×10^{-6}
nuclear spin noise	1.9 kHz$_{rms}$ [c]	3.6×10^{-6}	8.9×10^{-6}
wideband noise	12 µV$_{rms}$	125×10^{-6}	
Phase			
inaccuracy	0.64°	125×10^{-6}	31×10^{-6} [d]
Amplitude			
nominal	2 mV		
inaccuracy	14 µV	125×10^{-6}	
noise	14 µV$_{rms}$	125×10^{-6}	
off-spur	19 µV [e]		217×10^{-6}
off-noise	10 µV$_{rms}$		125×10^{-6}
Duration			
nominal	500 ns		
inaccuracy	3.6 ns	125×10^{-6}	
noise	3.6 ns$_{rms}$	125×10^{-6}	
		$F_{XY} = 99.9\,\%$	$F_I = 99.9\,\%$

Noise source	ENBW	Noise level
Frequency noise	2.5 MHz	$\mathcal{L}(1\,\text{MHz}) = -106\,\text{dBc/Hz}$
Wideband additive noise	2.9 MHz	$7.1\,\text{nV}/\sqrt{\text{Hz}}$
Amplitude noise	1.0 MHz	$14\,\text{nV}/\sqrt{\text{Hz}}$, SNR = −40 dB
Amplitude off-noise	2.0 MHz	$7.1\,\text{nV}/\sqrt{\text{Hz}}$

[a] Due to the RWA.
[b] Due to leakage in FDMA-setup using rectangular envelopes.
[c] From [61], $T_2^* = 120\,\mu\text{s}$.
[d] FDMA Z-corrections limit the idling operation.
[e] Equivalent to −41 dBc.

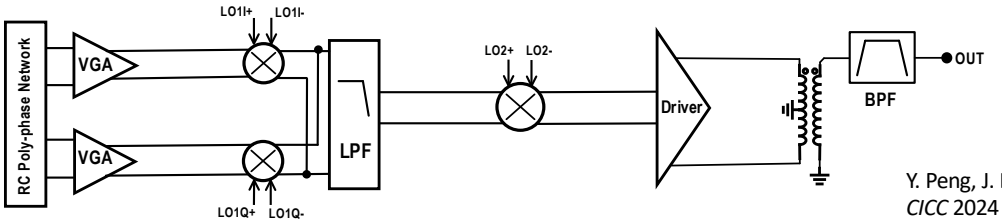
J. van Dijk, Thesis, 2021

The Design of Brévine



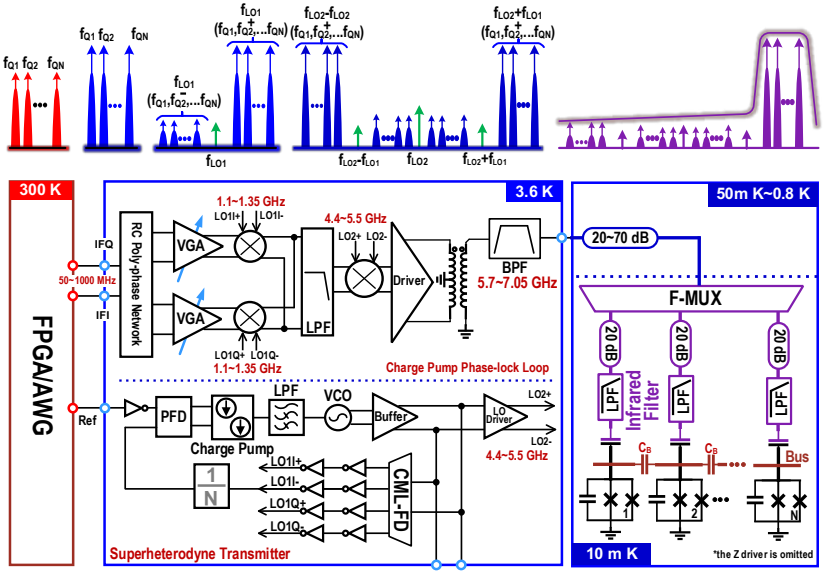
Y. Peng et al., CICC 2024

Brévine: IF Architecture



Y. Peng, J. Benserhir, *et al.*, *CICC* 2024

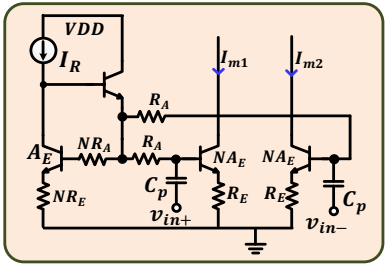
Brévine: Complete Architecture



Brévine: What Was Done Differently

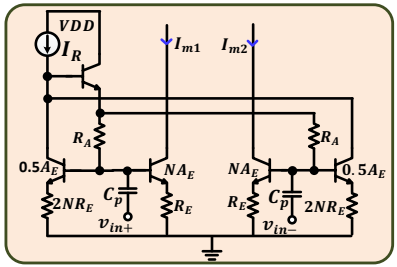
Highly Linear G_M Cell for 1st Stage Mixer

- **Classical G_M Cell**



- Pseudo-differential.
- Without linearity improvement.

- **Enhanced IIP2 G_M Cell**



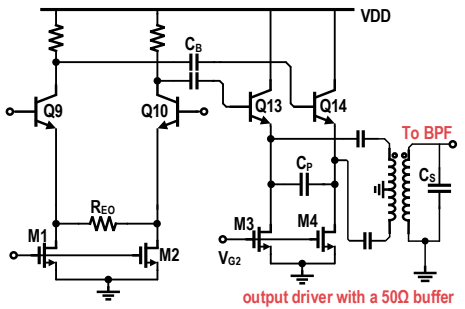
Pete Sivonen et al., TCAS-I 2005

- With 2nd order intermodulation cancellation.
- Without IIP3 improvement.

Enhanced IIP2 & IIP3

Y. Peng et al., CICC 2024

High-linearity Caprio's-quad Output Driver



- High linearity is required

Emitter Resistor Degeneration:

$$\Delta I = \frac{v_{in} + \Delta v_{BE}}{R_{E0}}$$

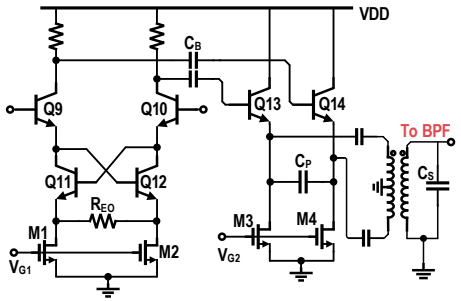
Δv_{BE}: base-emitter voltage difference of Q9 and Q10

- $v_{BE9} \neq v_{BE10}$ => ΔI vs v_{in} has imperfect linearity

- Technique widely used but ***moderate linearity***.

Y. Peng et al., CICC 2024

High-linearity Caprio's-quad Output Driver



- Caprio's Quad architecture is used.
- Cross-coupled pair Q3- Q4 is added.

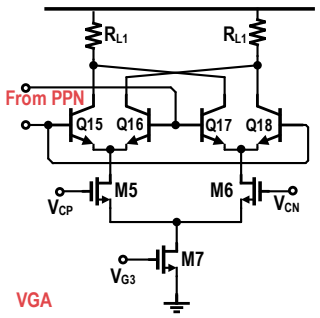
Emitter Resistor Degeneration:

$$\Delta I = \frac{v_{in} + (v_{BE,9} - v_{BE,11}) + (v_{BE,12} - v_{BE,10})}{R_{E0}}$$

- **Caprio's Quad is *very linear*.**
- Limited voltage input swing => **Low output is needed to drive the qubit**

Y. Peng et al., CICC 2024

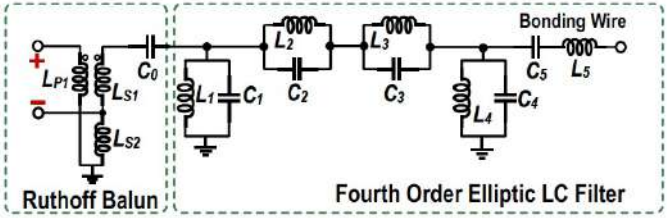
BiCMOS VGA

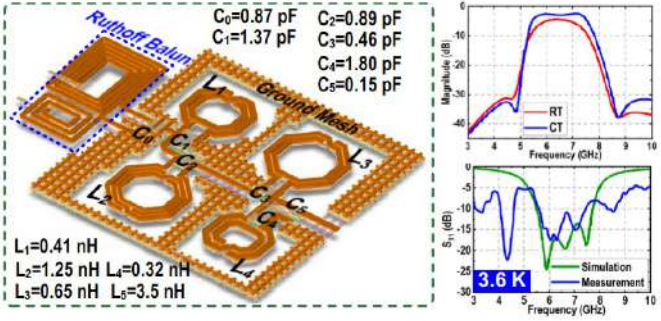


- Tune the output power to drive the qubit.
- HBTs compared to MOSFETs have:
  - **High transit frequency f_T** ↑
  - **High linearity** ↑
  - **Large transconductance g_m** ↑
  - **Large headroom => Static power consumption** ↑
- **M5, M6, M7** are implemented as MOSFETs.
- **Q15, Q16, Q17, Q18** are implemented as HBTs

Y. Peng et al., CICC 2024

Ruthoff Balun and Elliptic LC Filter



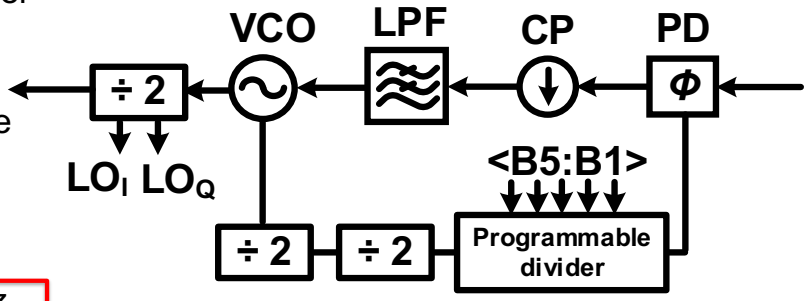


Y. Peng et al., CICC 2024

- Ruthoff Balun implemented on chip with better amplitude and phase balance in the operating band
- Elliptic LC BPF filter achieved excellent out-of-band rejection

Frequency Synthesizer

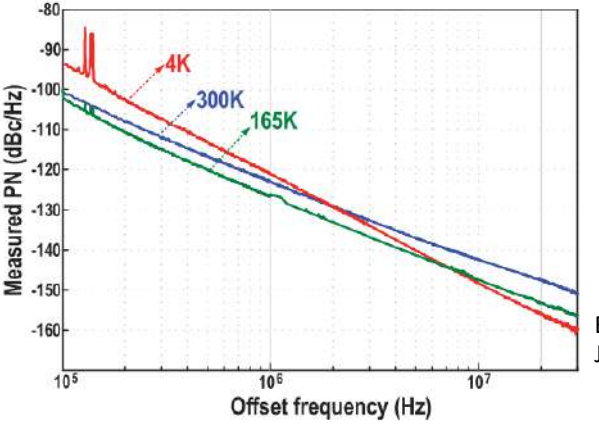
- Analog charge-pump integer-N phase-locked loop
- Programmable divider to ensure locking range to the reference clock
- VCO: Hybrid Class B/C Mode-Switching VCO
- Carrier frequency: 6.6 GHz (for SC qubits) – 2-40 GHz (for spin qubits)
- PN < -115 dBc/Hz @ 1MHz



A. Ruffino et al., ISSCC 2021
Y. Peng et al., JSSC 2022

Design Challenges

- Flicker noise at cryogenic temperature increases 10x due to higher active trap density at SiO_2-Si interface
- Flicker noise corner of CMOS-based VCO 1~5 MHz at 4.2K.



B. Patra et al., IEEE JSSC'2018

Hybrid Class B/C Mode-switching VCO

- Class C VCO

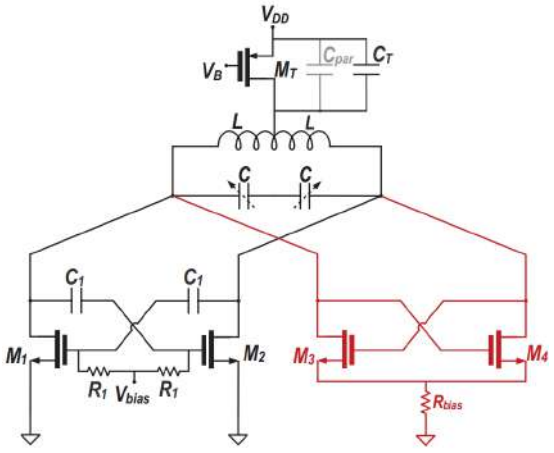
→ Better current efficiency for HBT-based VCO

- Hybrid Class B/C operation

→ No extra start-up circuits: save power

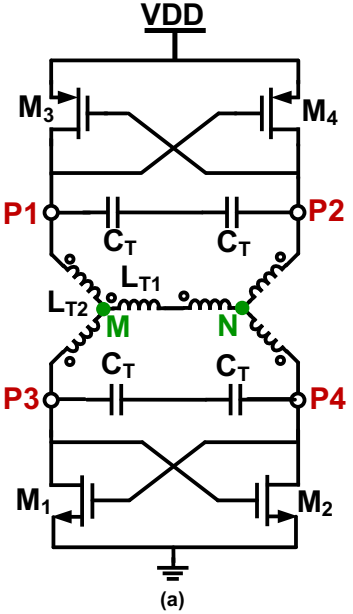
- 2 independent VCOs coupled

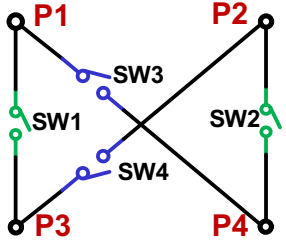
→ Better phase noise

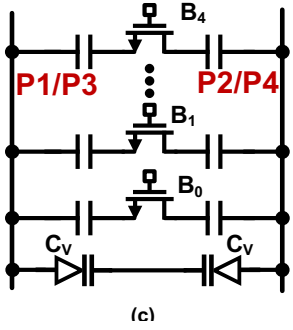


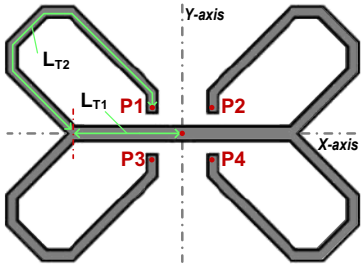
Fanori et al., ISSCC 2012

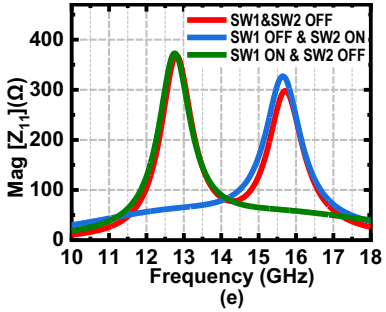
Hybrid Class B/C Mode-switching VCO







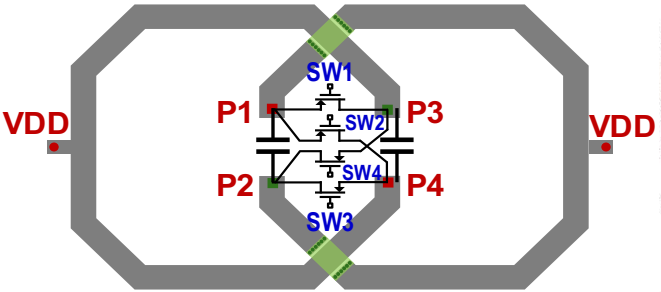




Y. Peng et al., ISSCC 2022

Dual-mode Tank Design

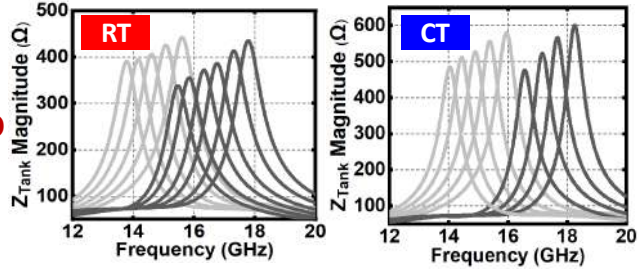
Switches Design

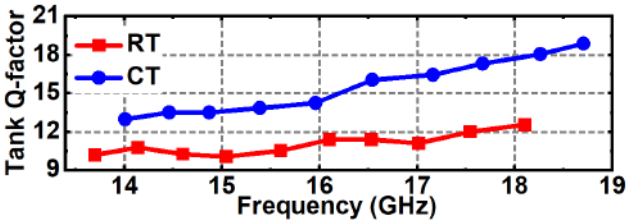


$$R_{on,max} \approx \frac{R_T}{2Q_T}\frac{\omega_0}{\Delta\omega_M}$$

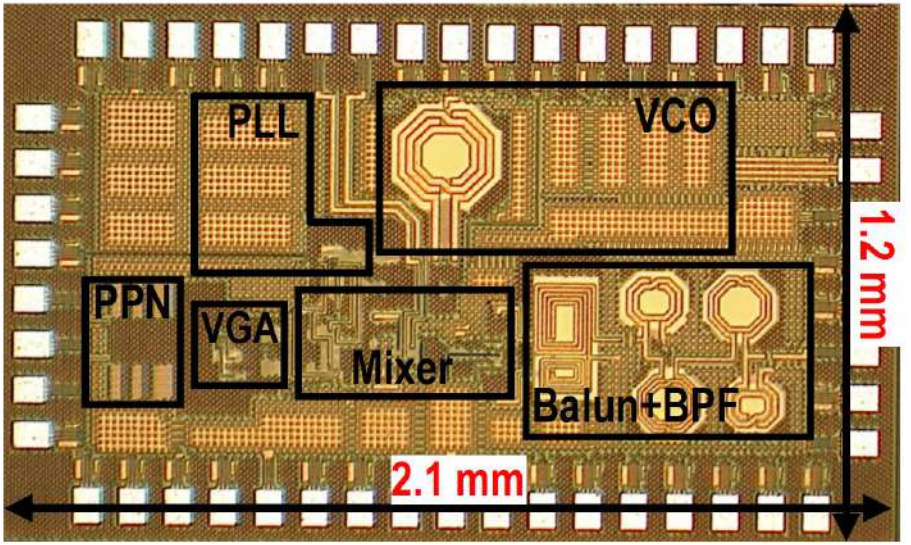
SW1~SW4: 12 μm/R_{on}~150 Ω

Q-factors of LC-tank at CT



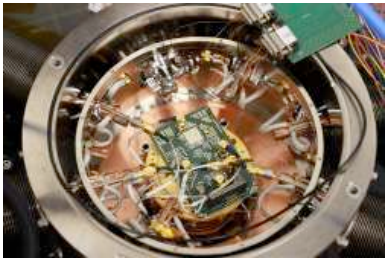


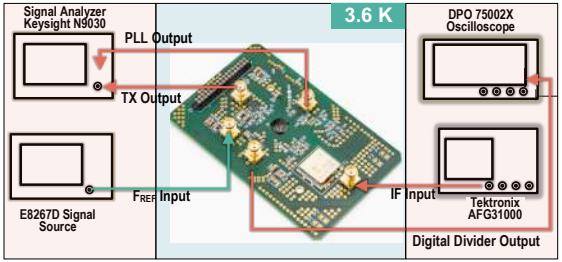
The Brévine Chip



Y. Peng et al., CICC 2024

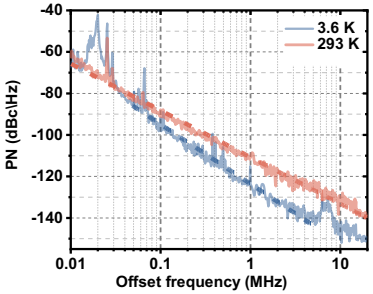
Measurement Setup

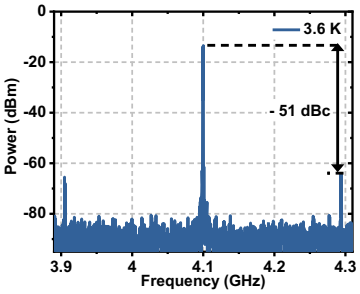




- The Lakeshore probe station is modified to support the measurements
- Phosphor bronze wires are used for DC connections

VCO Characterization: Phase Noise

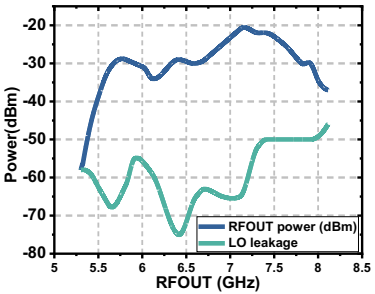


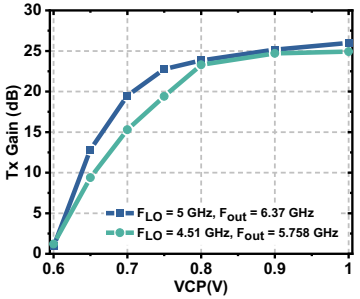


- At **239 K**: PN is **-110 dBc/Hz @ 1 MHz** offset from the **4.1 GHz** carrier
- At **3.6 K** : PN is **-127 dBc/Hz @ 1 MHz** offset from the **4.1 GHz** carrier

Y. Peng et al., CICC 2024

Controller Characterization: Output Power

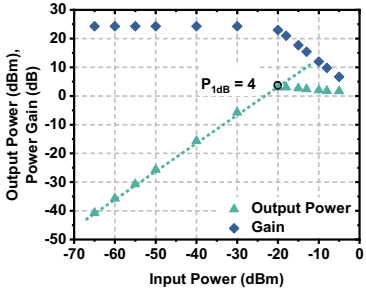


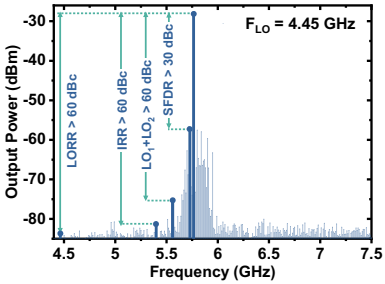


- **Output power: -40 dBm < P_{out} < -20 dBm**
- **LO leakage. : -75 dBm < $P_{leakage}$ < -50 dBm**
- **Tunable** controller gain: **0** to **30 dB**

Y. Peng et al., CICC 2024

Controller Characterization: Linearity

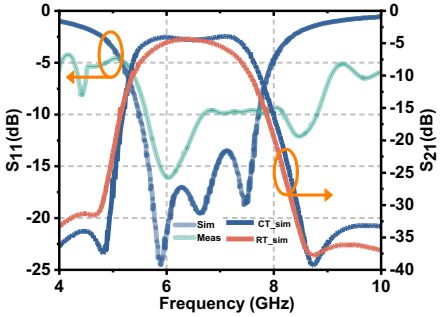




- **Good linearity : P1dB = 4 dBm** at **3.6 K**
- At **3.6 K** : **SFDR** = **30.8 dBc**, IMD3 > **30 dBc**, IRR > **53 dBc**, LORR > **60 dBc**

Y. Peng et al., CICC 2024

Controller Characterization: Bandpass Filter



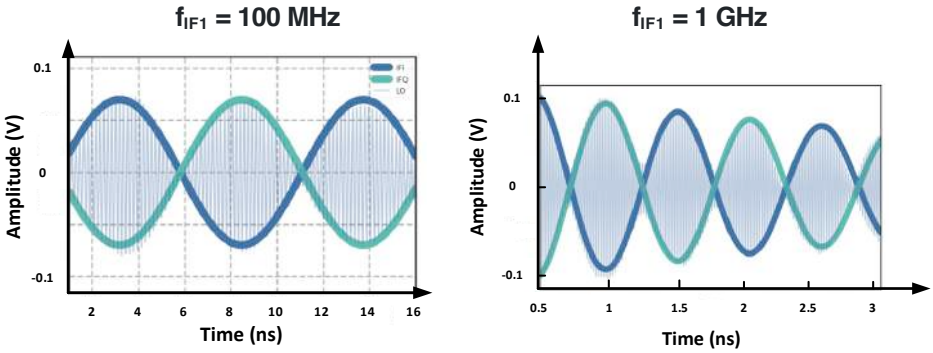
- At CTs, Q-factor of an inductor is enhanced.
- **On-chip** BPF replaces coaxial filter block.

> 30 dB out-of-band suppression

3 dB in-band insertion loss

Y. Peng et al., CICC 2024

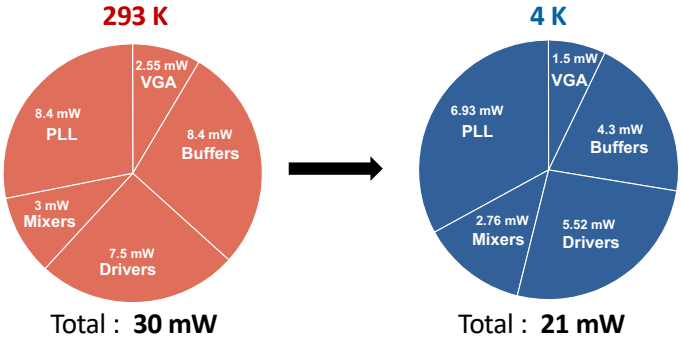
Controller Characterization: Time Domain



- Time Domain output waveforms at T = 3.4 K
- Wide range of IF can be used

Y. Peng et al., CICC 2024

Controller Characterization: Power



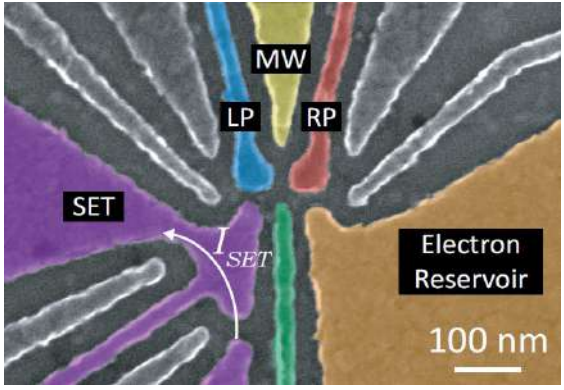
- Power consumption limited by the **PLL**, **buffers** and **drivers**.
- The **PLL** can be **shared** among multiple qubit channels.

Y. Peng et al., CICC 2024

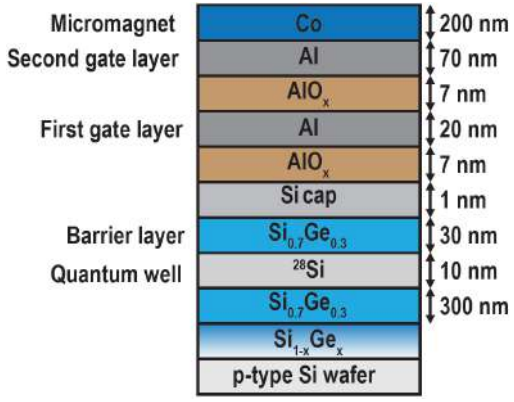
Qubit Device in Experiments

- Two-qubit processor – control done using Horse Ridge chip

Top-view

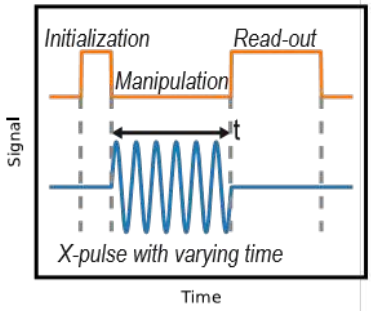


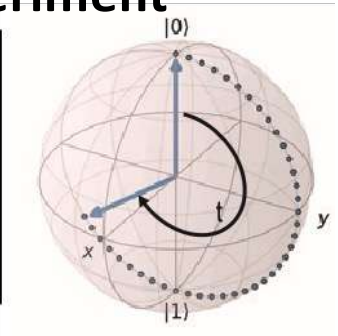
Cross-section view



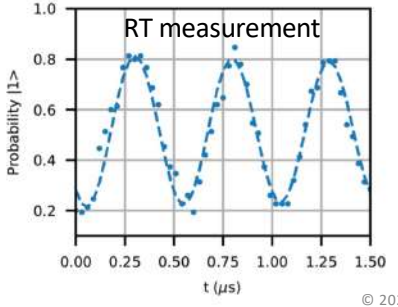
X.Xue, B. Patra, arXiv, 2020

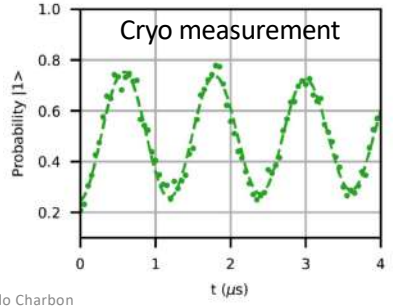
Rabi Experiment



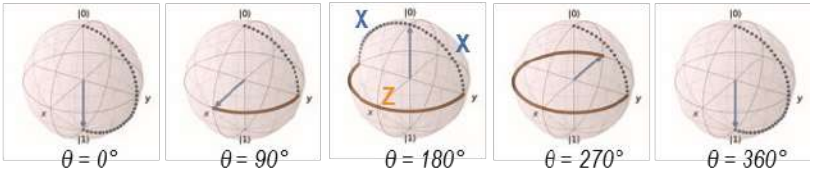


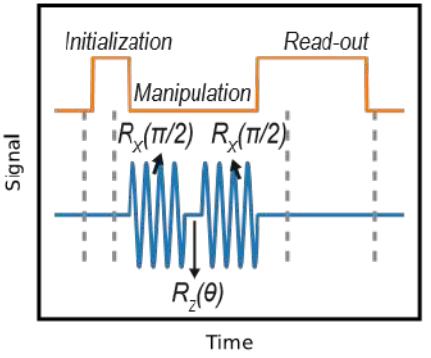
B. Patra, J.v.Dijk *et al.*, *ISSCC* 2020, *JSSC* 2020

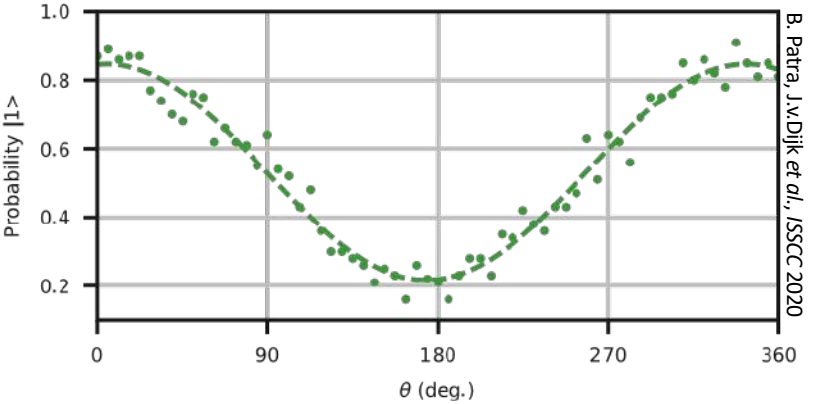




Ramsey Experiment

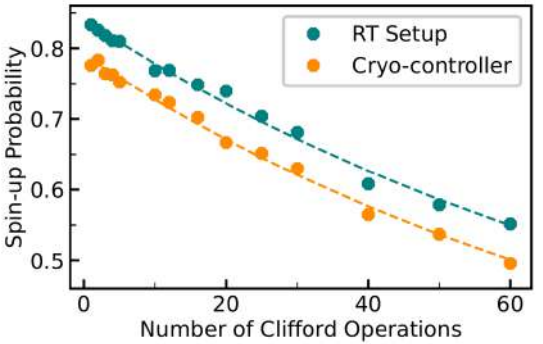






Randomized Benchmarking

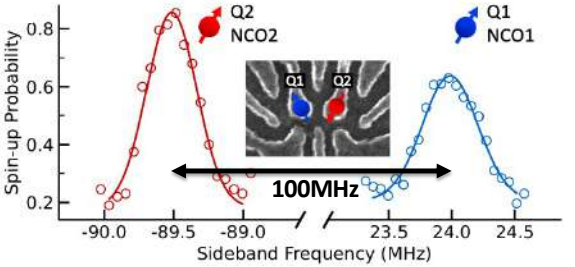
- Up to 60 Clifford gates: Each Clifford gate is averaged over 32 different randomized sequences
- Consistently repeatable: Fidelity limited by qubit sample

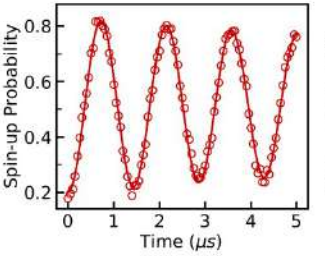


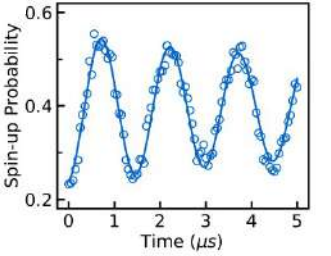
Fidelity = 99.71±0.03%

Fidelity = 99.69±0.02%

Simultaneous Rabi Oscillations by Way of FDMA

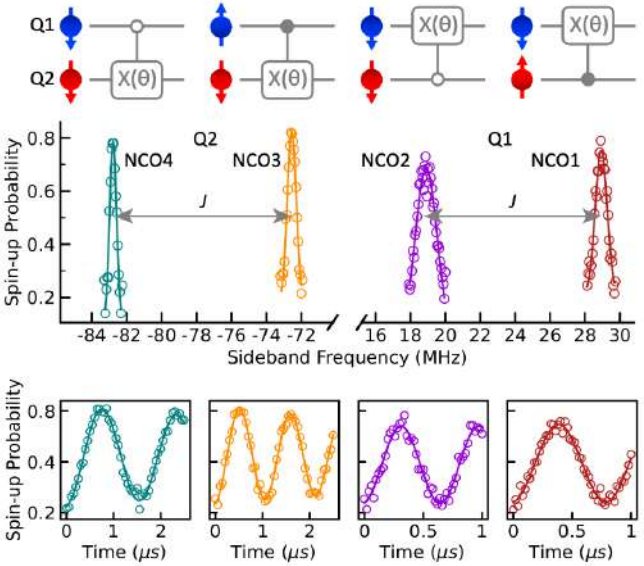






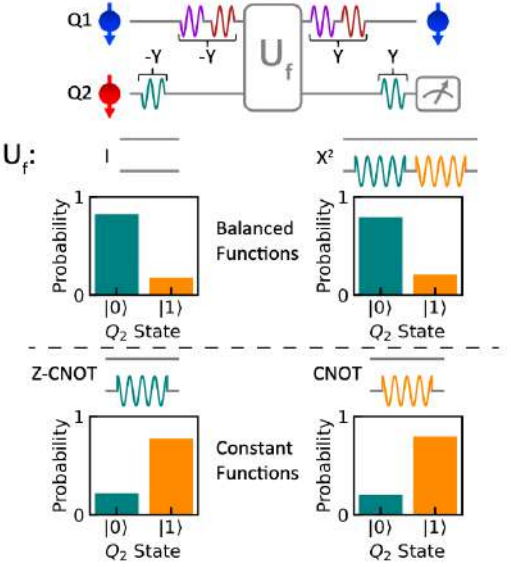
X. Xue *et al.*, *Nature* 593 (2021)

2-Qubit Gate



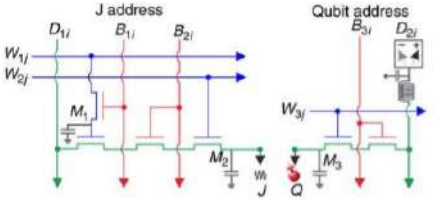
X. Xue *et al.*, *Nature* 593 (2021)

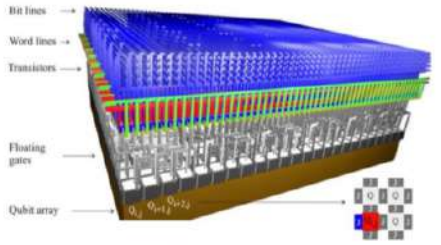
Deutsch-Jozsa Algorithm



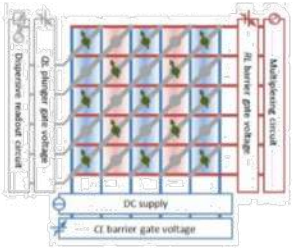
Perspectives: Beyond 100 Qubits

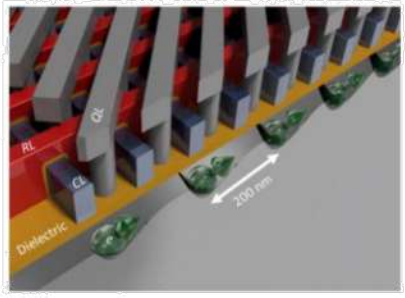
Proposals for Scalable 2D Qubit Arrangements





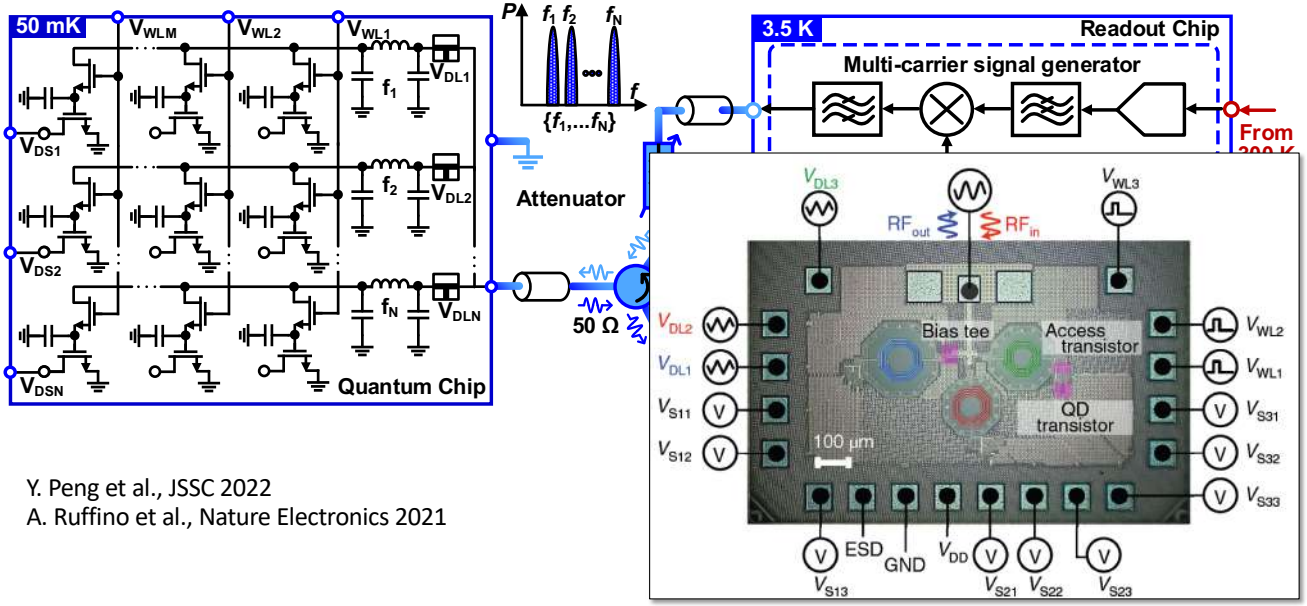
M. Veldhorst *et al.* *(UNSW), Nature Comm.* (2017)





R. Li et al., arXiv 1711.03807 (2017)

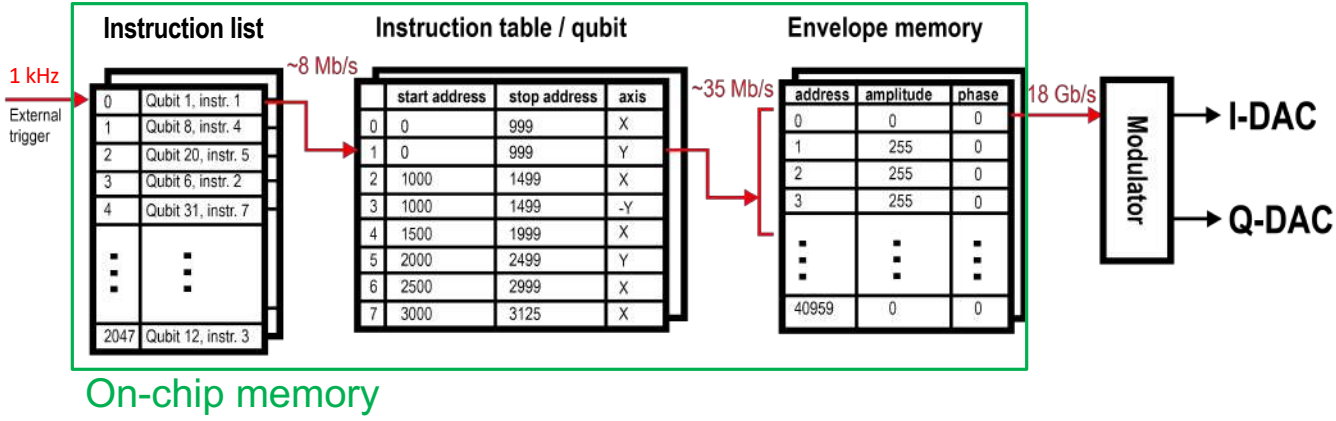
3x3 Qubit Readout



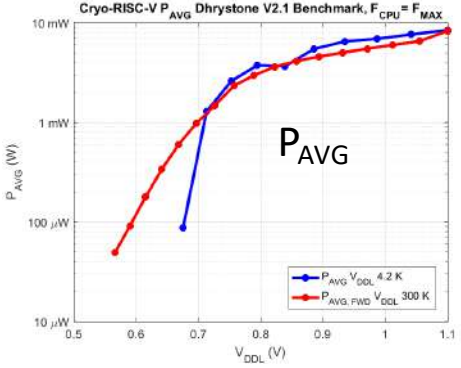
Y. Peng et al., JSSC 2022
A. Ruffino et al., Nature Electronics 2021

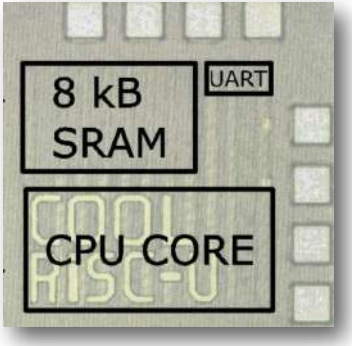
Instruction Set Memory

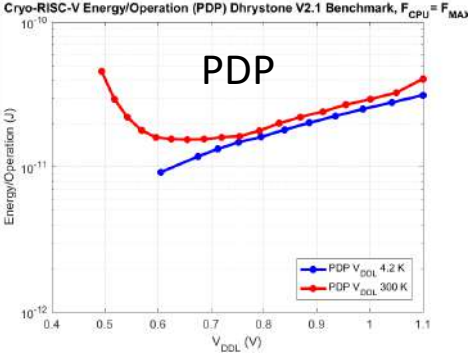
- No high-speed connection required during quantum algorithm execution



Open-Source Components

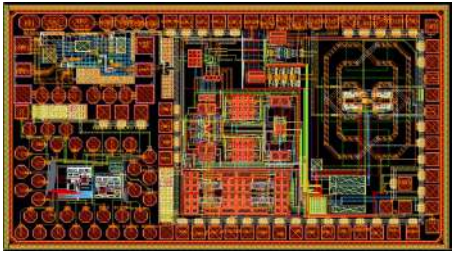




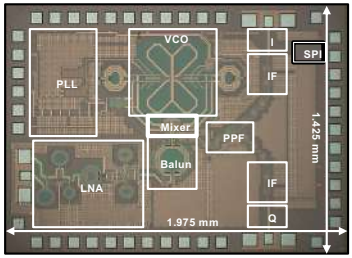


- Risc-V running at 4K
- Pavg and Power-dalay-product

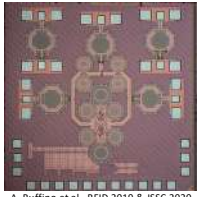
aqualab Quantum Designs



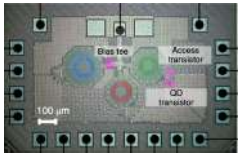
Y. Zou, J. Benserhir, V. Pesic, Y. Peng, December 2023



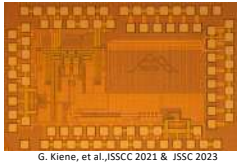
A. Ruffino et al., ISSCC 2021 – Y. Peng et al., JSSC 2022



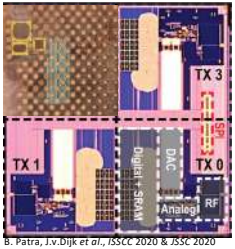
A. Ruffino et al., RFID 2019 & JSSC 2020



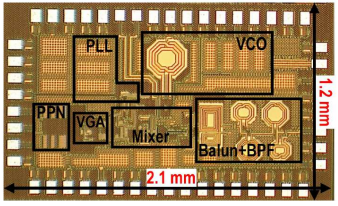
A. Ruffino et al., Nature El. 2020



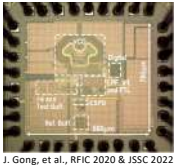
G. Kiene, et al.,ISSCC 2021 & JSSC 2023



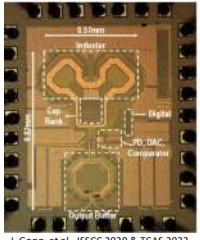
B. Patra, J.v.Dijk *et al., ISSCC 2020 & JSSC 2020*
X. Xue et al., Nature 2021; Pellerano et al., CICC 2022



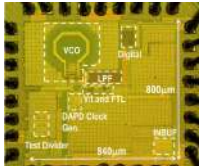
Y. Peng et al. CICC 2024



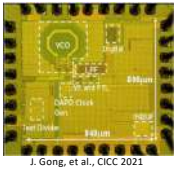
J. Gong, et al., RFIC 2020 & JSSC 2022



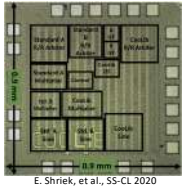
J. Gong, et al., ISSCC 2020 & TCAS 2022



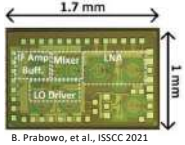
J. Gong, et al., ISSCC 2021 & JSSC 2023



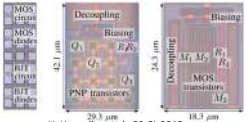
J. Gong, et al., CICC 2021



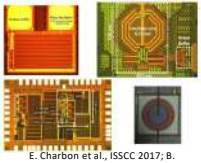
E. Shriek, et al., SS-CL 2020



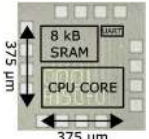
B. Prabowo, et al., ISSCC 2021



H. Homulle, et al., SS-CL 2018

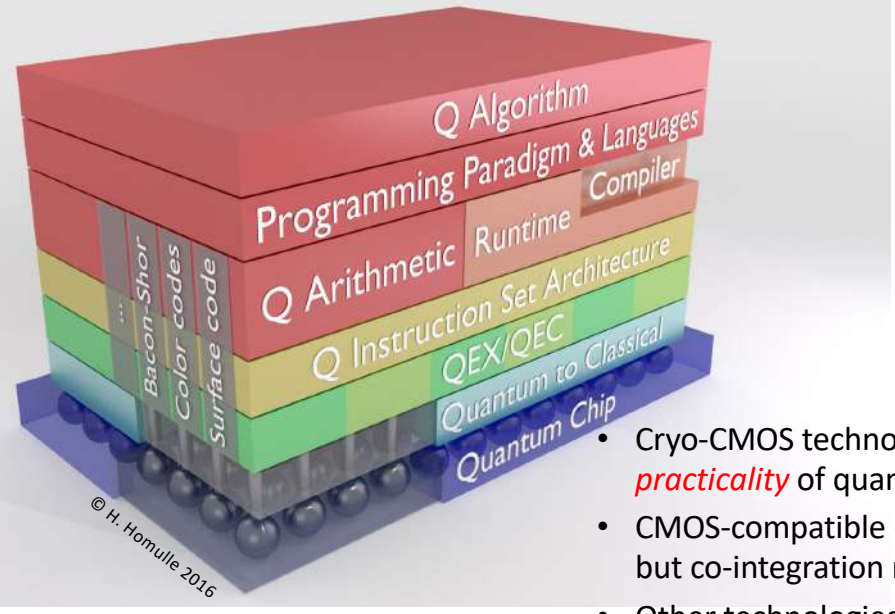


E. Charbon et al., ISSCC 2017; B. Patra et al., JSSC 2017



E. Shriek, et al., SS-CL 2020

Conclusions



- Cryo-CMOS technology is key to *scalability* and *practicality* of quantum computers
- CMOS-compatible qubits could emerge soon, but co-integration may be enough
- Other technologies like 3D integration and high-T qubits could be important enablers

Thank You

ISSCC 2023

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