MPSoC FORUM 2026 · KEYNOTE

Highly-Dependable Computing for Orbital Data Centers

An MPSoC FPGA-Centric Approach

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JAXA Space Strategic Fund — “Orbital Data Center Construction Technology”
Inn at Laurel Point, Victoria, British Columbia, Canada · June 22, 2026

SPACEBLAST DigitalBlast

SPEAKER

About the speaker

Kouichi Ono

Fellow, SPACEBLAST, Inc. / DigitalBlast, Inc.

Now (since 2026): Leading technology development for SpaceBlast's space-cloud business and orbital data centers — dependable computing platforms built on MPSoC FPGA hardware/software co-design, plus space-environment power & thermal management.

IBM Research – Tokyo (1994–2025): System-oriented research — embedded development support, program analysis, mobile agents, automated test generation. Technical lead on MFP and automotive ECU programs; built Model-Driven Systems Engineering (MDSE) for complex SoC-based products.

Selected background

- **Waseda University** Doctoral course, Electrical Eng. (Computer Eng.), 1994
- **Research Associate** Waseda Univ, 1990–1992
- **JSSST Board Member** 2003–2006
- **Adjunct Lecturer** Waseda (2003–2007), Kyushu Univ. (2009)
- **IPA / SEC WG** Embedded Systems WG; co-authored ESDR (2010–12)

AGENDA

What this talk covers

01 JAXA Space Strategy Fund

02 Why Orbital Data Center

03 Our Challenge: High-Dependability Technology for On-Orbit Data Computing

04 Radiation-resistant mechanisms

05 Heat control

06 Demonstration

01

FUNDING

JAXA Space Strategy Fund

PROJECT FUND

This project is funded by the Japanese government

宇宙戦略基金

JAXA (Japan Aerospace Exploration Agency)
Space Strategy Fund
https://fund.jaxa.jp/

Project Name:
Orbital Data Center Construction Technology
Program Funding Period:
Six years (April 2026 – March 2032)
Total Budget:
US $ 85 million (= Japanese ¥ 13.5 billion)
https://fund.jaxa.jp/content/uploads/kekka2_12.pdf

02

BACKGROUND

Why Orbital Data Center
Why On-Orbit Data Computing

CONTEXT

The orbital data center era is within sight

Launch costs are falling while onboard sensors and comms generate data faster than we can downlink it. Processing must move to where the data is — orbit.

Falling launch cost

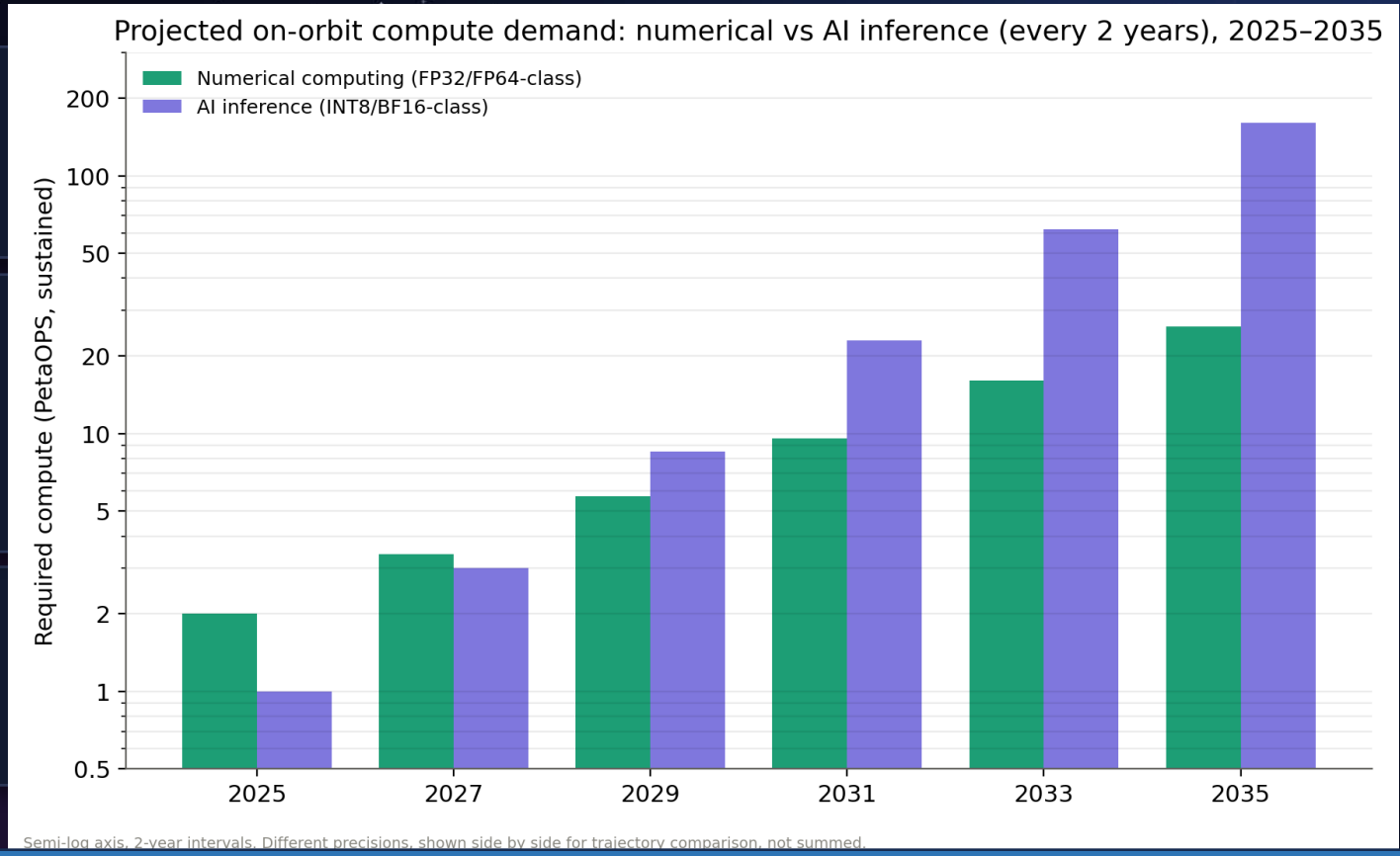
Reusable heavy-lift collapses $/kg — mass-to-orbit is no longer the binding constraint.

Sensor data explosion

Higher-resolution EO (Earth Observation), SAR (Synthetic Aperture Radar) and comms payloads outpace downlink bandwidth.

In-space AI demand

On-orbit inference, EO analytics and mission-critical workloads need compute in orbit.



1. Vertical axis is logarithmic
2. Comparing numerical computing to AI inference is meaningless, but the difference in growth rates is important

REFERENCES

Referred for estimating on-orbit data computing demand

Tha graph in the previous page is generated based on the estimation of on-orbit data computing demand based on the following data sources:

- Epoch AI, Trends in Machine Learning compute / Training compute: https://epochai.org/trends
- OpenAI, AI and Compute (2018): https://openai.com/research/ai-and-compute
- TOP500 / Green500: https://top500.org/ , https://top500.org/lists/green500/
- IEEE IRDS: https://irds.ieee.org/
- SemiAnalysis / McKinsey: https://www.semianalysis.com/ , https://www.mckinsey.com/
- ESA Φ-sat-1 / Φ-sat-2: https://www.esa.int/
- ESA OPS-SAT: https://www.esa.int/Enabling_Support/Operations/OPS-SAT
- CCSDS: https://public.ccsds.org/
- Novaspace / Euroconsult, Analysys Mason: https://www.novaspace.com/ , https://www.analysysmason.com/

THE PROBLEM

Space breaks three assumptions of ground computing

1 Radiation

Charged particles flip bits and latch up circuits. At advanced nodes, soft errors are constant — not exceptional. And the accumulation of radiation dose degrades the semiconductor devices and causes hard errors.

2 No convection

In vacuum there is no air or water cooling. >99% of consumed power becomes heat. Heat conduction to the cold plate is only a temporary escape. The only way to dissipate heat is through thermal radiation from the radiator into space.

3 Intermittent link

For communication with LEO (Low Earth Orbit; attitude 100-2000km) satellites/ISS and ground center, contact windows are short and bandwidth is scarce. The system must keep running — and decide — on its own.

What the platform must deliver, simultaneously

- **High dependability**
- **Energy & heat efficiency**
- **Advanced autonomy**

No single device gives all three. The answer is an architecture — not a part.

THE PROBLEM

Scaling makes soft errors unavoidable — even for AI

As transistors shrink, the critical charge falls; advanced-node SRAM is the dependability weak point. Commercial GPGPUs/accelerators used as-is in orbit are unsafe.

Estimated SEU rate

1.2×10^{-7}

events / bit / day

7 nm SRAM, LEO 500 km / 51.6°
CRÈME96 AP8MAX, solar minimum

0.5 – 5 recognition errors / hour

for an image-recognition model held in SRAM

Parameters held in SRAM

ResNet-50	**~25.6 M**
Vision Transformer	**~86.0 M**

More stored bits → more cross-section for upsets. A single flipped weight can corrupt an inference and cascade into a service outage.

DESIGN CHOICE

Rad-hard (radiation-hardening) ASIC vs. COTS — a third way

Parts based on radiation-hardening by process (RHBP) are robust but expensive, fab-locked, and lag the leading node. Pure COTS is fast and dense but fragile. We propose architecture-level radiation-hardening by design (Architecture-level RHBD) instead.

- **Architecture-level RHBD** — OUR LAYER
  Silicon Heartbeat · full-stack dependability · autonomous control (Physical AI)
- **Rad-Hard by Design**
  Redundancy / lock-step · scrubbing / ECC on COTS SoCs
- **Rad-Hard by Process**
  Specialized fabs, materials & cells (SOI, etc.)
- **COTS components**
  Commercial off-the-shelf peripherals / discretes

The operating principle

Don’t avoid errors — accept them.

Ensure dependability through detection, isolation and self-repair, built from **logically-synthesizable circuits** that are independent of fab, materials and technology node.

- Not tied to a specific fab or node — rides the COTS roadmap
- Hardening lives in the FPGA fabric, re-synthesizable as nodes evolve
- The semiconductor itself becomes a radiation sensor

03

CHALLENGE

Our Challenge: High-Dependability Technology for On-Orbit Data Computing

Full-Stack approach for high-dependability

- High-dependability functions implemented in semiconductors using logically synthesizable circuits.
- Adoption of a software stack meeting functional safety standards of Automotive.
- System-wide monitoring and control via AI - AI orchestration.

- Not dependent on semiconductor materials or specialized circuits.
- Not dependent on specific fabs or technology nodes.
- Leverage widely available consumer technologies.

Technical and economic objections in dependability

- SOI technology is highly resilient to radiation effects, but there are no plans to apply it beyond the current leading-edge process nodes.
- Dependence on specific semiconductor processes or fabs significantly limits its medium-to-long-term usability.
- Certain materials and specialized circuits (analog, logic circuit cells) become extremely expensive, making their use impossible at a realistic price range.

CONCEPT

DIOS: Dependability Improvement Technology on Orbit Server System

Full-stack solution of Aggressively adopt high-dependability Hardware, Software and AI technology trends across multiple domains

●High-dependability Hardware

- High-dependability CPU: RISC-V HD (High Dependability)
- High-dependability AI Accelerator: AI Engine HD
- MP-SoC (Multi-Processor System on a Chip) configuration suitable for both application and real-time uses

●High-dependability Software

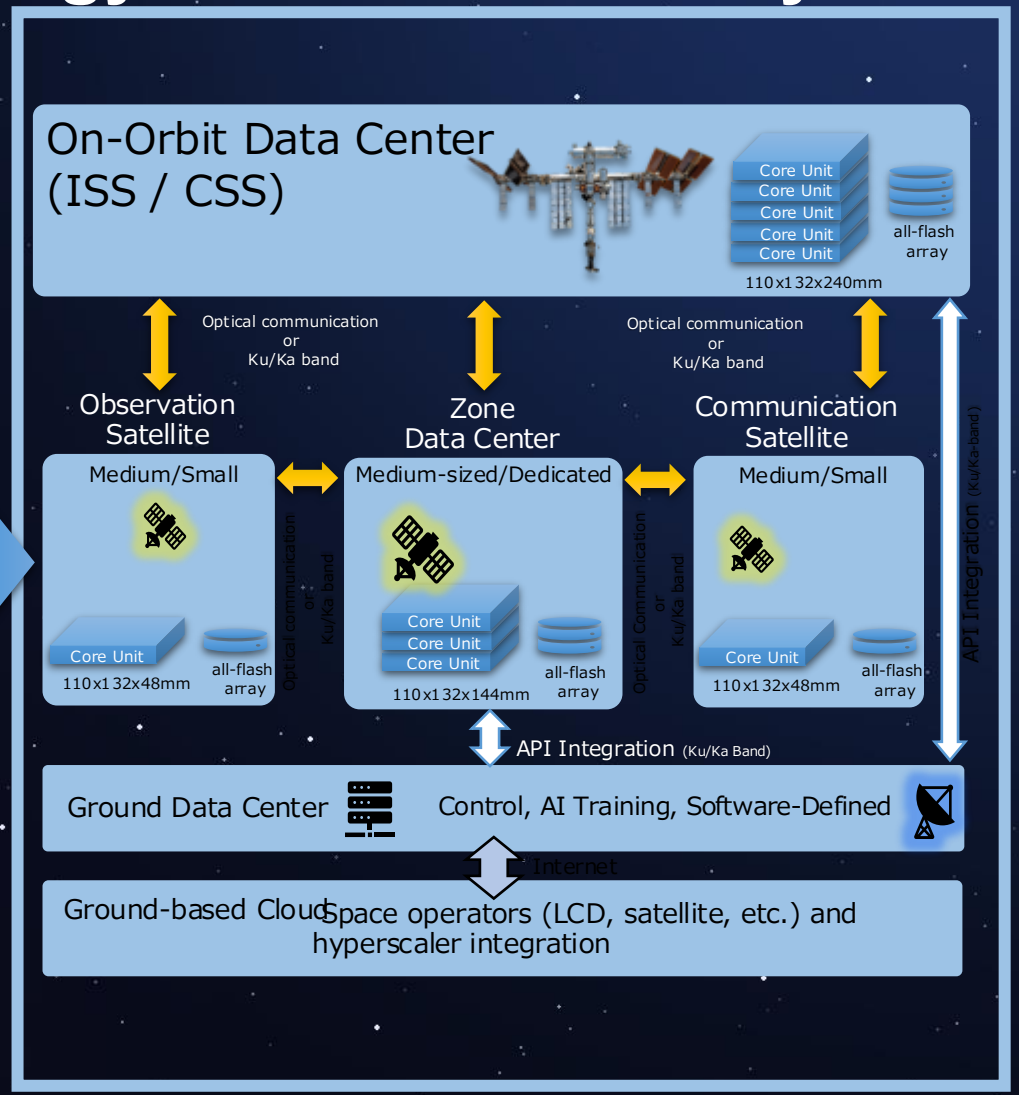
- Virtualized Linux running on a high-dependability framework
- High-dependability real-time OS and real-time hypervisor
- Early adoption of high-dependability technology meeting next-generation autonomous vehicle functional safety requirements (ISO 26262)

●AI-based System Resource Control

- Achieves high dependability, high energy efficiency, and low heat dissipation through AI-based control of dependability functions and system resource management
- Utilization of reinforcement learning-based AI
- Integrated control via autonomous AI - Operational range restricted for safety assurance

High-dependability Data Center Essential Requirements

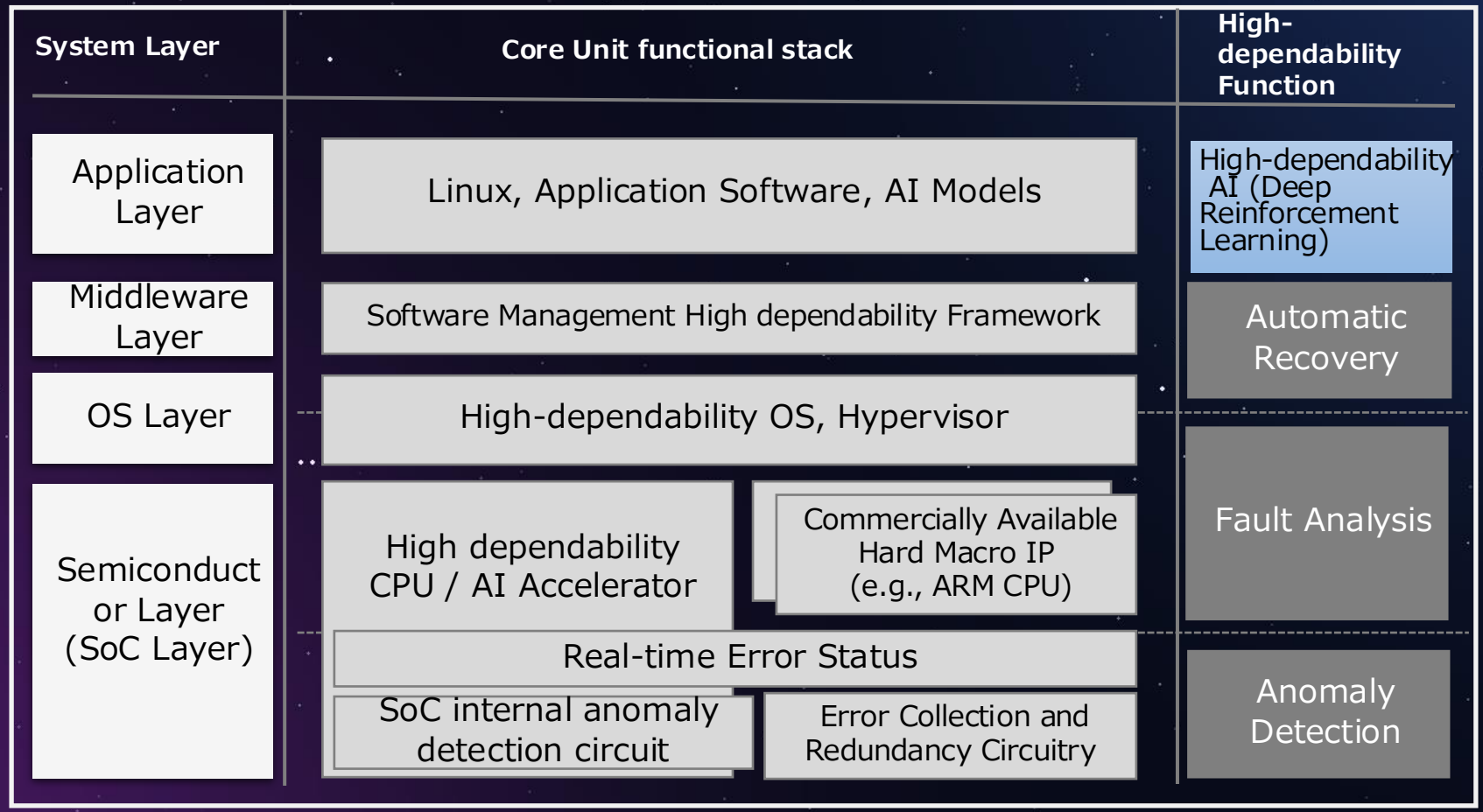
1. High Availability (Uptime)
   - Redundancy and data sharing
2. Highly Reliable System Arch.
   - Clustering and Load Sharing
3. Cluster system monitoring
   - Failure Detection, Analysis, and Recovery
4. Load Sharing
   - Load Balancers & Service Monitoring
5. Server Virtualization
   - Hypervisor-based Energy Efficiency
   - Improved energy efficiency, effective resource utilization through AI,
   - Utilization of open-source assets



APPROACH

The Full-Stack Approach for High-dependability

- The ”Core Unit” consists of two OBCs(On-board computer), forming the smallest unit in a data center
- Multiple core units are clustered together to form a data center
- The core unit's high-dependability technology widely utilizes technologies from semiconductors to AI in a Full-Stack approach



THESIS

Why the heterogeneous MPSoC FPGA is the building block

Programmable Logic as substrate

Hardening circuits are synthesized into the PL fabric — node- and fab-independent, re-targetable as COTS scales.

Heterogeneous compute domains

SoC IP (ARM Core Processors, AI Engine array) and RISC-V HD / AI Engine HD implemented as the PL fabric let software be pinned per domain — making fault isolation tractable.

Reconfigurability = recovery

Partial reconfiguration (ICAP; Internal Configuration Access Port) rewrites a faulted region in microseconds; the fabric is both the workload and the repair tool.

Performance density

AI-Engine throughput at edge-class power — the density an orbital data center needs without an ASIC tape-out.

PLATFORM

DIOS hardware architecture with MPSoC FPGA

Real-time control processor. Controls satellite and station equipment. Supports dual redundancy.

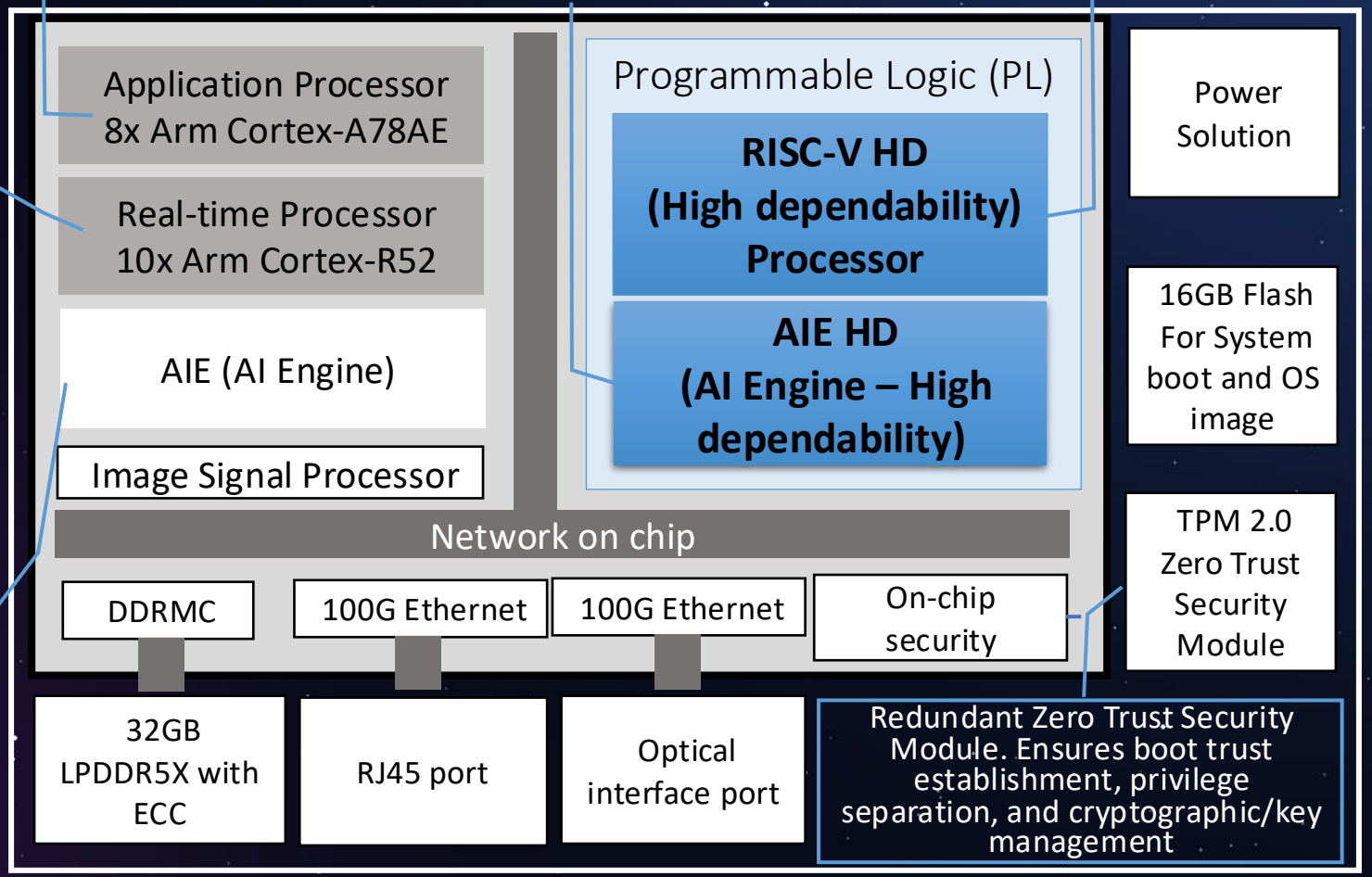
High-performance CPU. For application execution. Supports dual redundancy

High-dependability AI accelerator engine. DIOS's high-dependability circuit technology applied to the accelerator's internal circuitry

High-dependability CPU. DIOS high-dependability circuit technology applied to CPU internal circuits

On-board Computer (OBC)

- Multiple CPUs redundantly utilized for each application and equipment control in the data center
- The newly developed RISC-V HD and AIE HD handle high-dependability functions
- Dynamic control of energy consumption and heat generation through diverse power-saving features



Application AI accelerator. Supports TensorFlow, PyTorch, ONNX, and over 200 models in the Model Zoo (repository)

04

RADIATION

Radiation-resistant mechanisms

RADIATION

Where the radiation comes from

Three populations, each with a different origin, energy, and the geometry that lets it reach a spacecraft.

Trapped particles (Van Allen belts)

- Charged particles held by Earth's magnetic field
- Inner belt: energetic protons · Outer belt: relativistic electrons
- Dominant LEO dose source — through the SAA

Galactic Cosmic Rays (GCR)

- High-energy heavy ions from outside the solar system
- Low flux but very high LET; nearly impossible to shield
- Drive SEL / SEB and high-LET upsets; peak when the Sun is quiet

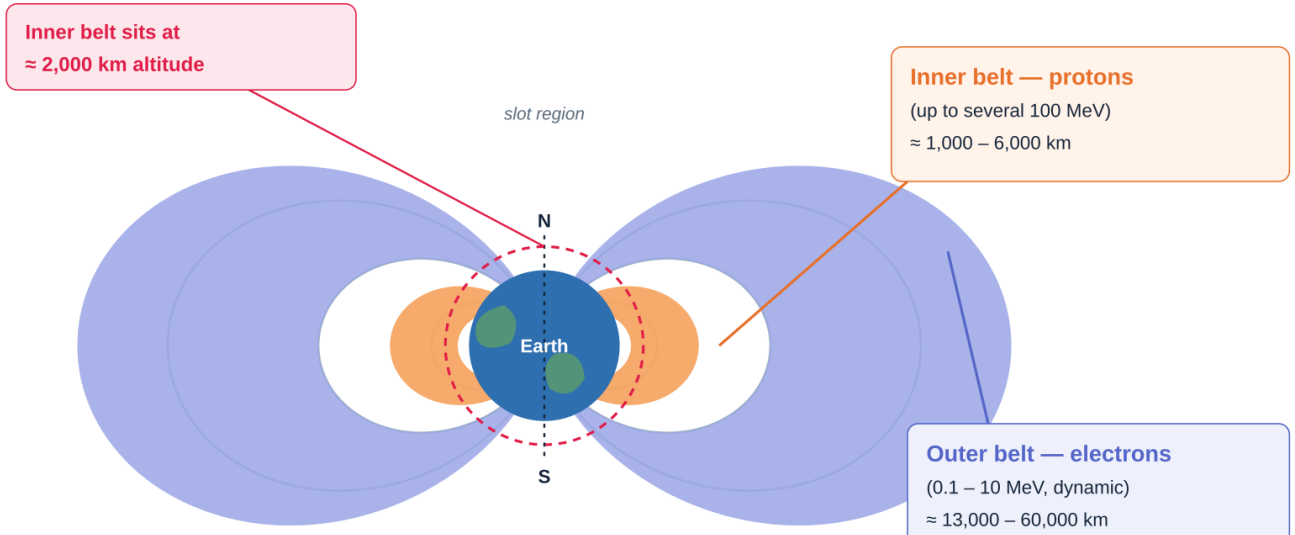
Solar Energetic Particles (SEP)

- Episodic proton bursts from solar flares / CMEs
- Huge, short-lived fluxes → sudden dose spikes
- Reach high latitudes and the poles most easily

Geometry sets the dose. Geomagnetic shielding is strongest at the equator and weakest at the poles and over the South Atlantic Anomaly. Two parameters describe this: the **L-shell** (which field line a particle is trapped on) and the **geomagnetic cutoff rigidity** (the minimum momentum a particle needs to reach a given location). The next slides follow these two ideas.

RADIATION

(1) The Van Allen belts & Earth



Charged particles trapped by Earth's dipole field form two doughnut-shaped belts; in a meridional cut they appear as lobes hugging the magnetic equator.

STRUCTURE

An inner belt and an outer belt, separated by a low-flux "slot." Their boundaries follow magnetic field lines (L-shells).

ALTITUDES

Inner belt ≈ 1,000–6,000 km — a representative ~2,000 km up, peak proton flux ~3,000 km. Slot ~6,000–13,000 km. Outer belt ≈ 13,000–60,000 km.

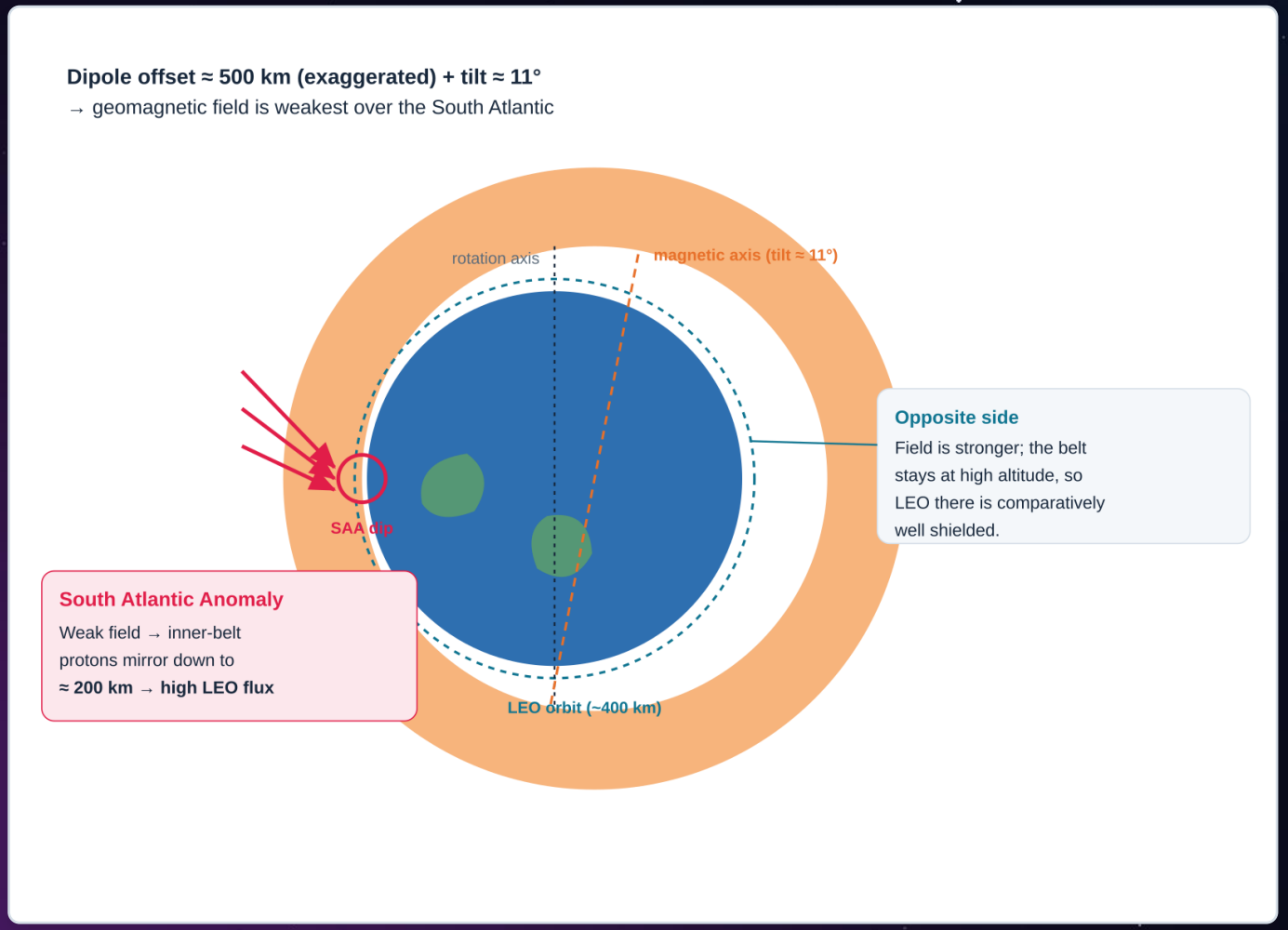
PARTICLES

Inner: protons up to several hundred MeV (very penetrating) plus electrons. Outer: relativistic electrons (0.1–10 MeV), highly dynamic during storms.

For LEO: The inner belt is the main hazard — and it is what dips into the SAA.

RADIATION

(2) South Atlantic Anomaly (SAA) — why it exists



Earth's magnetic dipole is tilted ~11° and offset ~500 km from the planet's center, so the field is weakest over the South Atlantic.

WHY IT FORMS

Where the field is weakest, trapped inner-belt protons mirror down to their lowest altitudes (≈ 200 km). A LEO spacecraft there plunges into the inner belt.

DISTRIBUTION

A broad region centered ~25°S, 30–40°W, spanning South America to southern Africa; drifting westward (~0.3°/yr) and slowly reshaping.

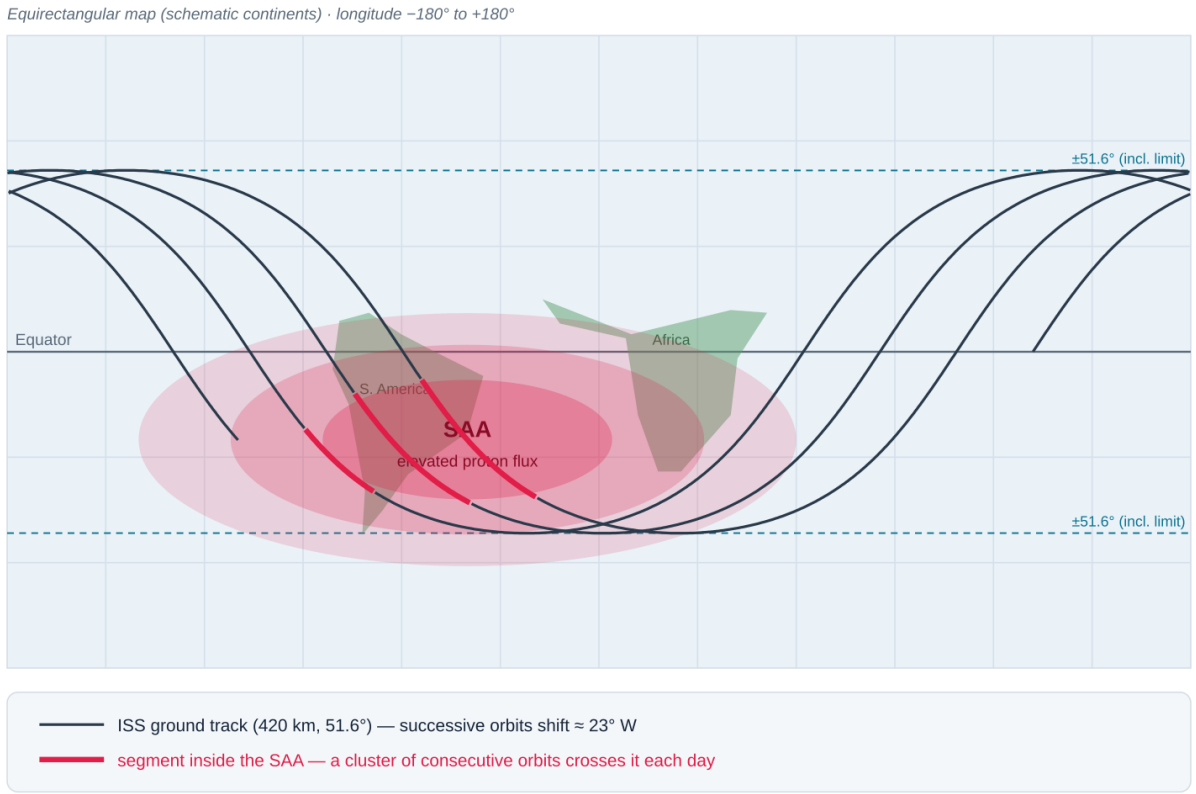
EFFECT

The SAA produces the large majority of LEO trapped-particle dose and single-event upsets. Crews report “light flashes”; sensitive instruments are often safed during passes.

Key point: Most LEO SEUs occur in the few minutes per orbit spent inside the SAA.

RADIATION

(2) SAA distribution & the ISS example



For an ISS-class orbit (≈ 420 km, 51.6°), the ground track sweeps through the SAA on a cluster of consecutive orbits each day.

ORBIT

Period ≈ 92.8 min → ~15.5 orbits/day; each successive ground track shifts ≈ 23° west.

SAA PASSES PER DAY

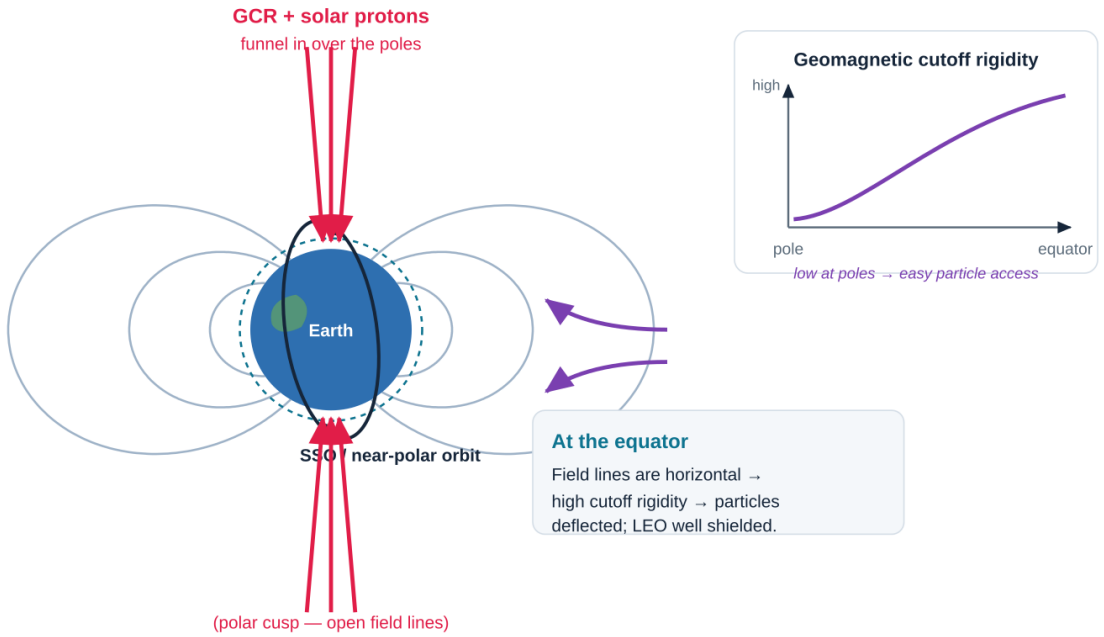
Roughly 6–9 of the daily orbits cross the SAA (depending on the flux threshold), in one consecutive block.

TIME IN THE SAA

Each transit lasts ≈ 5–12 min; cumulative time ≈ 40–85 min/day — on the order of ~1 hour. These minutes dominate the daily SEU count and proton dose.

Assumptions: Illustrative — simplified Keplerian track; SAA modeled as an elevated-flux ellipse (~25° S, 40° W). Exact count depends on the chosen flux contour and drifts over time.

(3) Near-Polar Orbit (NPO) & Sun-Synchronous Orbit (SSO)



Every orbit crosses both polar regions (≈ 28–30 high-latitude transits/day).

During a Solar Particle Event, polar passes can deliver large dose spikes; GCR adds a steady, high-LET background.

Near-polar orbits (e.g. Sun-synchronous, ~98°, 600–800 km) pass over both poles every orbit — exactly where geomagnetic shielding is weakest.

CUTOFF RIGIDITY

The field deflects particles strongly at the equator (high cutoff) but barely at the poles (low cutoff), so GCR and solar protons reach LEO over the polar caps.

POLAR CUSP

Open, near-vertical field lines funnel particles straight down; the spacecraft crosses these high-latitude regions ≈ 28–30 times/day.

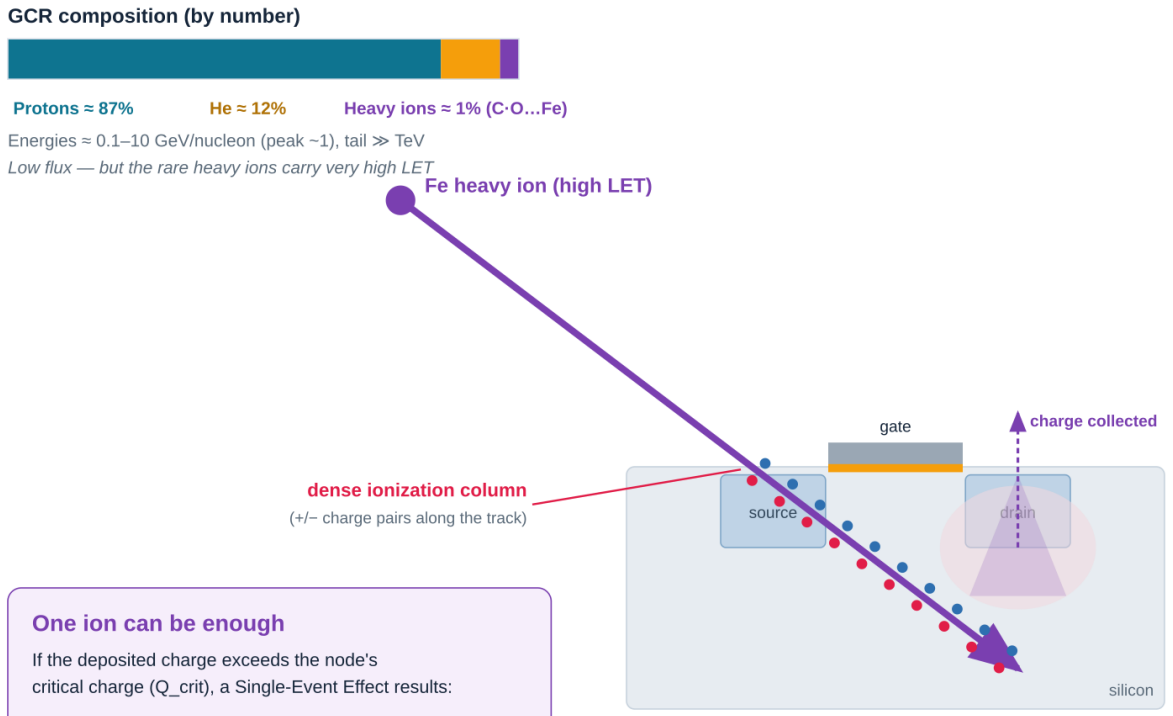
SOLAR EVENTS vs GCR

Solar Particle Events deliver large dose spikes at the poles; between events, GCR gives a steady, very penetrating, high-LET background (SEL / SEB / high-LET SEU).

Also: High-latitude passes can clip the outer electron-belt “horns” → surface dose & internal (deep-dielectric) charging.

RADIATION

(4) Galactic Cosmic Rays (GCR) — a direct hit



GCR are atomic nuclei accelerated outside the solar system to enormous energies — sparse, but each one individually dangerous.

WHAT THEY ARE

By number: ~87% protons, ~12% helium, ~1% heavier nuclei from carbon and oxygen up to iron (Z=26) and beyond. The rare heavy ions carry most of the damage potential.

ENERGY & FLUX

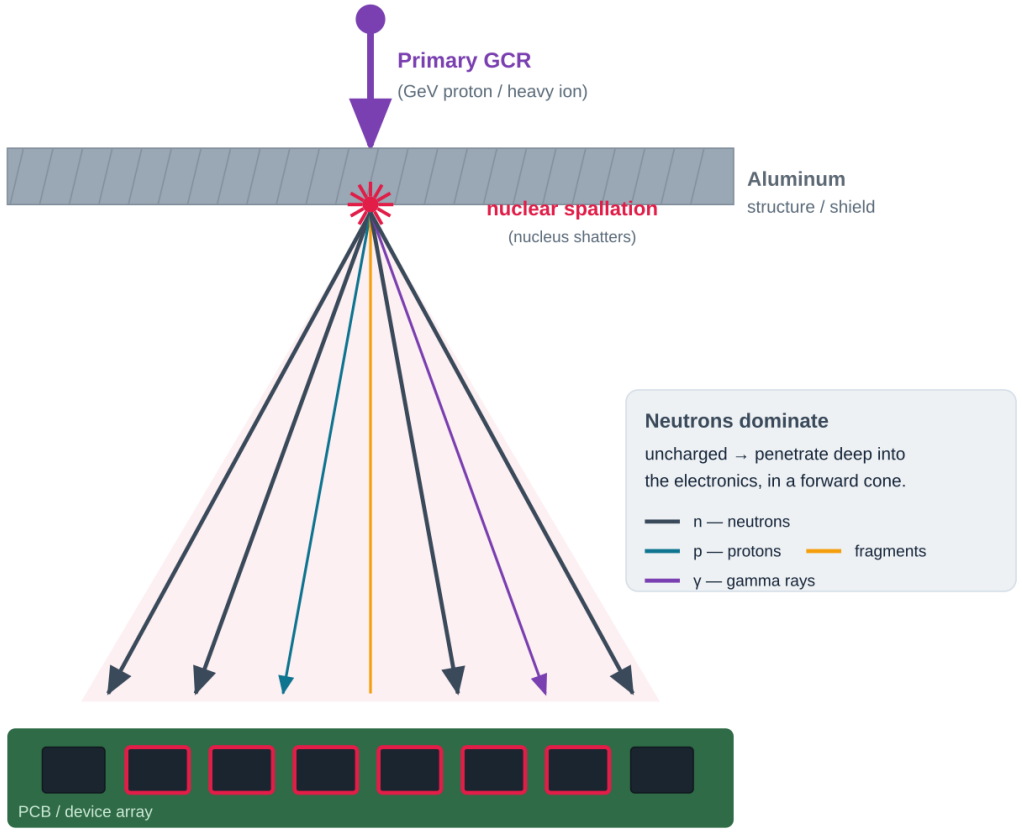
Spectrum peaks near ~1 GeV/nucleon with a tail far above TeV. Flux is low (a few particles cm^{-2} s^{-1}) and rises when the Sun is quiet (solar minimum).

UNSHIELDED STRIKE

One heavy ion leaves a dense column of electron–hole pairs (very high LET/Linear Energy Transfer). If the charge collected at a node exceeds its critical charge, a Single-Event Effect fires at once.

Why it matters: High LET means a single ion can cause not just soft SEU/SET but destructive SEL or SEB/SEGR — and no practical shield stops GeV heavy ions.

(4) When shielding backfires — secondary showers



Many devices struck at once → simultaneous SEE (MCU / MBU, correlated upsets) — can defeat simple redundancy.

More aluminum can mean more secondaries: shielding has an optimum, and redundant copies should not share one footprint.

Aluminum stops electrons and slow protons, but a high-energy GCR can shatter an aluminum nucleus and create a spray of secondaries.

NUCLEAR SPALLATION

The collision breaks the nucleus apart, producing neutrons, protons, lighter fragments and gamma rays — a shower directed forward, into the spacecraft interior.

A CONE OF NEUTRONS

Uncharged neutrons penetrate deeply and fan out in a cone. Where that cone lands, many devices are struck within nanoseconds of one another.

MULTI DEVICE SEE

The outcome is multiple-cell / multiple-bit upsets and correlated events across chips — a common-cause failure that can defeat simple redundancy.

Design implication: Shielding has an optimum — more aluminum can mean more secondaries — and redundant copies should be physically separated, not in one shower footprint.

RADIATION

Implications by region & orbit

Mapping the environment to where it bites — and to the device-level effects from the companion deck.

Source	Where it dominates	Main device effects	Design response
Inner belt via the SAA	LEO at moderate incl. (ISS 51.6°, i-SEEP)	SEU bursts; proton TID & DDD	EDAC/scrubbing; SAA-aware operations
Outer-belt electrons	MEO/GTO; high-latitude “horns”	Surface dose; deep-dielectric charging	Shielding; grounding & bleed paths
GCR (heavy ions)	Everywhere; worst at poles & solar min	SEL, SEB, high-LET SEU	Latch-up protection; TMR / FDIR
Solar protons (SEP)	Polar / high-latitude; episodic	Dose spikes; SEU surge	Safing; radiation design margin (RDM)

Bottom line: *altitude alone doesn't predict dose. The SAA loads a 51.6° LEO platform with trapped-proton SEUs in a few minutes per orbit, while a polar/SSO satellite trades that for GCR + solar-proton access over the caps. Both must be carried explicitly in the radiation budget and FDIR design.*

Classification of radiation effects

Two families: instantaneous single-particle events, and slow cumulative-dose degradation.

Single Event Effects (SEE) — Soft Errors

SEU (Single Event Upset)
— bit flip in a storage cell

SET (Single Event Transient)
— transient pulse in logic / analog

SEFI (Single Event Functional Interrupt)
— device enters an abnormal mode

Single Event Effects (SEE) — Hard Errors

SEL (Single Event Latch-up)
— parasitic SCR latch-up, high current

SEB (Single Event Burnout)
— burnout of a power device

Cumulative dose effects — Hard Errors

TID (Total Ionizing Dose)
— ionizing dose trapped in oxides → Vth shift, leakage

DDD (Displacement Damage Dose)
— atomic displacement → lattice defects → reduced carrier lifetime

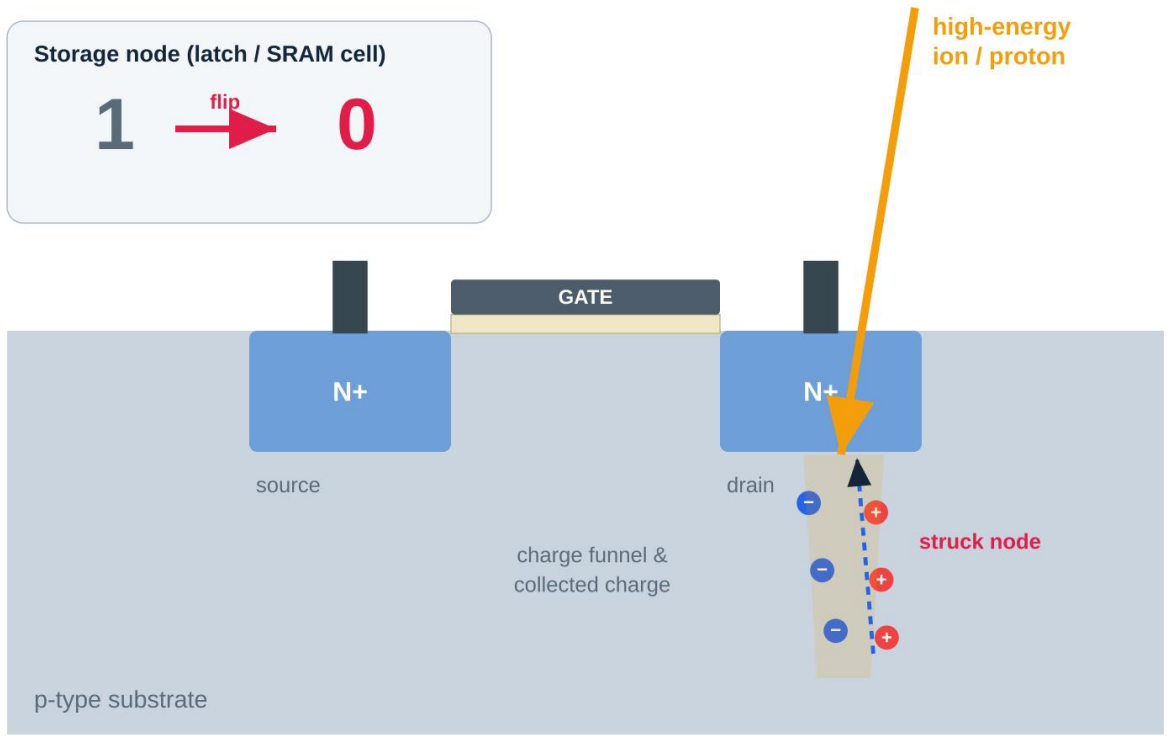
Single-event effects come from one particle and are stochastic.
Cumulative effects build up with total exposure over the mission.

Soft Error: temporary malfunction (recoverable)
Hard Error: permanent malfunction (destructive)

RADIATION

SEU : Single Event Upset

Soft Error (recoverable)



A single energetic particle deposits enough charge at a sensitive node to flip a stored logic state — a "bit flip."

MECHANISM

The ion ionizes silicon along its track, creating electron–hole pairs. Charge collected at a reverse-biased junction overrides the value held by a memory cell or flip-flop.

EFFECT

One or more stored bits change value. The data is corrupted, but the hardware is undamaged.

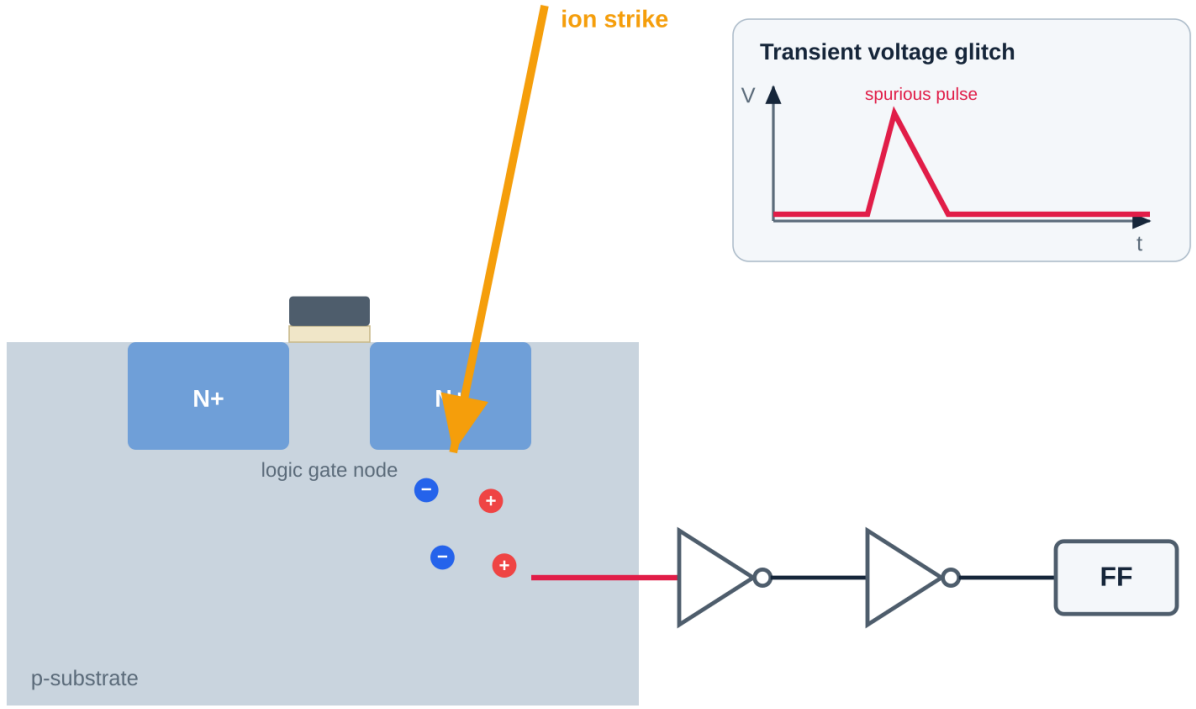
RECOVERY

Non-destructive ("soft error"). Cleared by rewriting, ECC/EDAC, or memory scrubbing.

Susceptible: SRAM, DRAM, flip-flops, registers, FPGA configuration memory

SET : Single Event Transient

Soft Error (recoverable)



Glitch propagates through the logic path → may be latched as a wrong value

A momentary voltage/current pulse generated in combinational logic (or analog circuits) by a single particle strike.

MECHANISM

Charge collection at a logic-gate node produces a spurious transient. Unlike an SEU, it occurs in circuitry that is not itself a storage element.

EFFECT

If the glitch reaches a latch during a clock edge, it is captured as a wrong value — becoming an upset. It can also disturb analog/mixed-signal parts (op-amps, comparators, PLLs).

RECOVERY

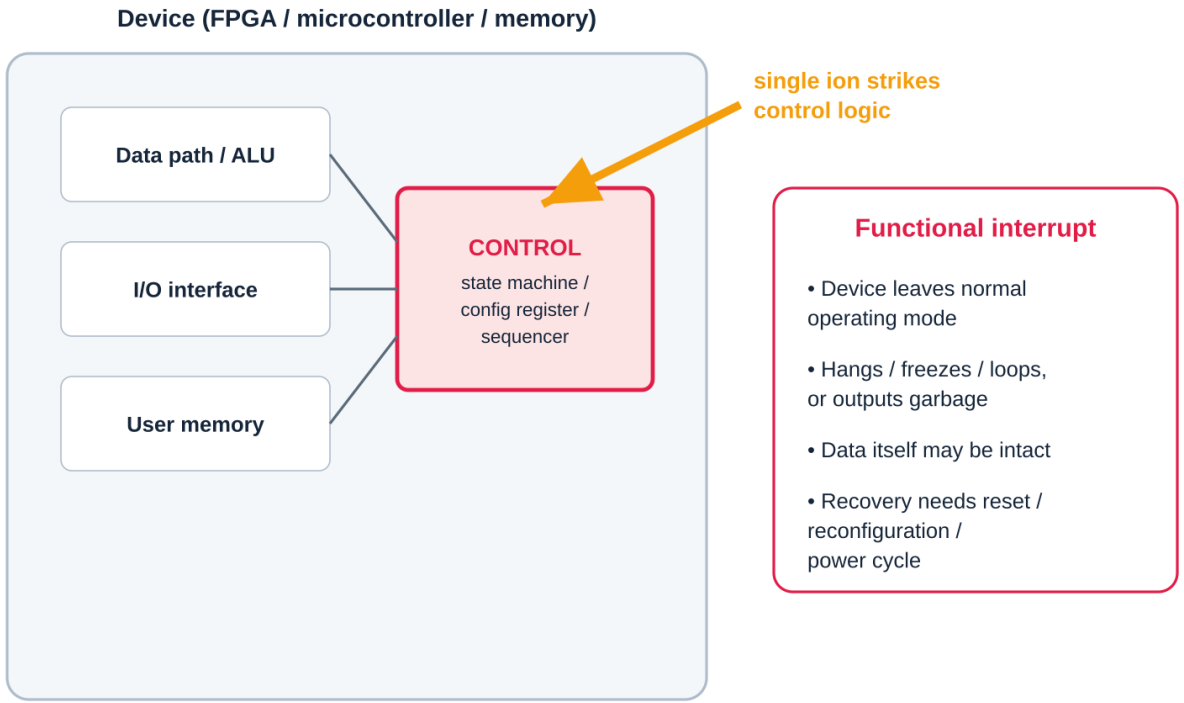
Non-destructive; pulse width and propagation depend on technology node and timing.

Susceptible: Combinational logic, clock/reset nets, analog & mixed-signal circuits

RADIATION

SEFI : Single Event Functional Interrupt

Soft Error (recoverable)



A single event puts the device into an abnormal operating mode, interrupting normal function.

MECHANISM

Typically an upset in control logic — a state machine, control/configuration register, sequencer, or reset/test circuitry — rather than in user data.

EFFECT

The device hangs, locks up, resets, or emits garbage. Stored data may be intact, yet the part is not operating.

RECOVERY

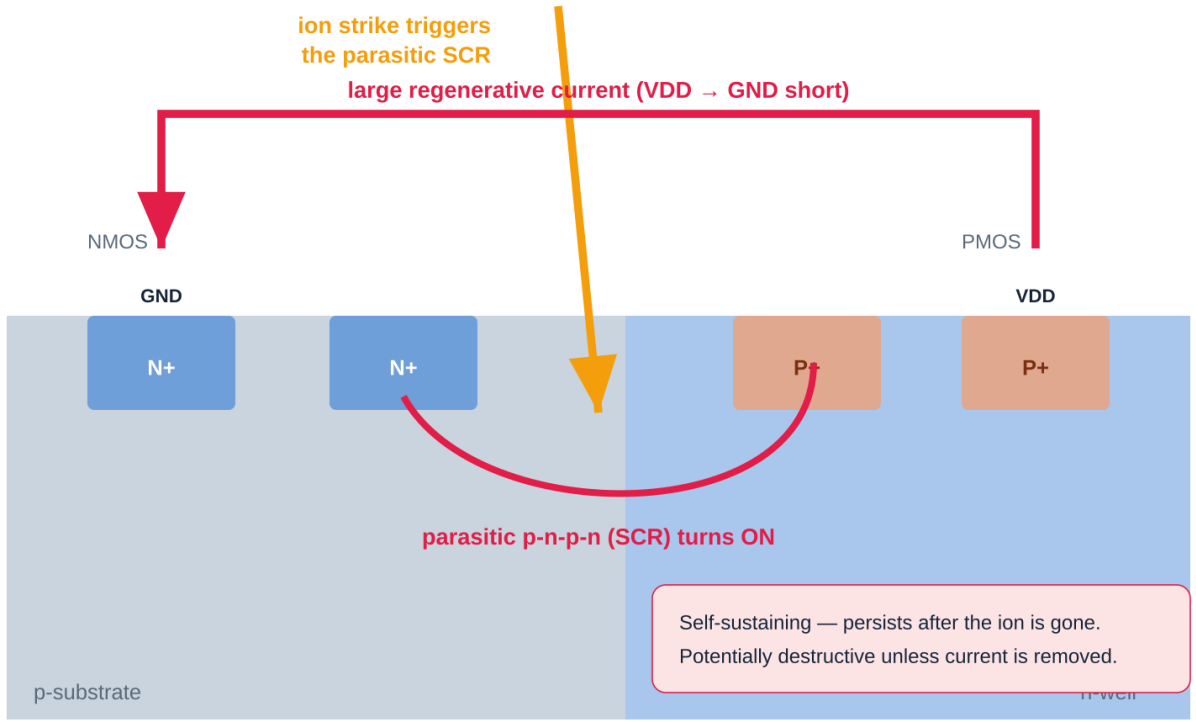
Requires a reset, reconfiguration, or power cycle — more disruptive than a single SEU.

Susceptible: FPGAs, microprocessors, advanced memories, ADCs / complex ICs

RADIATION

SEL : Single Event Latch-up

Hard Error (destructive)



A single particle triggers the parasitic p-n-p-n (SCR) structure inherent to bulk CMOS, shorting power to ground.

MECHANISM

The strike forward-biases the parasitic bipolar transistors; regenerative feedback latches them ON, creating a low-resistance VDD→GND path.

EFFECT

A large, self-sustaining current flows and persists after the ion is gone. Uncleared, localized heating can permanently destroy the device.

RECOVERY / MITIGATION

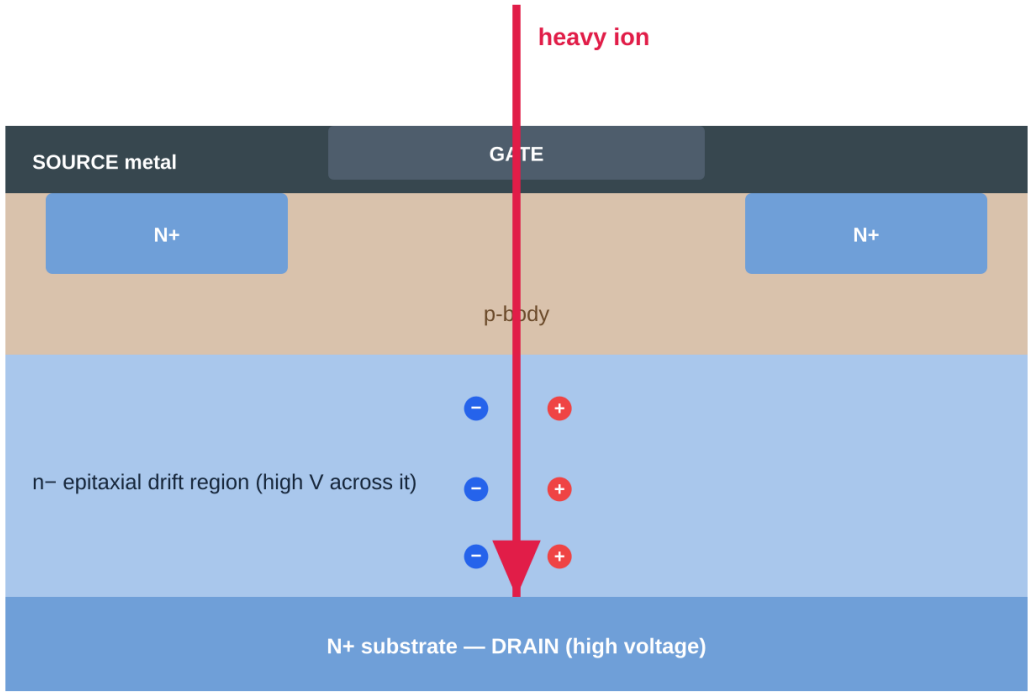
Power must be removed or cycled to clear it. Current-limiting, SOI, epitaxial substrates, and guard rings reduce susceptibility.

Susceptible: Power MOSFETs, IGBTs, BJTs, rectifiers at high bias

RADIATION

SEB : Single Event Burnout

Hard Error (destructive)



Ion track + high field → parasitic n-p-n BJT turns on → avalanche / current filament

→ localized thermal runaway → permanent burnout (destructive, hard failure)

A heavy ion triggers destructive, regenerative breakdown in a high-voltage power device.

MECHANISM

The dense ion track in a high-field region (e.g., the n- epi drift of a power MOSFET) turns on the parasitic BJT and starts avalanche multiplication / current filamentation.

EFFECT

Localized thermal runaway burns out the device — a permanent, catastrophic (hard) failure.

MITIGATION

- Voltage derating (operate well below rated VDS) and rad-hard / SEB-screened parts.

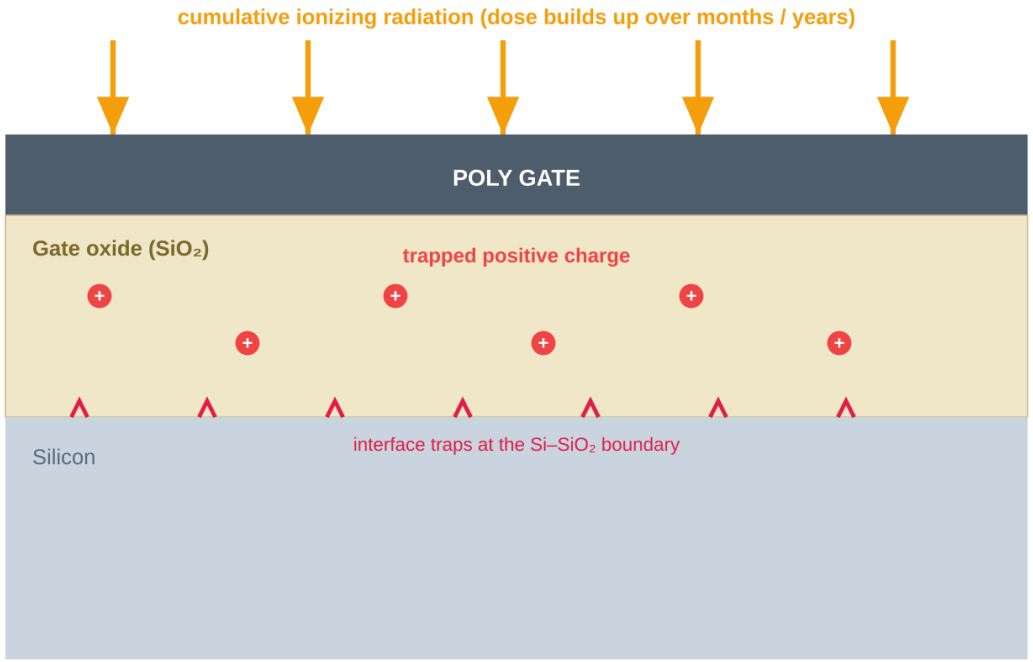
Susceptible: Bulk CMOS logic, memories, mixed-signal ICs

RADIATION

TID : Total Ionizing Dose

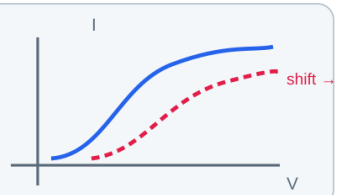
Gradual degradation

Hard Error (destructive)



Cumulative effects:

- Threshold-voltage (Vth) shift
- Increased leakage current
- Timing / drive-strength degradation, eventual functional failure



The long-term, cumulative effect of ionizing radiation depositing charge in insulating layers.

MECHANISM

Ionization in gate/field oxides creates electron–hole pairs; holes become trapped as positive oxide charge, and interface traps form at the Si–SiO_2 boundary.

EFFECT

Threshold-voltage shift, increased leakage current, and slower switching — progressing to parametric or functional failure.

METRIC / MITIGATION

Measured in rad(Si) or Gy; grows with mission dose. Mitigated by rad-hard design/process, shielding, and dose margin (RDM).

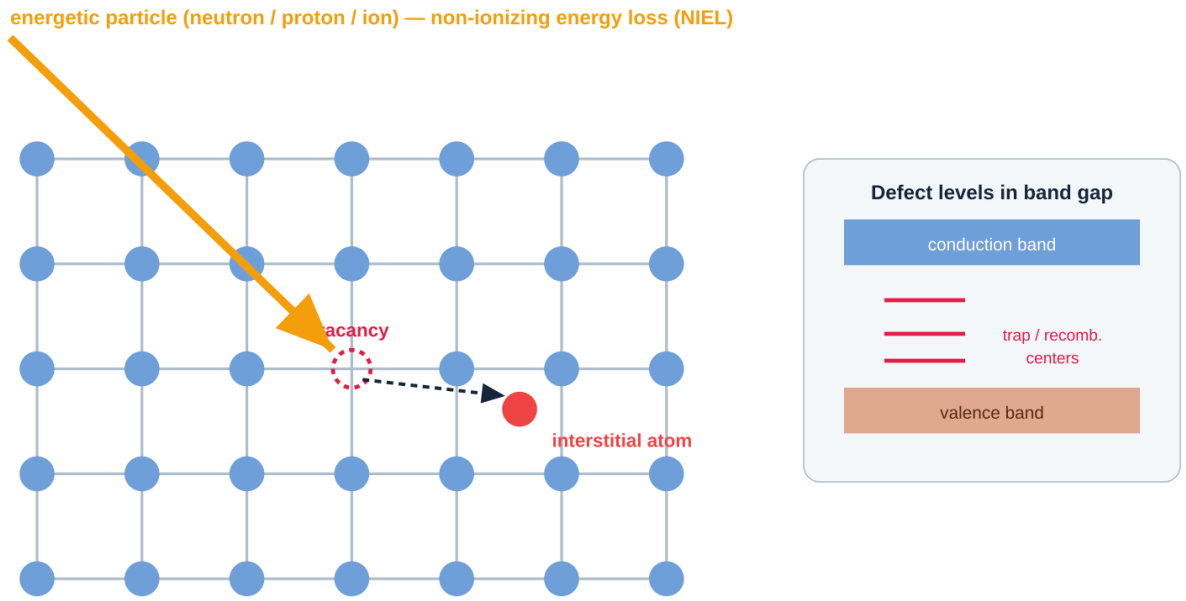
Susceptible: MOS transistors, oxides, almost all CMOS over mission life

RADIATION

DDD : Displacement Damage Dose

Gradual degradation

Hard Error (destructive)



Lattice defects act as recombination / trapping centers → reduced minority-carrier lifetime

Degrades bipolar devices, solar cells, photodiodes, LEDs, image sensors; effect is cumulative.

Cumulative damage from particles knocking atoms out of their crystal-lattice sites (NIEL: Non-Ionizing Energy Loss).

MECHANISM

A displaced atom leaves a vacancy and lodges as an interstitial (a Frenkel pair). These defects introduce energy levels within the band gap.

EFFECT

Defect levels act as recombination/generation and trapping centers, reducing minority-carrier lifetime and degrading device parameters.

METRIC

Quantified by particle fluence (cm^{-2}) or displacement damage dose; protons and neutrons dominate.

Susceptible: Bipolar devices, solar cells, photodiodes, LEDs, optocouplers, image sensors

MECHANISM

DIOS Radiation-resistant mechanisms for semiconductor

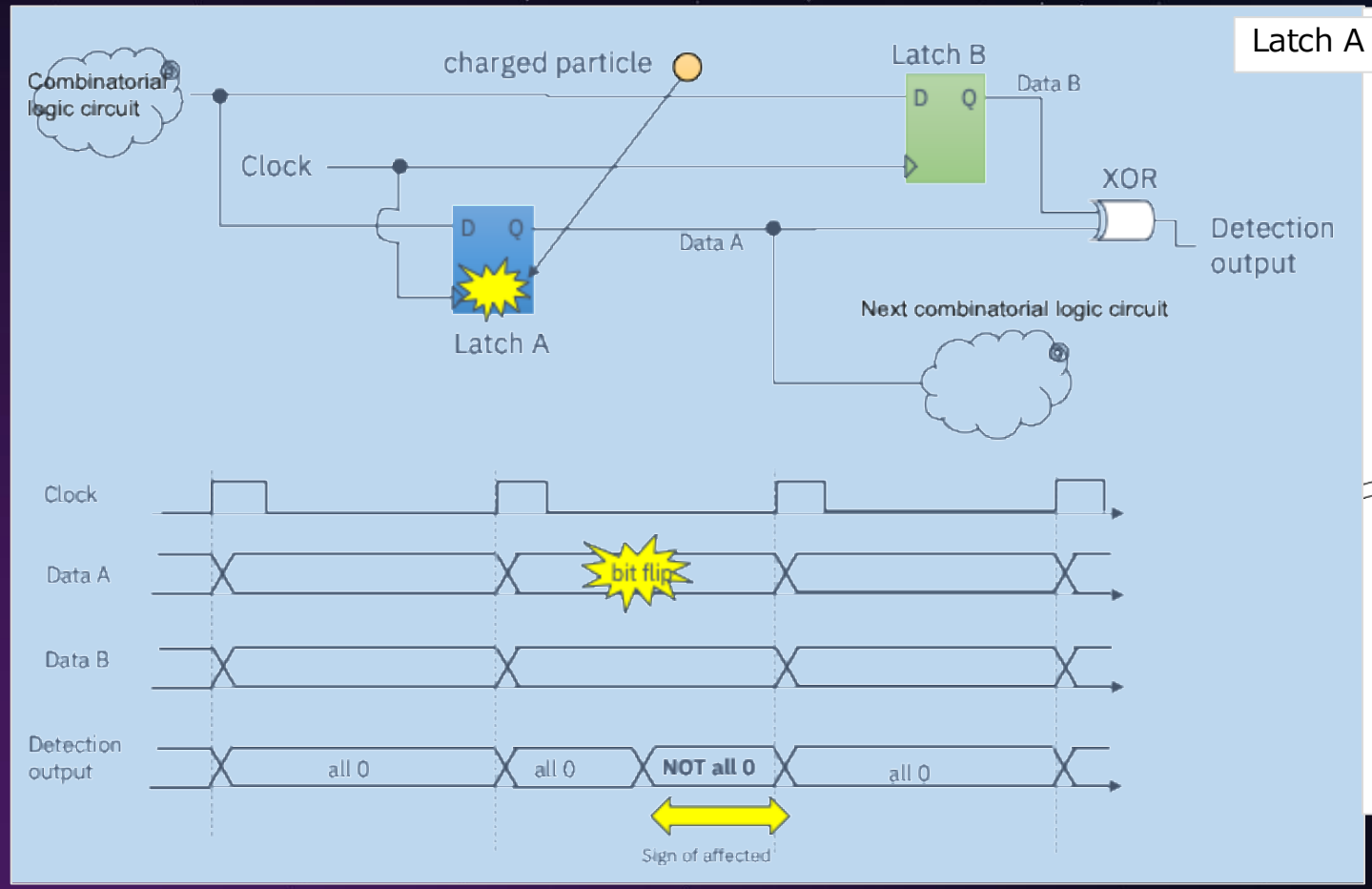
- Achieved through DIOS's high-dependability architecture—cannot be realized by any single technology alone
- By utilizing semiconductor circuits as "sensors," error detection previously impossible becomes achievable
- Overcomes inherent weaknesses of the latest technology nodes and FPGAs

Error Countermeasures	Error Detection and Mitigation	Target	SEU	SET	SEFI	SEL	SEB	TID	DDD
Memory Error Correction	ECC and Scrubbing Mechanism	DRAM and FPGA circuits incorporate LUT (Look Up Table) distributed RAM, Block-RAM, Ultra-RAM	✓	✓	✓	-	✓	-	-
Combination Circuit Error Countermeasures	Dual redundancy or triple redundancy	Dual redundancy: ARM CPU Triple redundancy: AI Engine (internally divided into three sections), RISC-V HD, AI Engine HD	-	✓	✓	✓	✓	-	-
Latch circuit Error countermeasures	Detection via output comparison of two physically separated latches	Circuits within RISC-V HD that are small in scale yet significantly impact CPU or AI accelerator operation, such as majority voting functions, error detection circuits, and register files	✓	✓	✓	✓ Combined with power supply monitoring	✓	-	-
CRAM Error Handling	ECC and Scrubbing Mechanism	CRAM (Configuration RAM). SRAM specific to FPGAs. Stores configuration information for programmable circuits.	-	-	✓	- Combined with power supply monitoring	✓	✓	✓
Detection of heavy particle collisions and neutron showers	Equipped with a sensor mechanism for locating the point of origin within a semiconductor chip	Entire programmable area	-	-	✓	-	✓	- Statistical estimation	- Statistical estimation

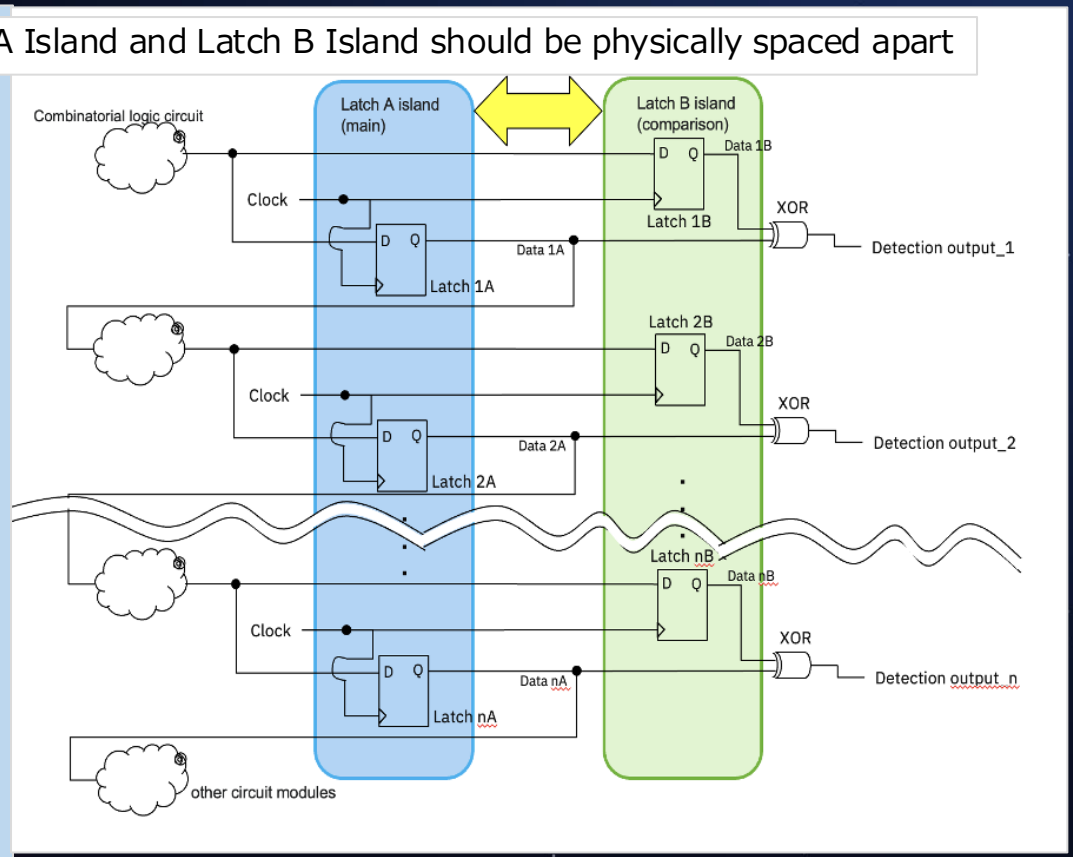
MECHANISM

Latch circuit Error countermeasures: detecting SEU of latch

- Prepare a comparison circuit that performs equivalent operations to the main circuit. Continuously compare values to detect SEUs.
- To prevent both the main circuit and comparison circuit values from inverting during a single SEU (to prevent malfunction), physically place them on the chip with a gap between them.
- Add one more one latch circuit for real time error collection.



Latch A Island and Latch B Island should be physically spaced apart

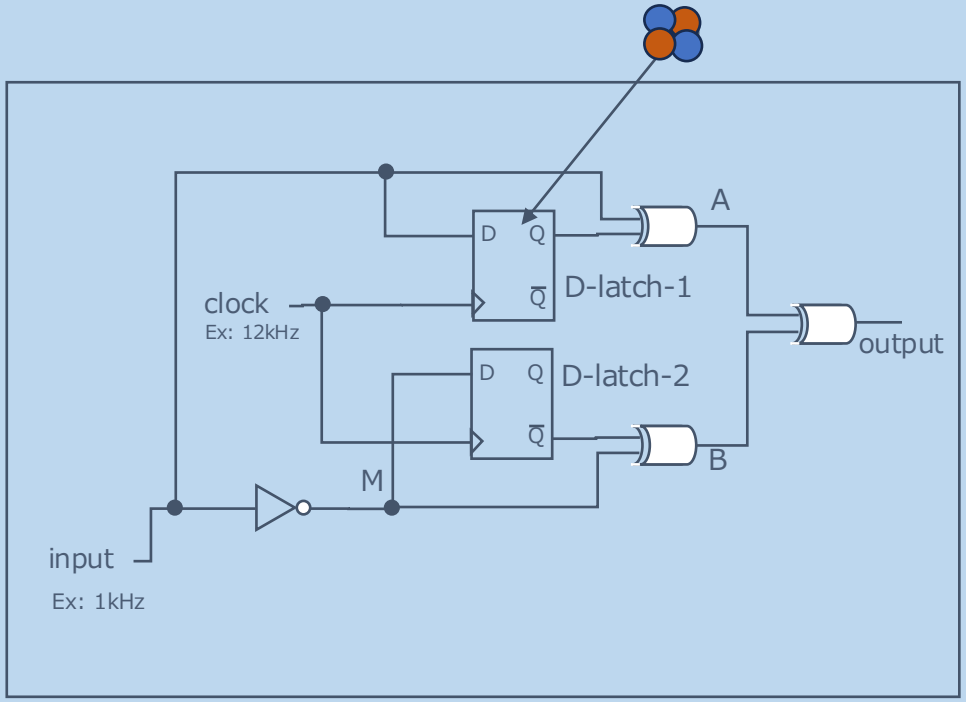


MECHANISM

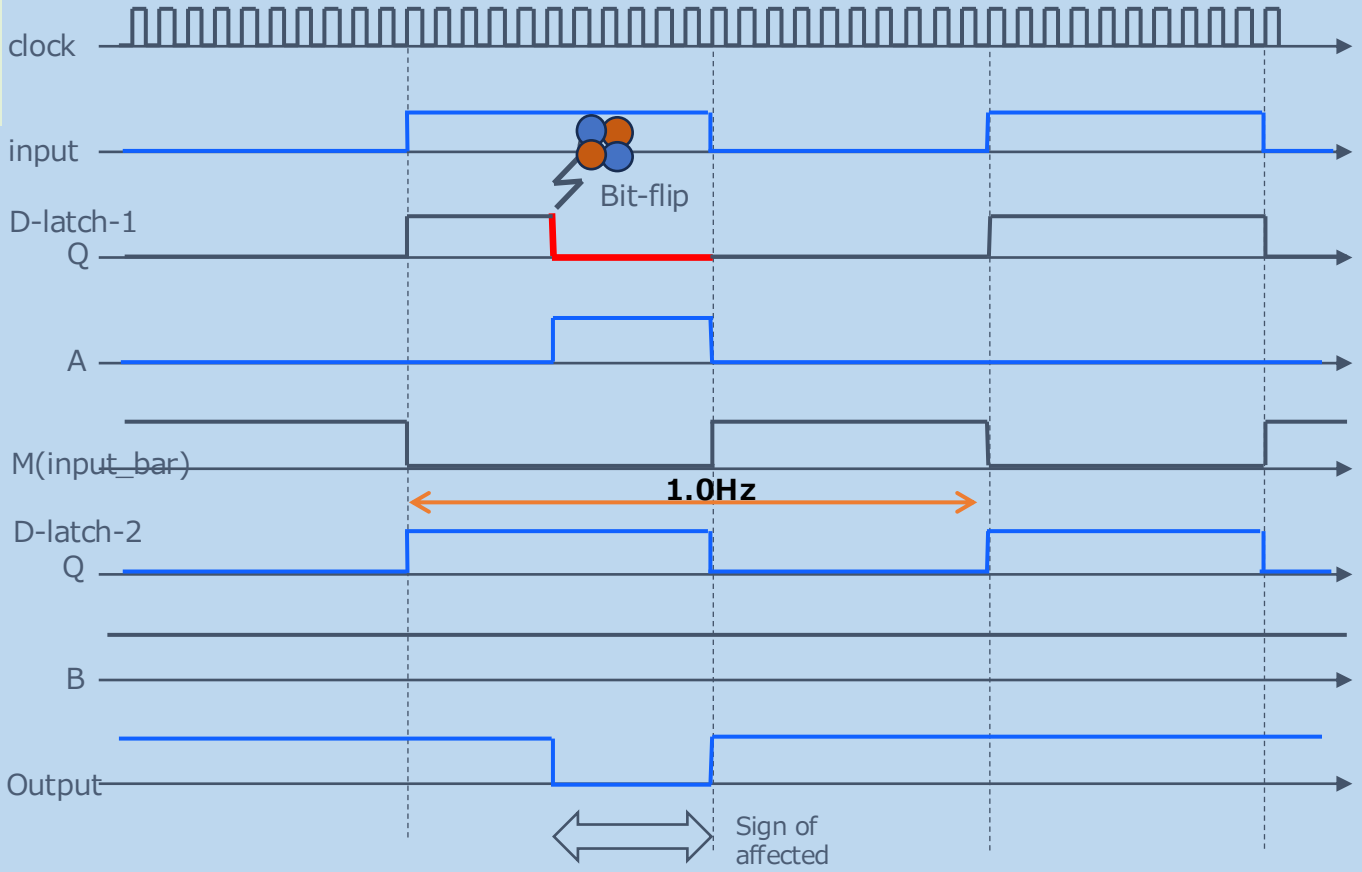
Silicon Heartbeat: detecting heavy-ion particle collisions

[Basic Idea]
- A small circuit and clock for bit-flip detection are prepared.
- A large number of the detection circuits are densely distributed on the chip.
- In order to identify the affected location, it is equipped with a circuit (register) that grasps the position, ID, and status of the detection circuits.

[Basic Idea (cont'd)]
- In order to enable to determine whether it is broken, affected or correct behavior, the output of the detection circuit is always toggled.
- It is applicable to both memory and logic circuits.



Circuit of a detection element

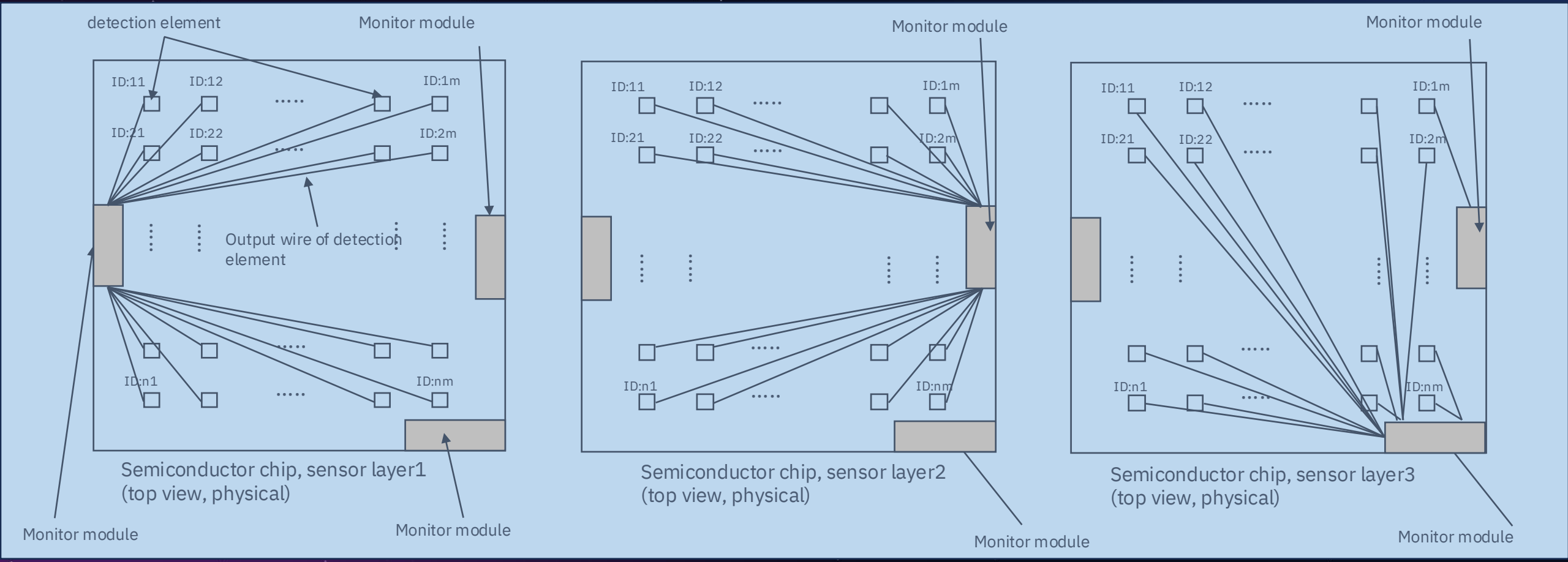


MECHANISM

Silicon Heartbeat: detecting neutron showers

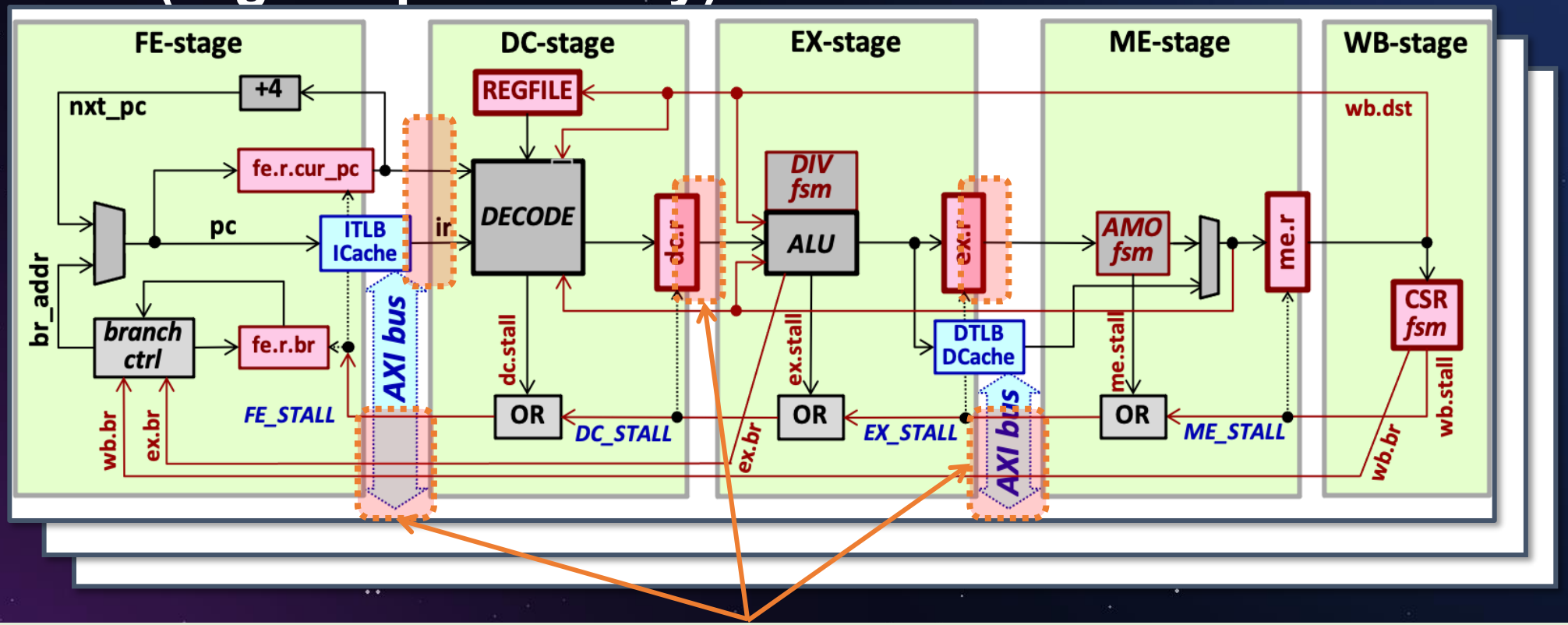
To avoid single failure mode:
- Monitor module(s) monitor output of detection elements
- Triple redundancy applied

(cont'd)
- Parallel connection between detection elements and one or more Monitor module(s)



MECHANISM

RISC-V HD (High Dependability) Processor



- **Triple-redundant RISC-V core**: Temporary fault detection via majority voting of internal redundant signals.
- **CRAM error detection**: If fault detection persists for multiple clock cycles, it is judged as a CRAM error and the faulty core's CRAM is rewritten (using ICAP).
- **FF Error**: Detected and automatically corrected by Latch circuit Error countermeasures.
- **Data RAM Error**: SRAM scrubbing - SW/OS cooperation.
- Fault area narrowing via **Silicon Heartbeat**.

MECHANISM

Memory Error Correction

Overcomes weaknesses of the latest technology node

- Using off-the-shelf GPGPUs or AI accelerators as-is is ***dangerous***
- SRAM and scrubbing mechanism adopted.

Per hour
0.5 to 5
Recognition errors occur

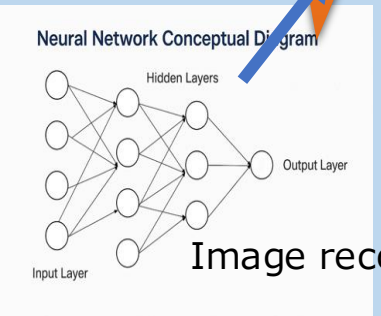


Image recognition AI

ResNet-50: Approximately 25.6 M
Vision Transformer: Approximately 86.0 M

Amount of parameters stored in SRAM

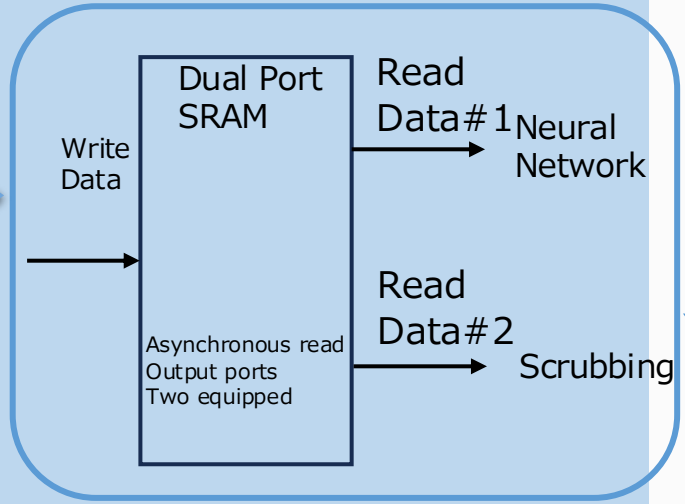
- Weaknesses in the latest semiconductor technology is the weakness in dependability of SRAM
- The reduction in cell capacitance due to miniaturization is the cause
- Software errors are unavoidable

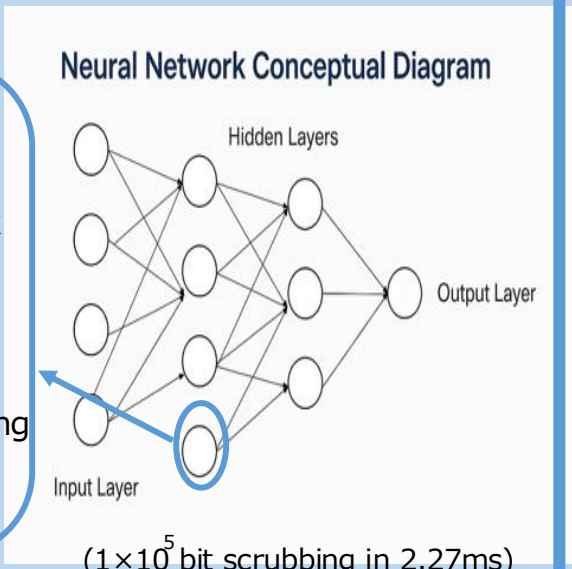
SEU 1.2×10^{-7} events/bit/day

Estimated Single-Event Upset (SEU) occurrence rate due to cosmic radiation (CRÈME96 AP8MAX model / Solar Minimum) when operating at a low orbit (500 km, 51.6°) in 7nm node SRAM (AMD data)

Detects errors within one second

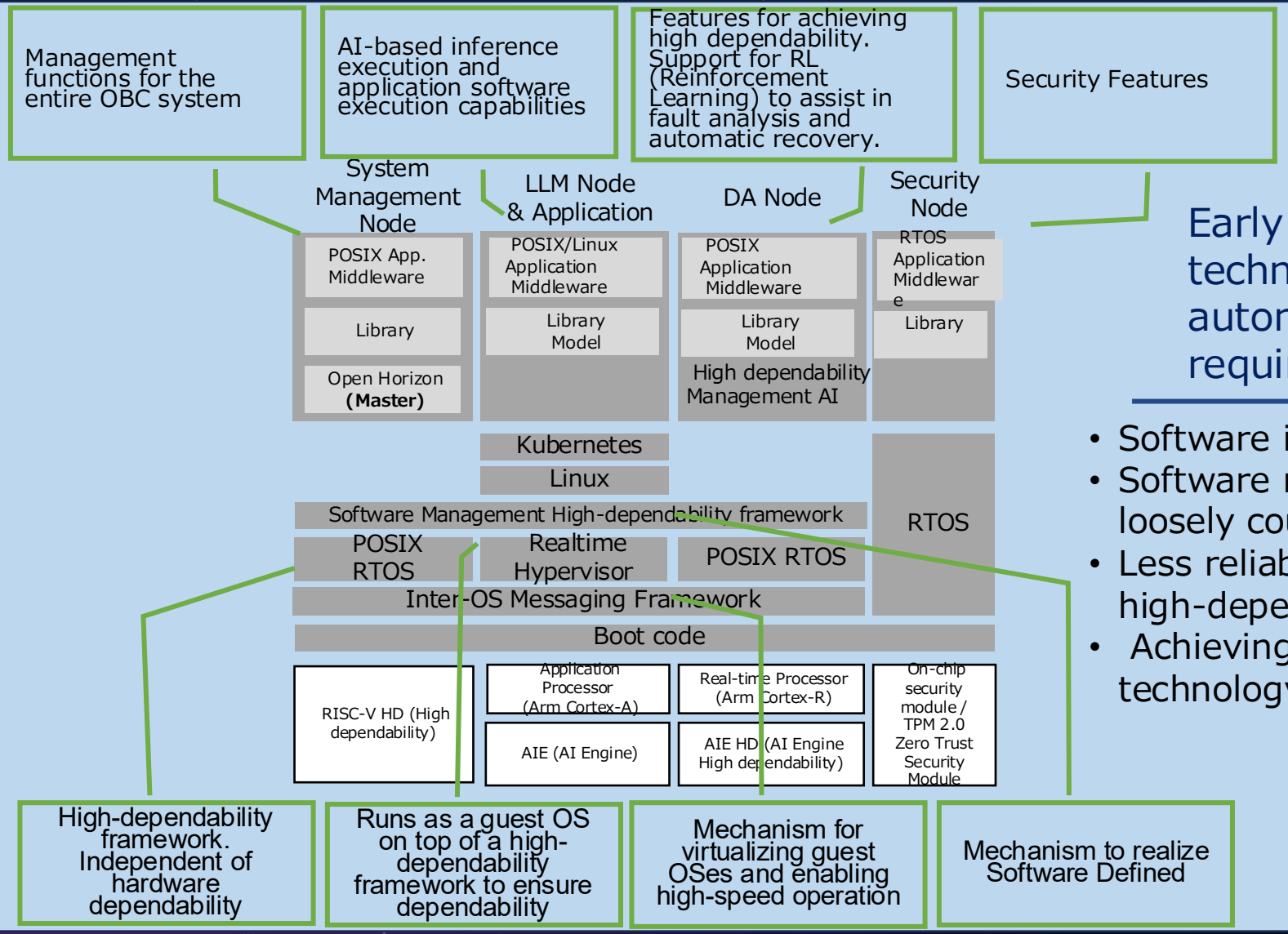
Achieved without overhead for AI operations





(1×10^{5} bit scrubbing in 2.27ms)

DIOS software architecture



Early adoption of high-dependability technologies meeting next-generation autonomous vehicle functional safety requirements (ISO 26262)

- Software is dedicatedly assigned to individual CPUs.
- Software running on CPUs or accelerators is each loosely coupled.
- Less reliable Linux runs as a guest OS on top of a high-dependability framework
- Achieving "Software Defined" through container technology (Kubernetes)

FDIR: Fault Detection, Isolation, and Recovery

- NASA document: “Fault-Detection, Fault-Isolation and Recovery (FDIR) Techniques : Utilize FDIR Design Techniques to provide for Safe and Maintainable On-Orbit Systems”, https://extapps.ksc.nasa.gov/Reliability/Documents/Preferred_Practices/dfe7.pdf
  - Detecting faults, such as a sensor failure or physical component malfunction
  - Isolating the source of the anomaly
  - Recovering from the fault and mitigating its effect on the system

[DIOS]
- Fault signals are captured by sensors including silicon heartbeat, lockstep mechanisms, and software heartbeat.
- Every step of D/I/R is processed by cooperation of System Management Node with RISC-V HD Processor and DA Node with AIE HD.
- Autonomous control and management

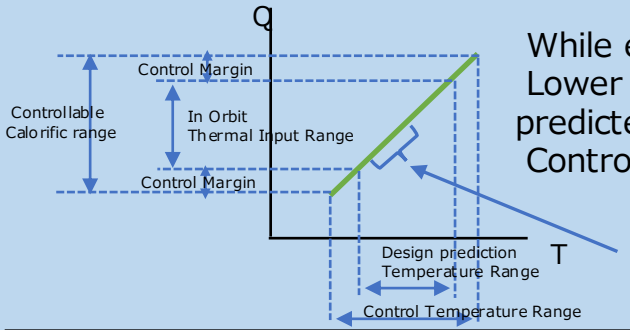
Autonomous control of dependability and energy consumption

Types of Damage Recovery in DIOS

Selecting the appropriate damage recovery from unpredictable cosmic ray-induced errors with many timing variations and dynamically changing hardware resource states

- Reset of specific IP core: 10 nsec
- Re-execution of specific software (function): Several microseconds until re-execution begins
- OS Reload: 5 to 10 sec
- System reset: 10 sec
- Disabling specific IP cores: Several microseconds until disabled
- Disabling specific memory and specific memory regions: Several microseconds until disabled
- FPGA restart: Several milliseconds
- IP core latch circuit reload: Several milliseconds

Thermal Control in the Core Unit



While ensuring control margin
Lower limit of the design predicted temperature range
Control near the lower limit

Control within this range

Using AI to analyze data obtained from power consumption (current values) and temperature (temperature sensors), the Core Unit proactively controls heat generation to ensure it always remains below the TDP using the following three functions:

- Function to reduce energy consumption by lowering the clock frequency
- Clock gating function
- Power gating function

Dynamically changing large amounts of hardware resources
Control the status of

Objective Function

- Minimize energy consumption = heat generation
- Maximize computational performance
- Maximize system lifetime

Variables

・OBC	x10
・Application CPU	x80
・Real-time control CPU	x100
・RISC-V HD	x10
・AI Engine	x10
・AI Engine HD	x10

All of the above: Clock frequency, clock supply, power supply, reset, and function stop

Constraints

- Radiation error types and frequency
- MTBF / MTTR
- Response time
- Maximum energy consumption
- Maximum Heat Generation
- Thermal Control Limit Ranges
- Workload size

Mathematical optimization is small-scale but becomes complex due to dynamic changes

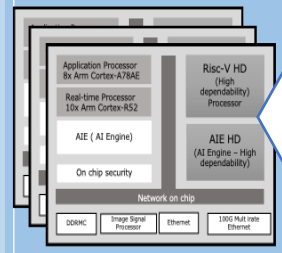
Using reinforcement learning and mathematical optimization
Application of AI inference

The AI Engine HD and DA node software suite enables highly reliable and high-speed control of the status of each hardware resource

Reinforcement Learning (Deep Reinforcement Learning)
AI Model

AI Model Training Environment

MP-SoC State Model



Interaction

Dynamic Scenario Generator

Rapidly auto-generates simulation operation scenarios with dynamically changing interactions

1. Automatically generates unintended (unpredictable) simulation scenarios. Complies with autonomous vehicle safety standard SOTIF-ISO/PAS21448.
2. Achieves high-speed automatic generation with low computational cost by incorporating bio-inspired Active Matter technology into dynamic interaction calculations

AUTONOMY

RL-based inference of the whole MPSoC fleet

Reinforcement learning plus mathematical optimization controls clock, power, reset and function-stop across a large, fast-changing resource set — in milliseconds, on orbit.

Variables

- Per-IP clock frequency & supply
- Power rails / gating
- Reset & function-stop
- Across 10 OBC · 80 app-CPU · 100 RT-CPU · RISC-V HD / AIE / AIE HD

Objectives

- Minimize energy = heat
- Maximize compute performance
- Maximize system lifetime

Constraints

- Radiation fault types & rate
- MTBF / MTTR · response time
- Max energy / heat · thermal limits
- Workload size

Trained safely on the ground. A dynamic scenario generator auto-creates unpredictable fault timelines (SOTIF / ISO PAS 21448 spirit); on orbit the agent's authority is bounded for safety. The AI Engine HD + RL node execute control quickly and dependably.

05

THERMAL

Heat control

PLATFORM

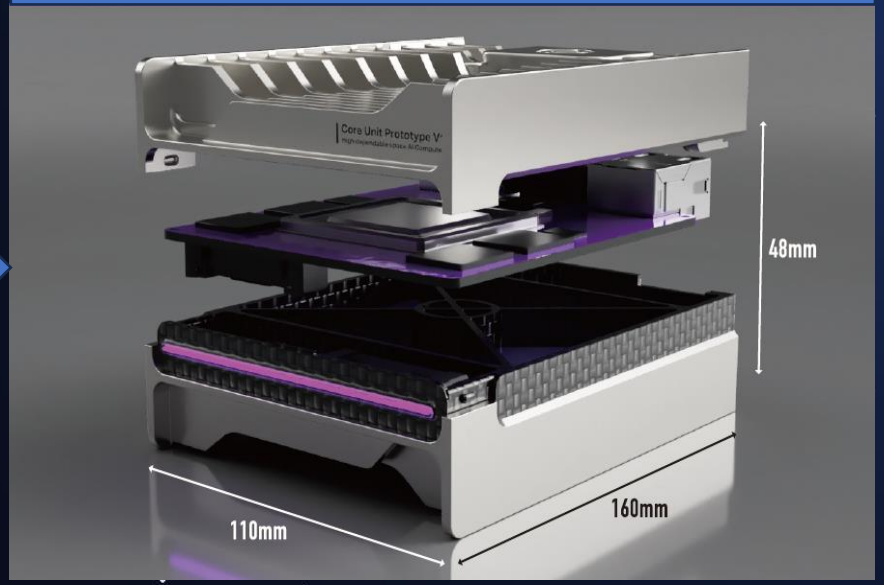
DIOS: OBC and Core Unit

OBC: On-Board Computer

OBC
example

x 2

Core Unit

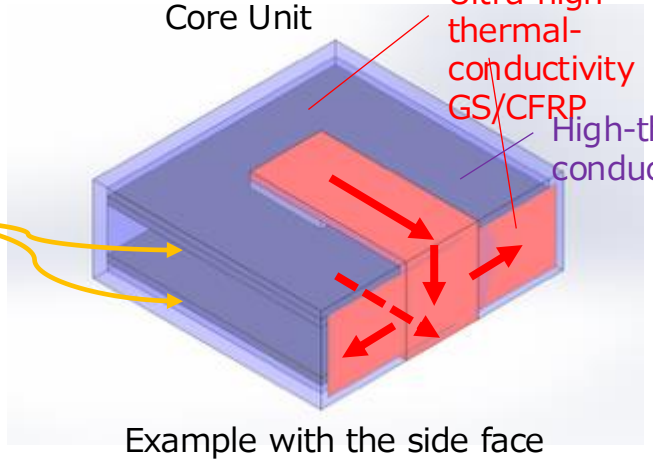


- For system redundancy
- For performance in parallel

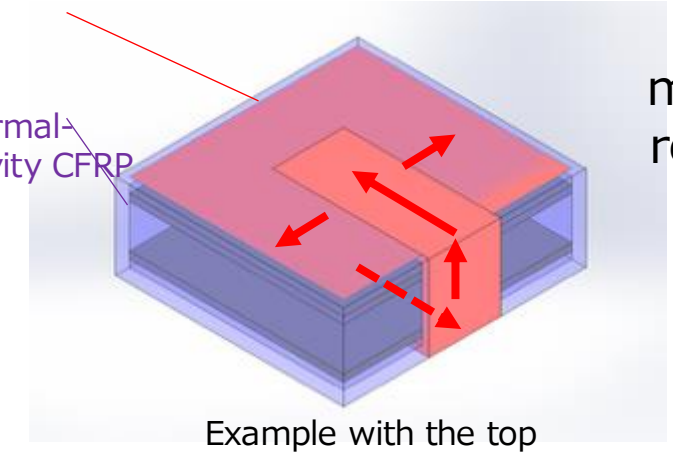
Heat transfer with new material

- Thermal radiation is the only way to dissipate heat in space.
- On the other hand, it is necessary to rapidly transport heat from the heat source to thermal radiators.
- Since heat is transported by conduction, materials with high thermal conductivity must be used in the conduction path.
- We adopted GS/CFRP, a new material that has twice the thermal conductivity of copper and is extremely lightweight.

OBC example



Example with the side face (right) as the heat-rejection surface (I/F)



Example with the top face as the heat-rejection surface (I/F)

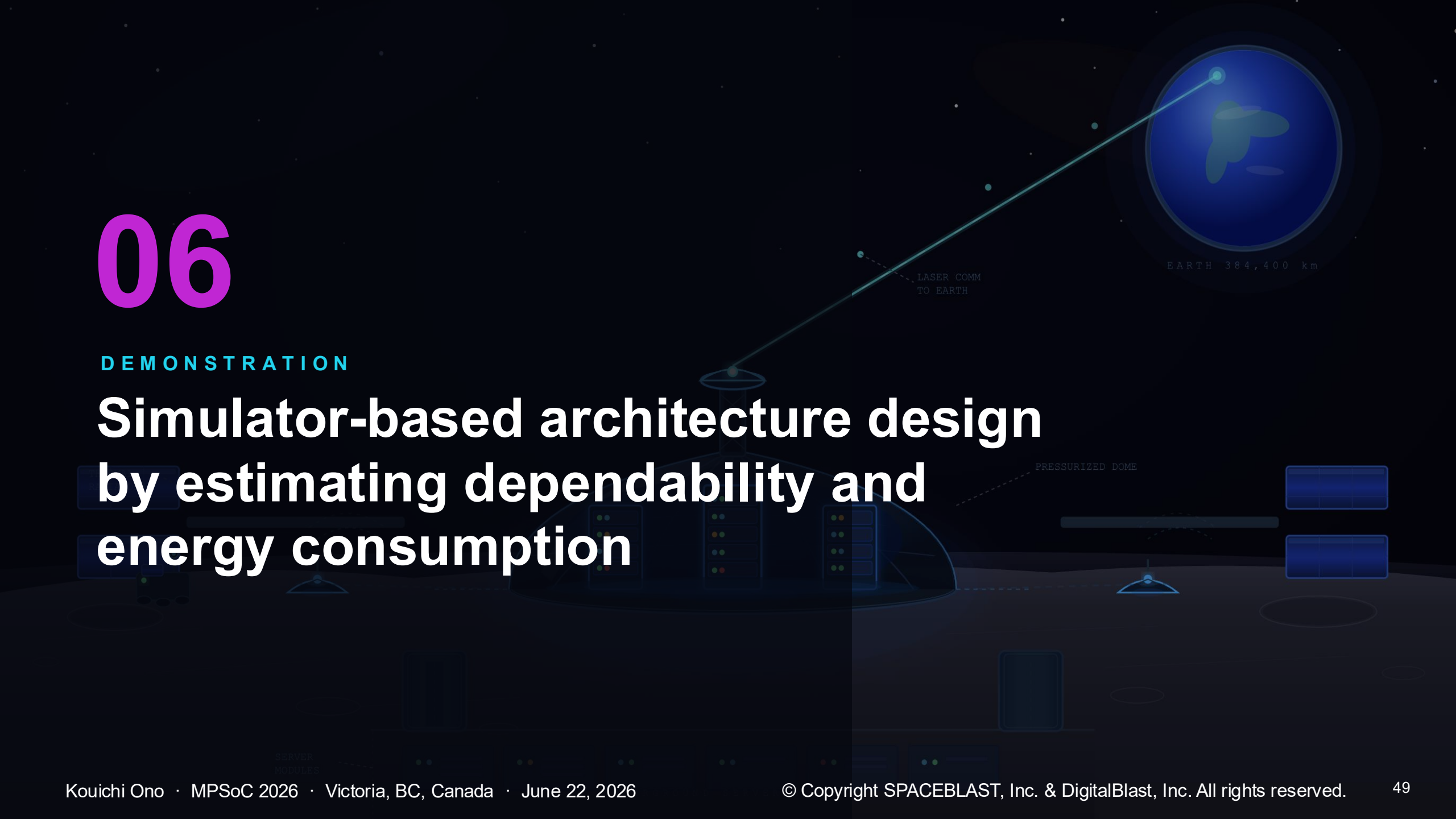
OBC Core Unit mounting and the heat-rejection path via ultra-high-thermal-conductivity GS/CFRP

THERMAL

AI-based heat control

Data obtained from power consumption (current) and temperature (sensor) is analyzed with AI; using the following three functions, the Core Unit proactively controls its heat generation to always stay at or below TDP.

- Core Unit: function using the MPSoC-resident AIE-HD to slow the clock frequency supplied to key IP, reducing energy consumption
- Similarly, a function that stops the clock to reduce energy consumption (clock gating)
- Function that cuts power to key IP to reduce energy consumption (power gating)



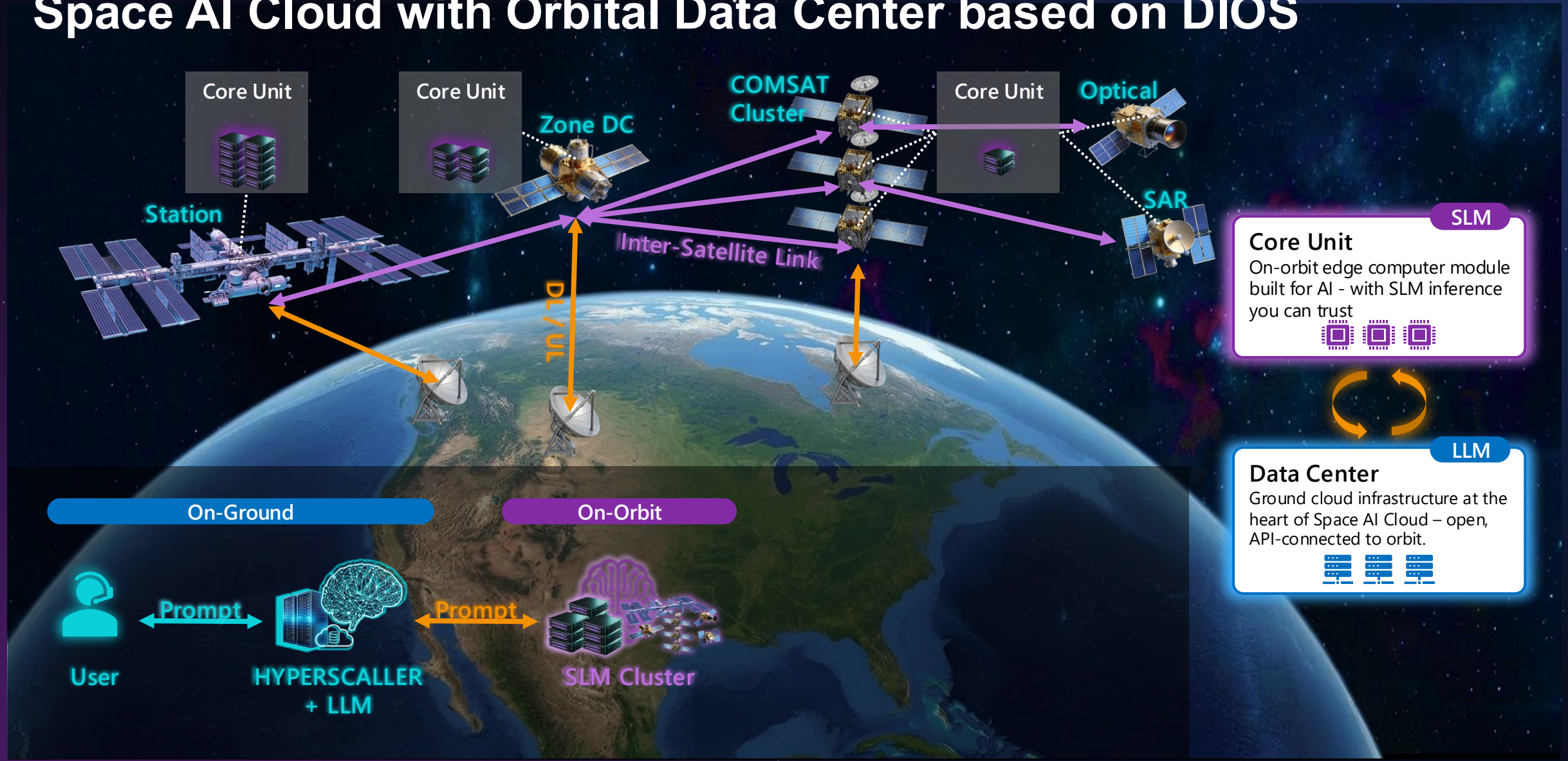
06

DEMONSTRATION

Simulator-based architecture design by estimating dependability and energy consumption

CONCEPT

Space AI Cloud with Orbital Data Center based on DIOS



SLM

Core Unit

On-orbit edge computer module built for AI - with SLM inference you can trust

LLM

Data Center

Ground cloud infrastructure at the heart of Space AI Cloud – open, API-connected to orbit.

VALIDATION

Proven on the ground, then on orbit

Ground: accelerator / proton-beam irradiation — SEE screening & coverage measurement

Build a prototype → verify function & radiation hardness → compute high-dependability coverage and validate it.

Program timeline

- **2026–28** — LEO test payload on orbit; first dependability data
- **2027** — Stage Gate — prototype function & rad-hardness verified
- **2028–30** — On-orbit demonstrations on ISS / commercial stations & satellites
- **2030–32** — Commercial orbital data center; licensing of the hardening IP

Highly-Dependable Computing for Orbital Data Centers

An MPSoC FPGA-Centric Approach

Thank you !!